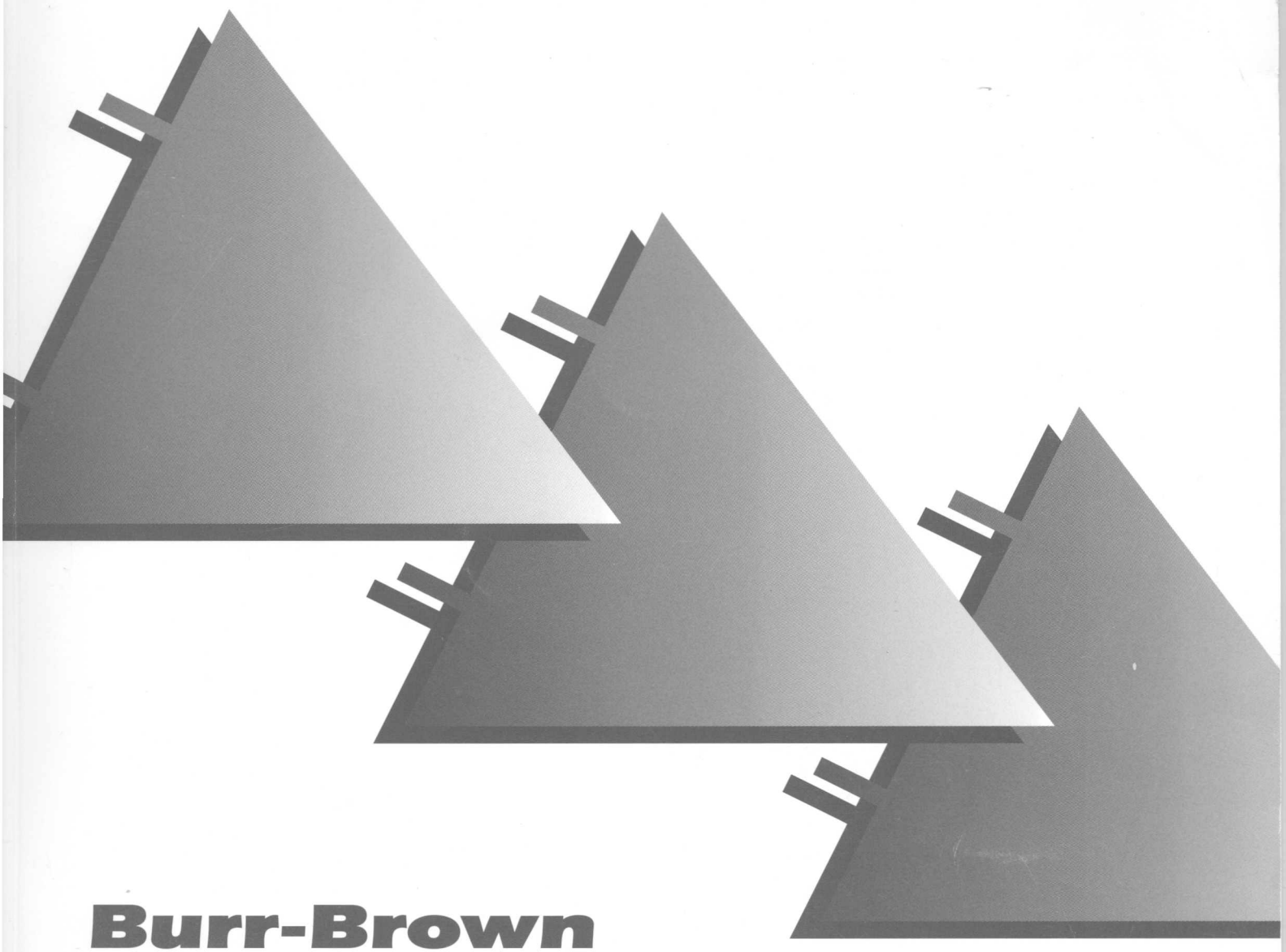

Burr-Brown

Collection of Applications Bulletins

BURR - BROWN®

TABLE OF CONTENTS

SECTION 11, High-Speed Data Converters

SECTION 13, Heat-Sinking and TO-3 Mounting

SECTION

CONTENTS BY AB-NUMBER

SELECTED PACKAGING MATERIALS

	MATERIAL	THERMAL CONDUCTIVITY (W/in-°C)			THERMAL EXPANSION (10^{-6}/°C)			TCR (10^{-6}/°C)	RESISTIVITY AT 20°C (μΩ-cm)
		NOM	LOW	HIGH	NOM	LOW	HIGH		
ELEMENTS	ALUMINUM	6.02	5.63	6.38	23.9	19.4	25	4290	2.66
	ANTIMONY	0.620	0.481	0.648(β)		8.46	10.8		41.7
	ARSENIC	1.28	1.08(α)	1.37(β)	4.7				33.3
	BARIUM	0.468			18				50.0
	BERYLLIUM	5.10	4.04	5.54(β)	12			25000	5.9
	BISMUTH	0.201(k)	0.134(a)	0.233(b)	13				106.8
	BORON	0.696	0.478(α)	0.808(β)	8.3				1.8×10^{12}(m)
	CADMIUM	2.46(k)	2.11(g)	2.62(d)	29.9			4200	6.83
	CALCIUM	5.10	3.20	5.23	22			4160	3.43
	CARBON	3.70(c)	0.0404(j)	58.9(z)		0.54	4.32		1375(l)
	CESIUM	0.912			97				20.0
	CHROMIUM(k)	2.38			6.1			3000	13.0
	COBALT(k)	2.54			12			6040	6.24
	COPPER	10.2			17			6800	1.673
	GALLIUM	1.04(e)	0.404(g)	2.24(f)	18				56.8
	GERMANIUM	1.53	1.18(α)	1.69(β)	5.9				10^2 - 10^7(t)
	GOLD (10.2 oz. troy/in^3)	8.08			14.2			4000	2.19
	HAFNIUM	0.584	0.569(α)	0.592(β)	5.9			3800	32.4
	INDIUM(k)	2.08	1.94(α)	2.12(β)	32				8.37
	IRIDIUM	3.73			6.8			3925	5.3
	IRON	2.04	1.85(h)	2.20(β)	11.7			6510	9.71
	LEAD	0.897	0.874(α)	0.904(β)	29.3			3360	20.65
	MAGNESIUM(k)	3.96			25			16500	4.46
	MANGANESE	0.198			22				185
	MOLYBDENUM	3.50			5.4				5.17
	NICKEL	2.31	2.10(α)	2.39(β)	13			6900	6.84
	NIOBIUM	1.36			7.1				12.5
	OSMIUM(k)	1.55			4.7			4200	9.5
	PALLADIUM	1.82			11.9			3770	10.8
	PHOSPHORUS		.0064(j)	.307(k)	126				10^{17}
	PLATINUM	1.82			8.8			3927	9.83
	RHENIUMk	1.22			6.7			3950	19.3
	RHODIUM	3.81			8.3			4200	4.51
	RUBIDIUM	1.48			90				12.5
	RUTHENIUM	2.97			9.6				7.6(l)
	SELENIUM	0.033(d)	0.013(j)	0.115(g)	38				12(AC)
	SILICON	3.78	2.1	4.27(β)	3.5[111](AB)	2.9	7.4		10^2 to 10^8(t)
	SILVER	10.9			19.6			4100	1.59
	STRONTIUM	0.899	0.826(α)	0.924(β)					23.0
	SULFUR(k)	0.0069	0.0039(α)	0.0073(β)	65				2×10^{23}(m)

NOTES: Values at 20°C unless otherwise specified. (α) At 100°C. (β) At 0°C. (a) || to triangle axis. (b) ⊥ to triangle axis. (c) Average value; graphite varies from 2.0 to 5.6 depending on type and orientation. Pyrolytic graphite is 0.16 and 50 ⊥ and || to layer planes. (d) Crystalline, ⊥ to c-axis; polycrystalline = 0.006W/in-°C. (e) || to a-axis. (f) || to b-axis. (g) || to c-axis. (h) Armco iron. (i) White phosphorous. (j) Amorphous. (k) Polycrystalline. (l) Resistivity at 0°C. (m) Intrinsic value, actual value sensitive to purity. (t) With 10^{21}/cm^3 to 10^{14}/cm^3 impurity concentration. (z) Type IIa diamond. (AB) Measured by J. Naylor. (AC) Crystalline, amorphous ≈ 10^6μΩ-cm.

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THERMAL AND ELECTRICAL PROPERTIES OF SELECTED PACKAGING MATERIALS (CONT)

	MATERIAL	THERMAL CONDUCTIVITY (W/in-°C)			THERMAL EXPANSION (10^{-6}/°C)			TCR [10^{-6}/°C]	RESISTIVITY AT 20°C [μΩ-cm]
		NOM	LOW	HIGH	NOM	LOW	HIGH		
ELEMENTS	TANTALUM	1.46			6.5			3830	12.4
	TELLURIUM	0.150			17				2×10^5
	TIN	1.70[k]	1.31[g]	1.89[d]	23	20	25	4700	11.5
	TITANIUM[k]	0.556	0.526[α]	0.569[β]	8.5				47.8
	TUNGSTEN	4.39	4.14	4.50	4.3	4.2	4.5	5240	5.6
	VANADIUM	0.780			7.7				24.8-26.0
	ZINC[k]	2.95				17	40	4190	5.8
	ZIRCONIUM	0.576	0.554	0.589	5.6			4400	41.0
ORGANIC	EPOXIES		0.0042	0.035		11.0	60		10^{21}[m]
	GLASS-EPOXY (PC-G10)	0.08			(n)	$10^{(n)}$	$15^{(n)}$		10^{21}[m]
	KAPTON	0.0039				34	40		10^{24}[m]
	NYLON		0.0054	0.0085		82.8	128		10^{20}[m]
	PARYLENE	0.0032				35	69		10^{22}[m]
	RTV	0.0053	0.004	0.008	930				3×10^{15}[m]
	TEFLON		0.0056	0.0296	83	50	162		10^{24}[m]
	MYLAR		0.0045	0.0073		60	95		10^{21}[m]
MISCELLANEOUS	AIR	0.00066							
	Al_2O_3	0.53[v]	0.42[w]	0.85[x]	6.7[v]	6.5	7.3		5×10^{21}[m]
	BRASS[p]	2.95				18	21	2000	6.4
	BeO	6.0	5.5	7.1	8.0	6.5	8.7		10^{22}[m]
	EUTECTIC (Au-Si) MP 370°C	5.5			13.7				2.53
	EUTECTIC (Au-Sn) MP 280°C	6.4			16				2.6
	EUTECTIC (Au-Ge) MP 356°C	6.7			12.6				2.6
	FERRITE	0.085		0.159		8	12		127×10^6
	GLASS[y]		0.010	0.037		0.55	12.4		10^{24}[m]
	KOVAR	0.425			5.5				49.0
	KOVAR-42	0.28			4.9				78
	MANGANIN	0.564	0.523	0.635	18.7			±15	44
	MICA	0.011	0.009	0.017		32.4	48.6		10^{21}[m]
	QUARTZ (SiO_2)	0.035	0.19[β][d]	0.37[β][g]	0.55				10^{24}[m]
	SAPPHIRE	0.821	0.691	1.0	6.67[q]	5.0[r]	8.33[s]		10^{25}[m]
	SOLDER (60/40)	1.0			23				13.5
	STEEL (1008)	1.2			12			6510	11
	STEEL, STAINLESS	0.35[303]	0.30[310]	0.94[501]	18[304]			170[AA]	112[AA]

NOTES: Values at 20°C unless otherwise specified. (α) At 100°C. (β) At 0°C. (d) ⊥ to c-axis. (e) || to a-axis. (f) || to b-axis. (g) || to c-axis. (k) Polycrystalline. (m) Intrinsic value; actual value sensitive to purity. (n) 40-300 for vertical axis. (p) Yellow brass. (q) || to c-axis at 50°C. (r) ⊥ to c-axis at 50°C. (s) || to c-axis at 500°C. (v) 96%. (w) 90%. (x) 99.5%. (y) See quartz. (AA) Nichrome 60% Ni, 25% Fe, 15% Cr.

THERMAL CONDUCTIVITY (K) CONVERSIONS

ORIGINAL UNIT	CONVERSION UNIT: cal / s-cm-°C	watt / cm-°C	watt / in-°C	BTU / hr-ft-°F	kg-cal / hr-m-°C	watt / m-°C
1 cal/s-cm-°C	1.0	4.186	10.63	241.9	360.0	418.6
1 watt/cm-°C	0.2389	1.0	2.540	57.8	86.00	100
1 watt/in-°C	0.09405	0.3937	1.0	22.75	33.86	39.37
1 BTU/hr-ft-°F	4.134(10^{-3})	0.01730	0.0440	1.0	1.488	1.730
1 kg-cal/hr-m-°C	2.778(10^{-3})	0.01163	0.0295	0.672	1.0	1.163
1 watt/m-°C	0.002389	0.01	0.0254	0.578	0.8600	1.0

EXAMPLE
232 (BTU/hr-ft-°F) x 0.0440
= 10.2 (watt/°C-in)

FORMULAE

$$°C/W = \frac{\text{Length (in)}}{\text{Area (in}^2\text{)} \cdot \text{K (W/in-°C)}}$$

BURR-BROWN®

APPLICATION GUIDE

Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85705
Tel: (602) 746-1111 • Twx: 910-952-111 • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

IMPLEMENTATION AND APPLICATIONS OF CURRENT SOURCES AND CURRENT RECEIVERS

This application guide is intended as a source book for the design and application of:

- Current sources
- Current sinks
- Floating current sources
- Voltage-to-current converters (transconductance amplifiers)
- Current-to-current converters (current mirrors)
- Current-to-voltage converters (transimpedance amplifiers)

This is not an exhaustive collection of circuits, but a compendium of preferred ones. Where appropriate, suggested part numbers and component values are given. Where added components may be needed for stability, they are shown. Experienced designers may elect to omit these components in some applications, but less seasoned practitioners will be able to put together a working circuit free from the frustration of how to make it stable.

The applications shown are intended to inspire the imagination of designers who will move beyond the scope of this work.

R. Mark Stitt (602) 746-7445

CONTENTS

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DESIGN OF FIXED CURRENT SOURCES

REF200 IC CURRENT SOURCE DESCRIPTION

The REF200 dual current source has two current sources plus a current mirror in an 8-pin plastic DIP (Figure 1). Because the circuit is fabricated with the Burr-Brown dielectrically isolated ***Difet***® Burr-Brown process, the three circuit blocks are completely independent. No power supply connections are needed to the chip. Just apply 2.5V or more to a current source for a constant 100µA output. Typical drift is less than 25ppm/°C and output impedance exceeds 500MΩ.

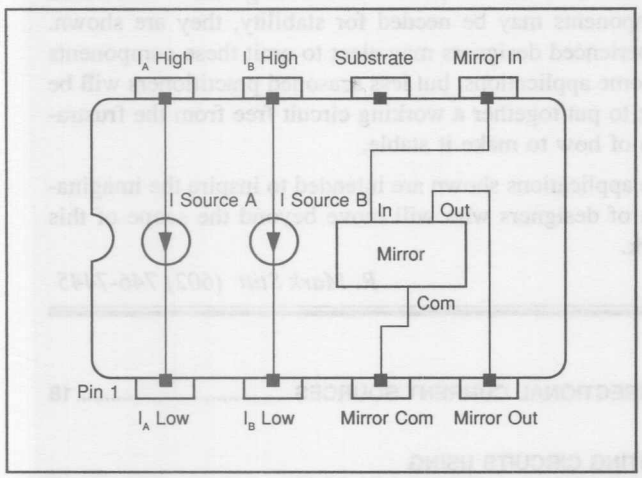

FIGURE 1. The REF200 Dual Current Source contains three completely independent circuit blocks—two 100µA current sources, and a current mirror.

The current mirror is useful in many applications. It uses a "full Wilson" type architecture as shown in Figure 2, with laser-trimming to ensure high accuracy.

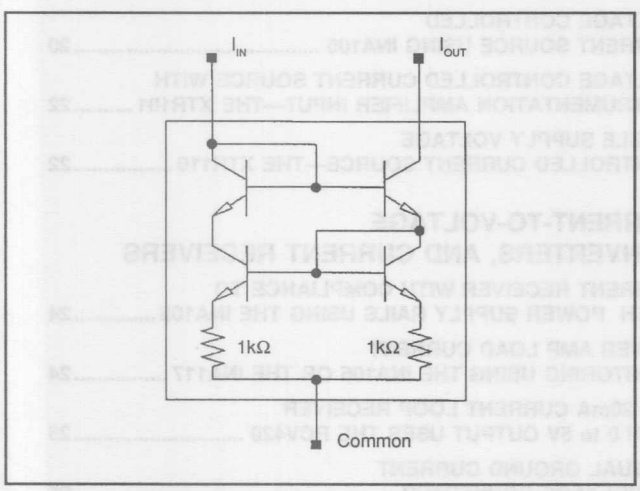

FIGURE 2. The REF200 Current Mirror uses a "full Wilson" architecture for high accuracy.

Each of the two current sources are designed as shown in Figure 3. Zero temperature coefficient (TC) is achieved by combining positive TC currents with a negative TC current. The positive TC currents are generated by a bandgap cell.

Current mirror Q_1– Q_2 forces equal currents to flow in 8/1 emitter ratioed devices Q_7 and Q_8. The proportional to absolute temperature (PTAT) voltage difference between the emitters—$(k \cdot t/q) \cdot \ln(8)$—is forced across the 4kΩ resistor resulting in a PTAT current of about 13µA. Because Q_{10} matches Q_7, and Q_3 matches Q_4, equal PTAT currents flow in each of the four Q_1 – Q_4 legs. The current in the Q_4 leg biases a Vbe/12kΩ current generator formed by Q_{11} and Q_{12}. The negative TC current from Q_{11} sums at the output. The 4kΩ and 12kΩ resistors are actively laser trimmed over temperature at wafer level to give an accurate zero TC output. NPN transistors Q_5, Q_6, and Q_9 cascode Q_7 and Q_8 for improved accuracy and output impedance. Likewise, J_1 and J_2 cascode Q_3 and Q_4. Using FET cascodes rather than PNPs eliminates noise due to base current. The capacitor provides loop compensation.

100µA was chosen as a practical value for the majority of applications. It is high enough to be used directly for sensor excitation in many instances, while it is low enough to be used in low power and battery powered applications where a higher current might be excessive. Also at higher output currents, thermal feedback on the chip and self heating would reduce the output impedance.

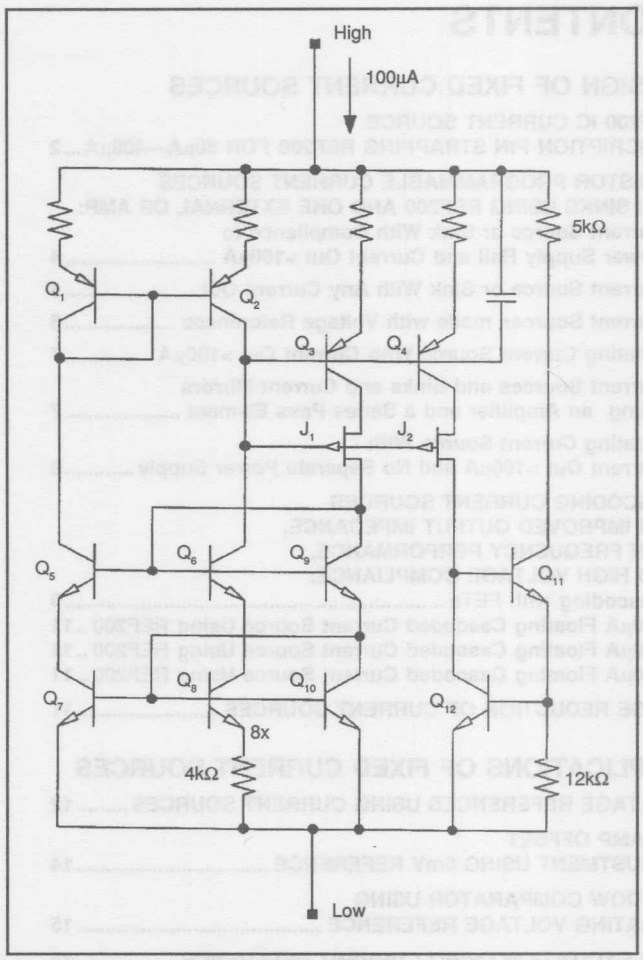

FIGURE 3. The REF200 Current Source cell is powered from its input terminals. It achieves zero TC by summing a positive TC current from a bandgap cell with a negative TC current.

Difet® Burr-Brown Corp.

construct a current source of any value. The REF200 can be pin strapped for 50µA, 200µA, 300µA, or 400µA, in addition to 100µA.

For a 50µA current sink, use the circuit shown in Figure 4. A 100µA current source is tied to the mirror common. Since a current mirror output must equal its input, 50µA flows in the input to ground, and the output is a 50µA current sink.

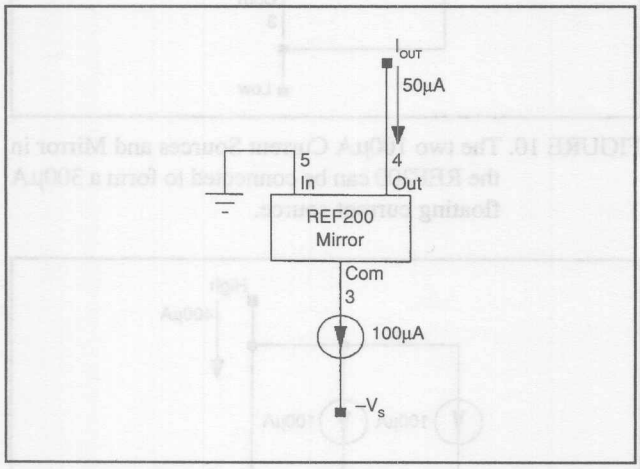

FIGURE 4. A 50µA Current Sink with compliance to ground can be made using one of the 100µA current sources and the mirror from the REF200.

PIN STRAPPING REF200 FOR: 50µA Current Source

For a 50µA current source, use the circuit shown in Figure 5. In this circuit a current sink subtracts 50µA from a second 100µA source leaving a 50µA source. Compliance is from below ground to within 2.5V of the positive rail.

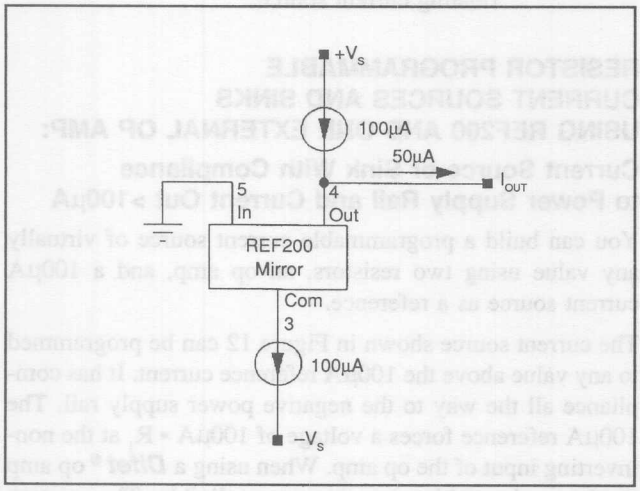

FIGURE 5. A 50µA Current Source with compliance from ground to $+V_S$ –2.5V can be made using both 100µA current sources and the mirror from the REF200.

negative rail with either a resistor and current source, or a resistor biased zener.

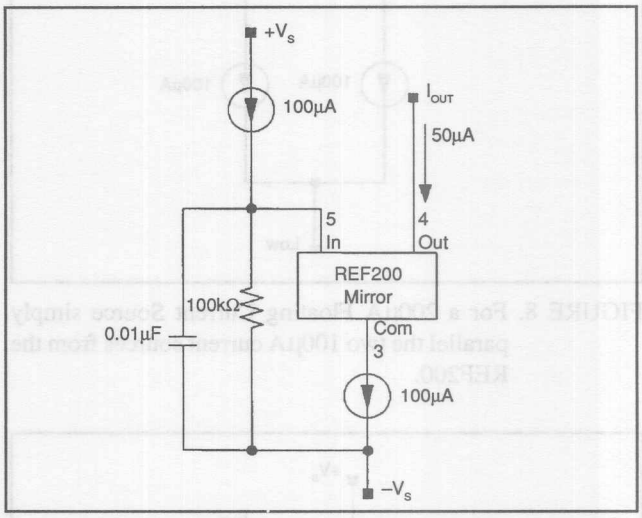

FIGURE 6. Compliance of the 50µA Current Sink (Figure 5) can be extended to $-V_S$+5V by referencing its bias point to the negative power supply rail using the other 100µA current and a resistor.

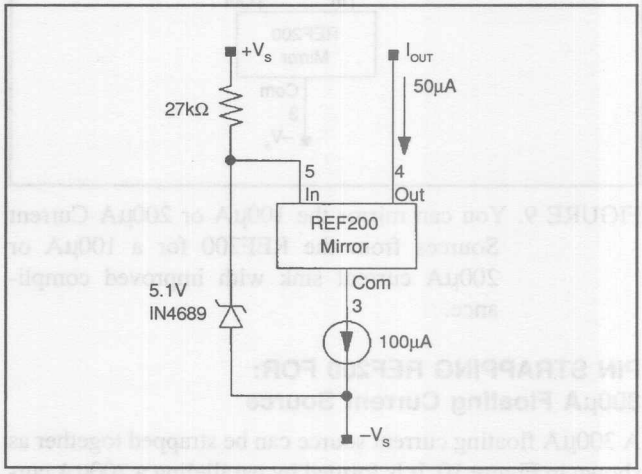

FIGURE 7. If you don't have a current source to spare, the 50µA Current Sink with compliance to $-V_S$+5V can be biased using a zener diode.

PIN STRAPPING REF200 FOR: 200µA FLOATING CURRENT SOURCE

A 200µA floating current source is formed by simply paralleling the two current sources as shown in Figure 8. For compliance nearer to the negative rail, use the mirror as shown in Figure 9. The output of the mirror can swing about a volt closer to the negative rail than the current source alone.

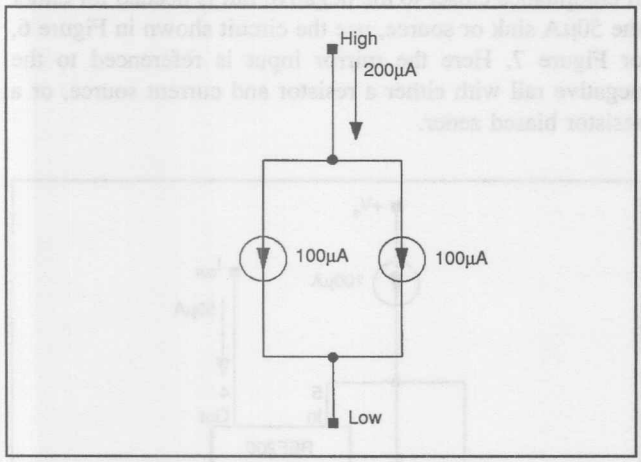

FIGURE 8. For a 200µA Floating Current Source simply parallel the two 100µA current sources from the REF200.

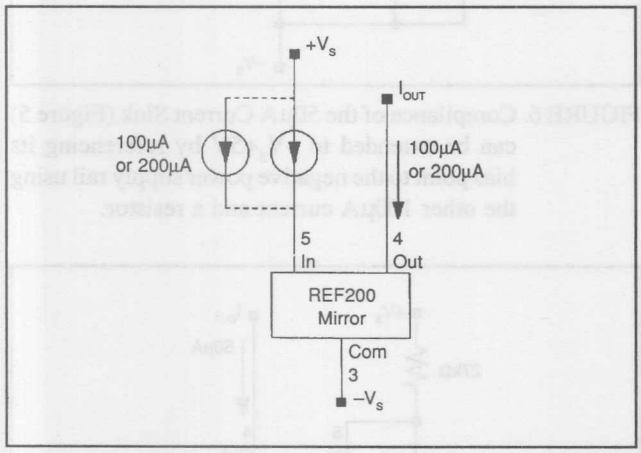

FIGURE 9. You can mirror the 100µA or 200µA Current Sources from the REF200 for a 100µA or 200µA current sink with improved compliance.

PIN STRAPPING REF200 FOR: 300µA Floating Current Source

A 300µA floating current source can be strapped together as shown in Figure 10. It is formed by paralleling a 200µA current source, made with one 100µA source and the mirror, with the other 100µA current source. The 200µA current source is made by connecting a 100µA current source to the mirror input so 100µA flows in the mirror output, and 200µA flows in the mirror common.

PIN STRAPPING REF200 FOR: 400µA Floating Current Source

A 400µA floating current source can be strapped together as shown in Figure 11. It is basically the same as the 200µA current source of Figure 10, except that 200µA is fed into the mirror input. This 200µA is summed with the 200µA that flows in the mirror output for a total of 400µA.

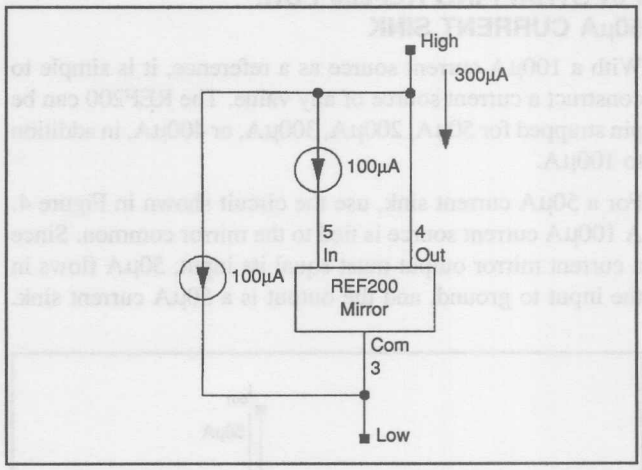

FIGURE 10. The two 100µA Current Sources and Mirror in the REF200 can be connected to form a 300µA floating current source.

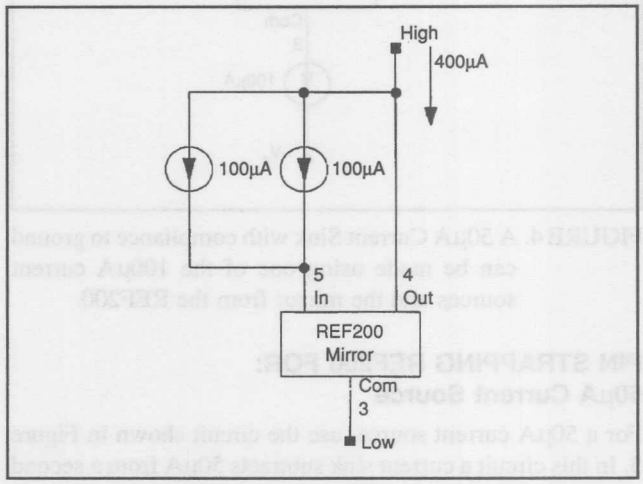

FIGURE 11. The two 100µA Current Sources and Mirror in the REF200 can be connected to form a 400µA floating current source.

RESISTOR PROGRAMMABLE CURRENT SOURCES AND SINKS USING REF200 AND ONE EXTERNAL OP AMP:

Current Source or Sink With Compliance to Power Supply Rail and Current Out >100µA

You can build a programmable current source of virtually any value using two resistors, an op amp, and a 100µA current source as a reference.

The current source shown in Figure 12 can be programmed to any value above the 100µA reference current. It has compliance all the way to the negative power supply rail. The 100µA reference forces a voltage of 100µA • R_1 at the noninverting input of the op amp. When using a ***Difet*** ® op amp as shown, input bias currents are negligible. The op amp forces the same voltage across R_2. If R_1 is N • R_2, the output current is (N+1) • 100µA. So long as the op amps input common mode range and its output can swing to the negative rail within the voltage drop across R_1, the current source can swing all the way to the negative rail. If the voltage drop across R_1 is large enough, any op amp can satisfy this

requirement. Figure 13 shows the same circuit turned around to act as a current sink. It has compliance to the positive rail.

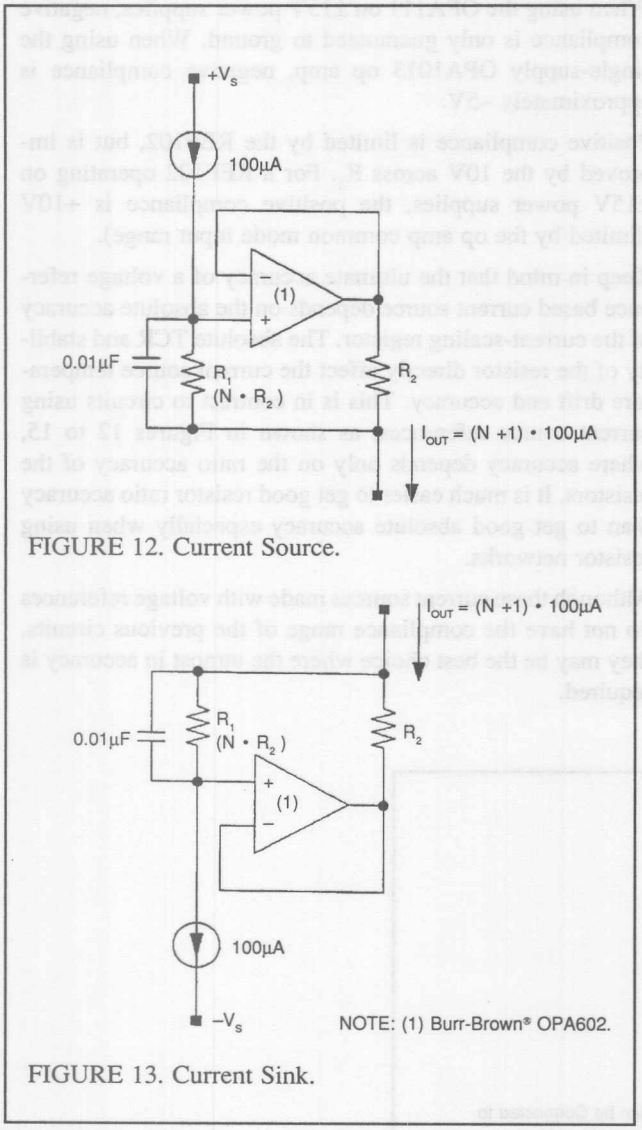

FIGURE 12. Current Source.

FIGURE 13. Current Sink.

FIGURES 12 and 13. For a programmable current source with any output current greater than 100µA and compliance to $+V_S$ or $-V_S$, use a 100µA current source as a reference along with an external op amp and two programming resistors.

Current Source or Sink With Any Current Out

For currents less than 100µA, use the circuits shown in Figures 14 and 15. They can be programmed for virtually any current (either above or below 100µA). In this case the 100µA current source forms a reference across R_1 at the inverting input of the op amp. Since the reference is not connected to the output, its current does not add to the current output signal. So, if R_1 is $N \bullet R_2$, then output current is $N \bullet 100\mu A$. Because compliance of the 100µA current source is 2.5V, the current source, Figure 14, can only comply within 2.5V of the negative rail—even if the op amp can go further. Likewise the current sink, Figure 15, has a 2.5V compliance to the positive power supply rail.

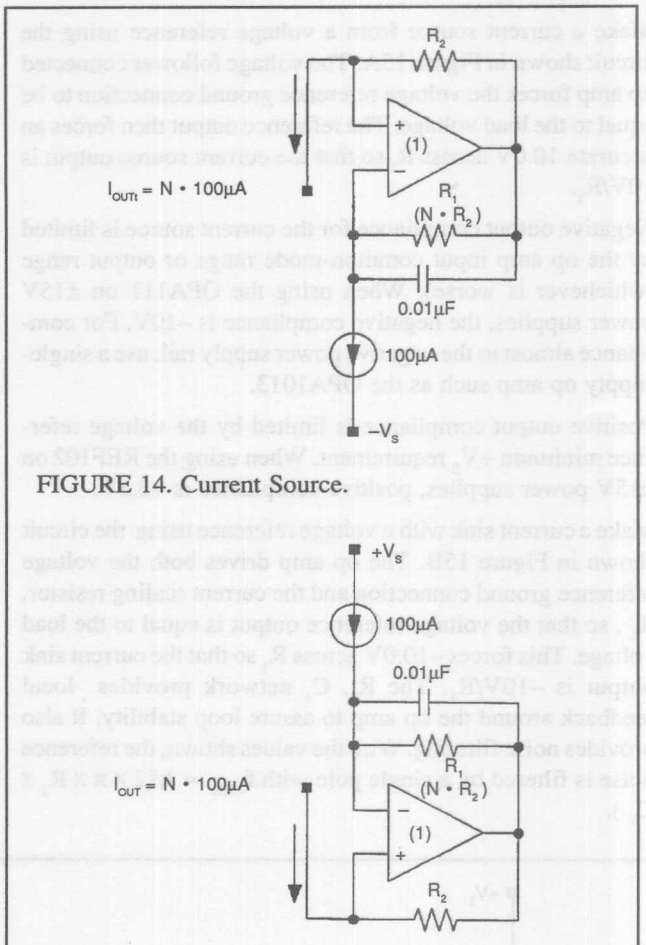

FIGURE 14. Current Source.

FIGURE 15. Current Sink.

NOTE: (1) Burr-Brown® OPA602 or OPA128.

EXAMPLES

R_1	R_2	I_{OUT}	
100Ω	10MΩ	1nA	→ Use OPA128
10kΩ	1MΩ	1µA	
10kΩ	1kΩ	1mA	

FIGURES 14 and 15. If you don't need compliance to the power supply rail, this circuit using a 100µA current source as a reference along with an external op amp and two programming resistors can provide virtually any output current.

Current Sources and Sinks Using Voltage References

To make a current source with the best possible accuracy use a zener-based voltage reference. The REF200 uses a band-gap type reference to allow low voltage two-terminal operation. Although this makes a more flexible general-purpose part with excellent performance, its ultimate temperature drift and stability cannot compare to the REF102 precision 10.0V buried zener voltage reference.

Make a current source from a voltage reference using the circuit shown in Figure 15A. The voltage follower connected op amp forces the voltage reference ground connection to be equal to the load voltage. The reference output then forces an accurate 10.0V across R_1 so that the current source output is $10V/R_1$.

Negative output compliance for the current source is limited by the op amp input common-mode range or output range (whichever is worse). When using the OPA111 on ±15V power supplies, the negative compliance is –10V. For compliance almost to the negative power supply rail, use a single-supply op amp such as the OPA1013.

Positive output compliance is limited by the voltage reference minimum $+V_S$ requirement. When using the REF102 on ±15V power supplies, positive compliance is +3.5V.

Make a current sink with a voltage reference using the circuit shown in Figure 15B. The op amp drives both the voltage reference ground connection and the current scaling resistor, R_1 , so that the voltage reference output is equal to the load voltage. This forces –10.0V across R_1 so that the current sink output is $-10V/R_1$. The R_2, C_1 network provides local feedback around the op amp to assure loop stability. It also provides noise filtering. With the values shown, the reference noise is filtered by a single pole with $f_{-3dB} = 1/(2 \times \pi \times R_2 \times C_1)$.

Negative output compliance for the current sink is limited by the op amp and further reduced by the 10V drop across R_1. When using the OPA111 on ±15V power supplies, negative compliance is only guaranteed to ground. When using the single-supply OPA1013 op amp, negative compliance is approximately –5V.

Positive compliance is limited by the REF102, but is improved by the 10V across R_1. For a REF102 operating on ±15V power supplies, the positive compliance is +10V (limited by the op amp common mode input range).

Keep in mind that the ultimate accuracy of a voltage reference based current source depends on the absolute accuracy of the current-scaling registor. The absolute TCR and stability of the resistor directly affect the current source temperature drift and accuracy. This is in contrast to circuits using current source references, as shown in Figures 12 to 15, where accuracy depends only on the ratio accuracy of the resistors. It is much easier to get good resistor ratio accuracy than to get good absolute accuracy especially when using resistor networks.

Although these current sources made with voltage references do not have the compliance range of the previous circuits, they may be the best choice where the utmost in accuracy is required.

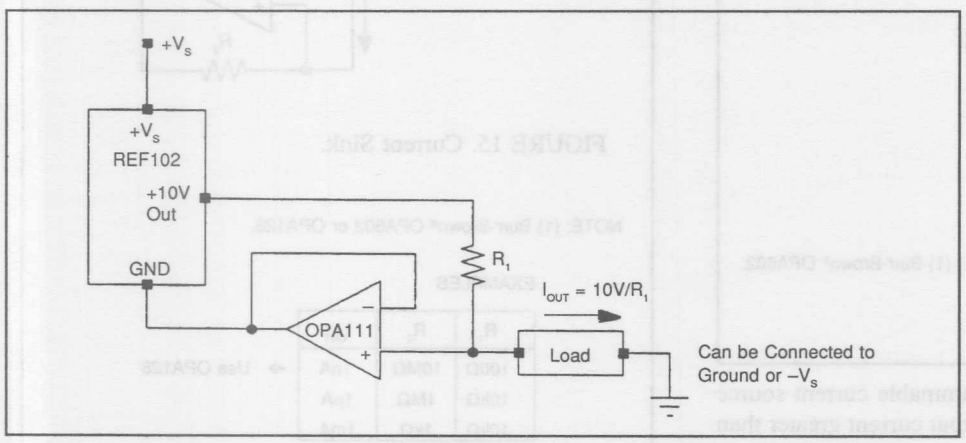

FIGURE 15A. Current Source using Voltage Reference and Op Amp.

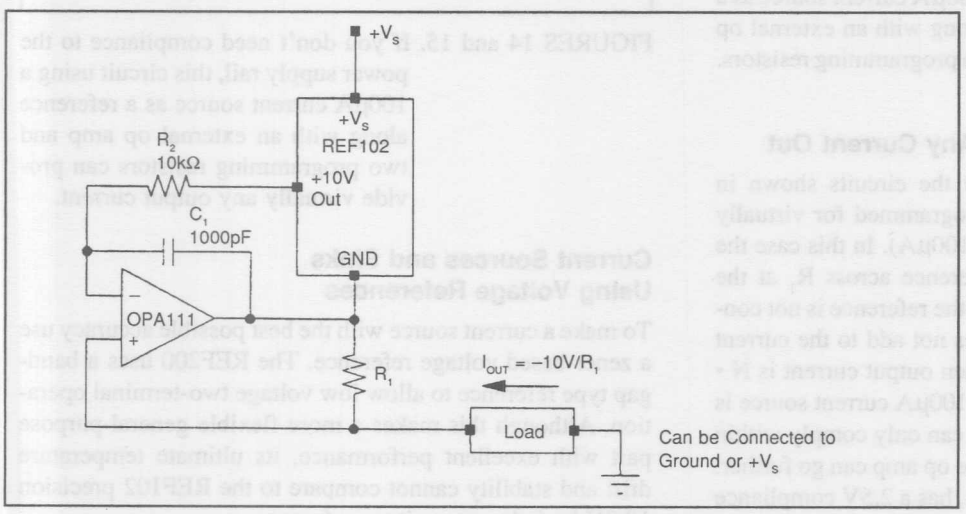

FIGURE 15B. Current Sink using Voltage Reference and Op Amp.

use the circuit shown in Figure 16. It is basically the same as the current source shown in Figure 12 except that R_2 is driven by a MOSFET. Since no current flows in the gate of the MOSFET or the inputs of the op amp, all current that enters the resistors (and no more) leaves. Therefore the current source is completely floating.

The power supplies of the op amp in this circuit, as in the other circuits, must be connected to $\pm V_S$. Also, the input and output common mode limitations of the op amp must be observed.

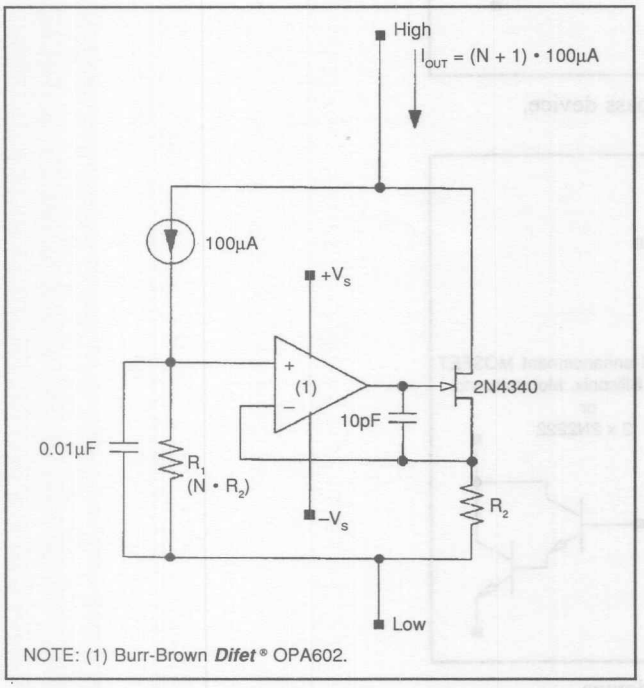

FIGURE 16. Use a 100µA Current Source as a reference, an external op amp, two programming resistors, and a series pass element for a programmable floating curent source.

Current Sources and Sinks and Current Mirrors Using an Amplifier and a Series Pass Element

In some applications it may be desirable to make a current source or sink using a series pass element in addition to an op amp. This approach provides the benefits of cascoding and also allows arbitrarily high current outputs.

The circuit used is the same as for the programmable floating current source shown in Figure 16. The difference is that the op amp power supply connection and reference input are both returned to a fixed potential. The result is either a current source or sink, but not a floating current source. The advantage is that the output can be any value, either more than, less than, or equal to the input reference. Also, a voltage source or even a variable voltage input can be used as a reference. The examples shown in Figures 17 through 20 show 100µA current sources used as references.

highly accurate no matter what the mirror ratio.

The pass element can bipolar, JFET, MOSFET, or a combination. The examples recommend MOSFETS because their low gate current minimizes output error. Also, MOSFETs with very high current ratings are available, and require no additional drivers.

In many cases bipolar devices are adequate and may be preferred due to their low cost and availability. With a bipolar device, the base current will add error to the output signal as discussed in the cascoding section. Using a darlington-connected bipolar device feeds the error current back into the signal path and reduces the error by the forward current gain (beta) of the input transistor.

In some high temperature applications, darlington-connected bipolar transistors may have lower error than FETs. As a rule of thumb, the gate current of a FET or MOSFET doubles for every 8°C increase in temperature, whereas the beta of a bipolar device increases approximately 0.5%/°C. Therefore, when operating at 125°C, the gate current of a FET will be about 6000 times higher than at 25°C, while the base current of the bipolar will be 1.5 times lower.

When selecting the op amp for this application, pay particular attention to input bias current, input common mode range, and output range.

The bias current of the op amp adds to the input current, and subtracts from the output current. For a 1:1 mirror application, the error is only the mismatch of bias currents or I_{OS} of the amplifier. For other ratios, assume that the error is equal to the full amplifier bias current. For most applications, the error will be negligible if a low bias current ***Difet***® amplifier such as the Burr-Brown OPA602 is used. Its I_B is 1pA max.

Be sure to observe the input common mode range limit of the op amp. For example, when using the OPA602 in a current sink application, the voltage between the op amp negative supply and its input must be at least 4V. In a split power supply application, R_1 and R_2 can be connected to ground, and the op amp negative supply can be connected to –5V or –15V and there is no problem. In a single supply application, or when R_1, R_2, and the op amp's $-V_S$ are all connected to the negative power supply, a drop of at least 4V must be maintained across R_1.

Using a single supply op amp allows the input common mode range to go to 0V. Especially in single supply current mirror applications, it is often desirable for the input and output to go to zero. The OPA1013 has an input common-mode range which extends to its negative power supply, and its output will swing within a few mV of the negative supply. Although the OPA1013 has bipolar inputs, its bias current is low enough for most applications.

Components R_3, R_4, and C_1 form a compensation network to assure amplifier stability when driving the highly capacitive inputs of some MOSFETs. In many applications they can be omitted.

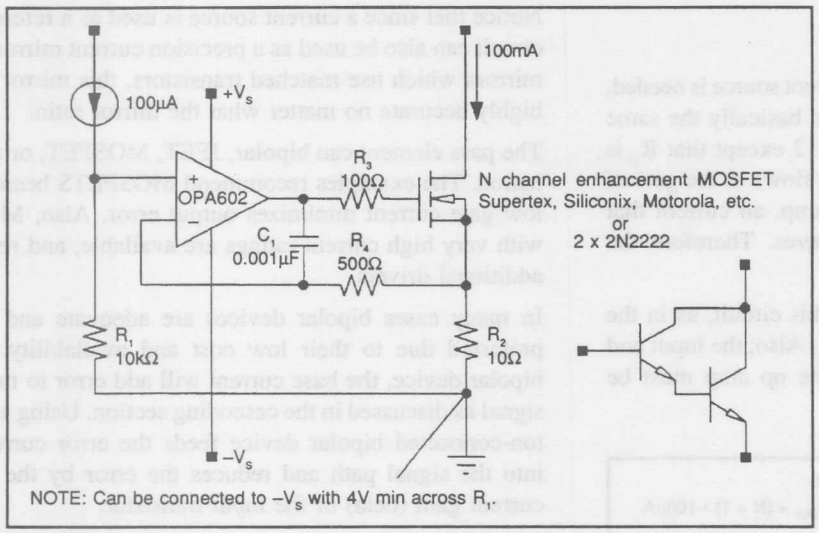

FIGURE 17. Programmable Current Sink using series pass device.

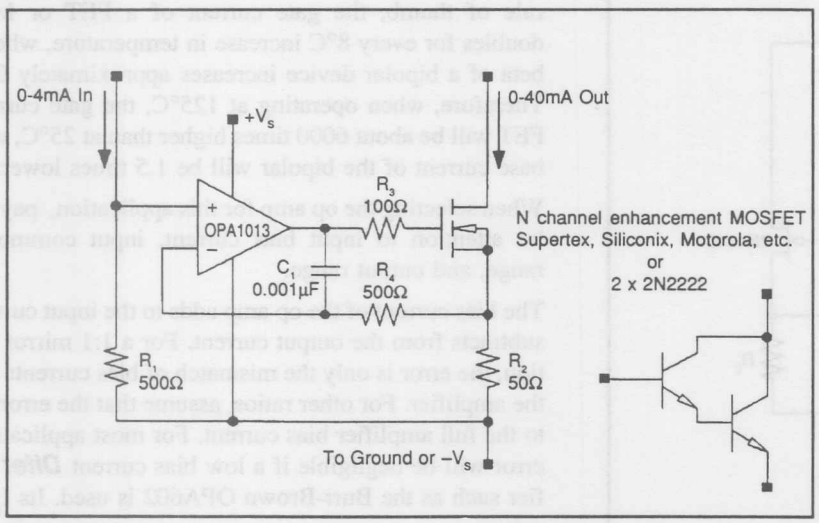

FIGURE 18. Sinking Current Mirror using series pass device.

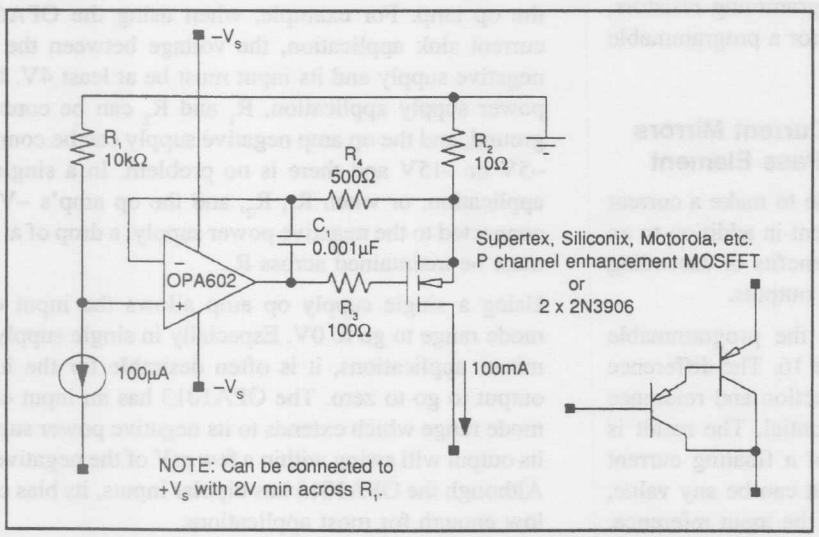

FIGURE 19. Programmable Current Source using series pass device.

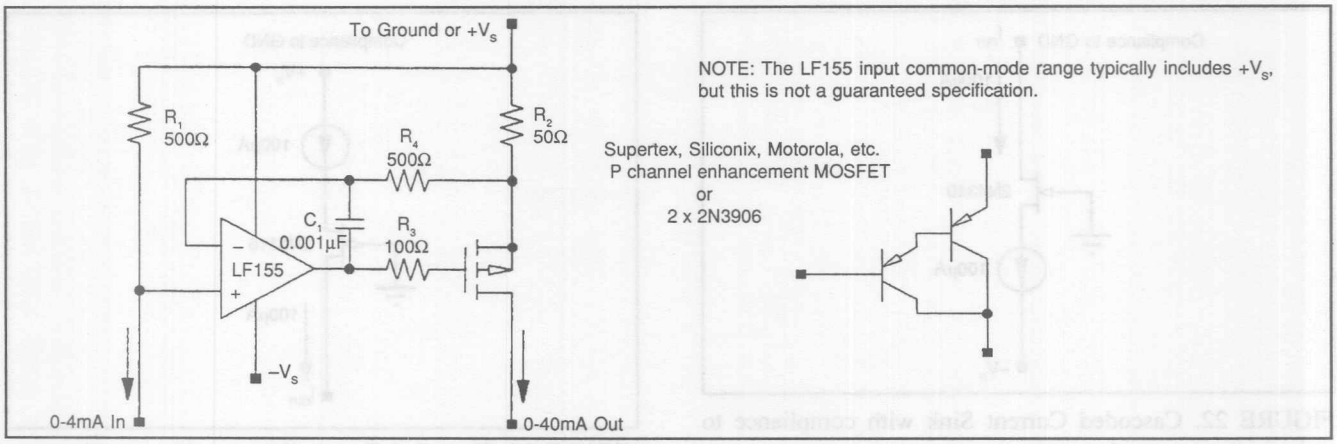

FIGURE 20. Sourcing Current Mirror using series pass device.

Floating Current Source With Current Out >100µA and No Separate Power Supply

If a programmable current source is needed, and no separate power supply is available, consider the floating current source shown in Figure 21. Here the op amp power supplies are connected to the current source input terminals. The op amp quiescent current is part of the output current.

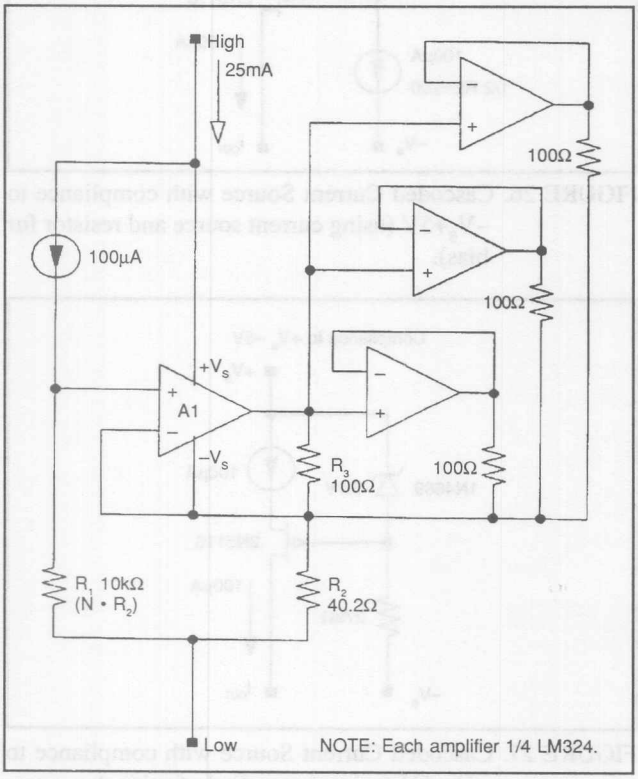

FIGURE 21. 25mA Floating Current Source using a quad single-supply op amp needs no external power supply.

There are two special requirements. First, a single supply op amp must be used (an op amp with an input common mode range that includes the negative supply rail). Also the output current must be greater than the op amp quiescent current.

The circuit is basically the same as Figure 12. The 100µA current flowing through R_1 produces a floating voltage reference at the non-inverting input of A_1. The op amp quiescent current flowing from its negative supply pin sums into the current flowing into R_2. The op amp outputs drive the additional current needed through R_2 so the voltage drop across it matches the voltage drop across R_1. If R_1 is N • R_2, the output current is (N+1) • 100µA. With the values shown, the output current is 25mA.

The op amp outputs are connected to R_2 through 100Ω resistors. The current delivered by A_1 produces an approximate 0.5V voltage drop across R_3. The other three op amps are connected as voltage followers so that the same voltage is dropped across the other three 100Ω resistors. The output current from each op amp is therefore equal and the load is shared equally. This technique allows any number of 10mA output op amps to be paralleled for high output current.

CASCODING CURRENT SOURCES FOR IMPROVED OUTPUT IMPEDANCE, HIGH FREQUENCY PERFORMANCE, AND HIGH VOLTAGE COMPLIANCE

Cascoding With FETs

The output impedance and high frequency performance of any current source can be improved by cascoding. Starting with a precision current source like the REF200 or any of the variations previously discussed, it is relatively easy to build a current source to satisfy just about any need.

Cascoding can also be used to increase high voltage compliance. High voltage compliance of a cascoded current source is limited solely by the voltage rating of the cascoding device. High voltage compliance of hundreds or even thousands of volts is possible.

Cascoding is the buffering of the current source from the load by a series pass device as shown in Figure 22. Here an N channel JFET cascodes the current source from the output. The gate of the JFET is tied to ground, its source to the current source, and its drain to the load. Variations in the load voltage are taken up by the drain of the JFET while the source voltage remains relatively constant. In this way, the voltage drop across the current source remains constant regardless of voltage changes across the load. With no changes in the voltage across the current source, and with no current lost through the JFET drain approaches infinity. AC performance of the cascoded current sink approaches that of the JFET.

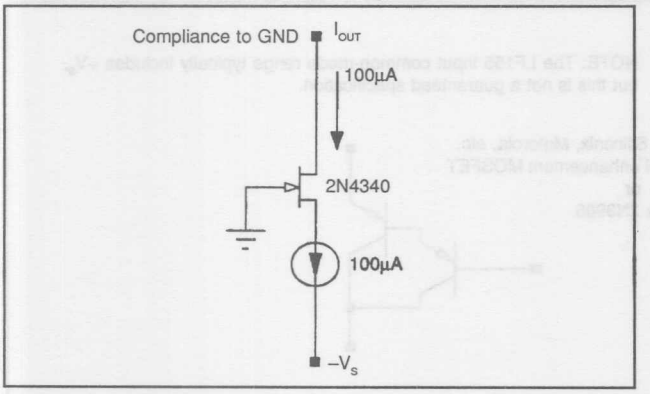

FIGURE 22. Cascoded Current Sink with compliance to ground.

Since the gate of the JFET is tied to ground, the output compliance is limited to near ground. If greater compliance is required for the current sink, the gate of the JFET can be referenced a few volts above the negative rail as shown in Figures 23 and 24. In Figure 23 the gate reference is derived from a resistor biased from the second current source. If a current source is not available, use a resistor biased zener as shown in Figure 24.

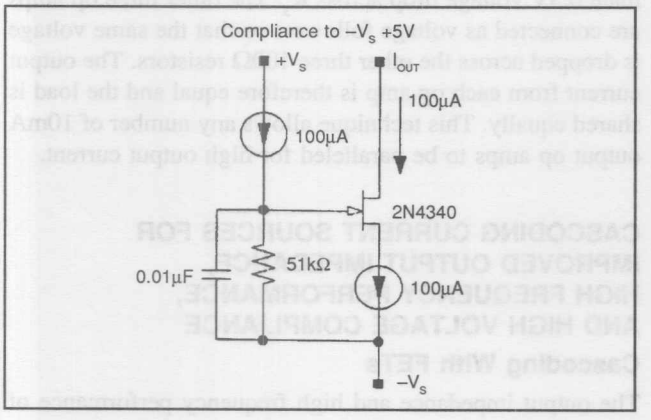

FIGURE 23. Cascoded Current Sink with compliance to $-V_S$+5V (using zener diode for bias).

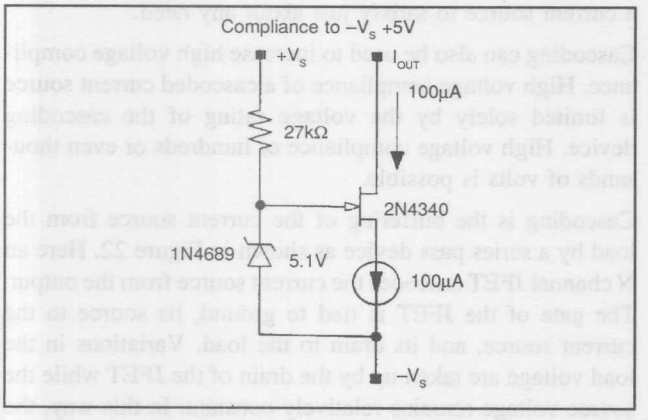

FIGURE 24. Cascoded Current Sink with compliance to $-V_S$+5V (using zener diode for bias).

To implement current sources, turn the circuits around and use P channel JFETs as shown in Figures 25 through 27.

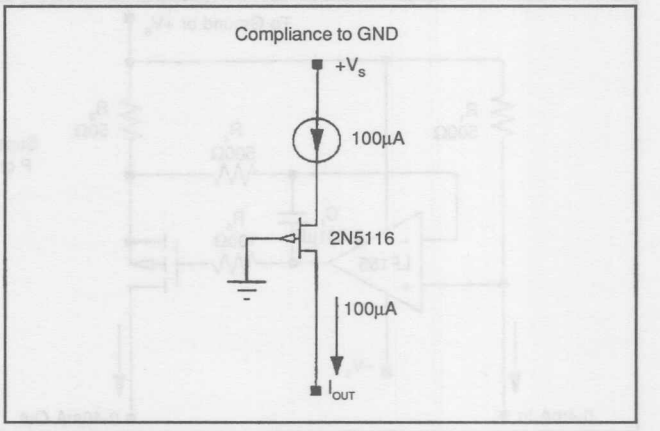

FIGURE 25. Cascoded Current Source with compliance to ground.

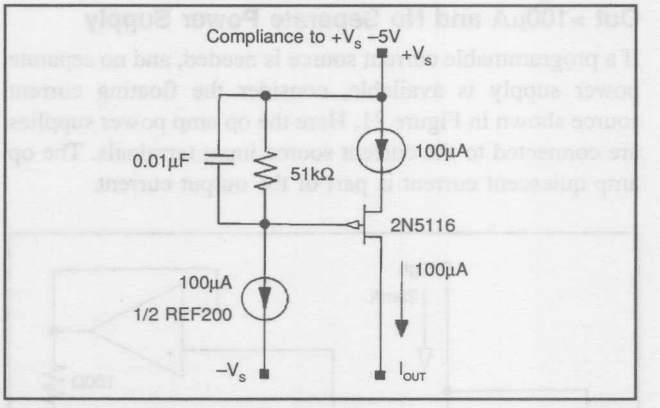

FIGURE 26. Cascoded Current Source with compliance to $-V_S$+5V (using current source and resistor for bias).

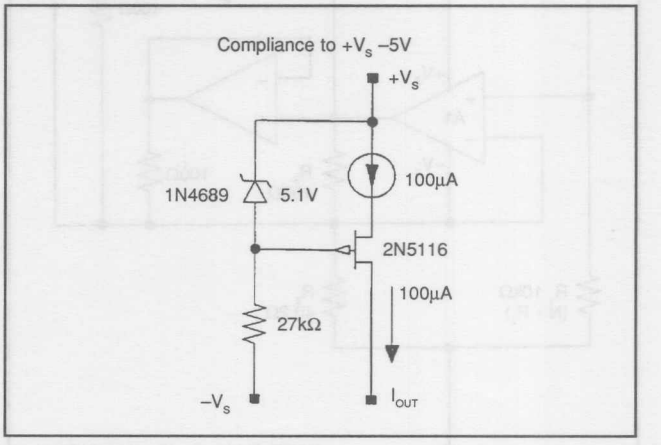

FIGURE 27. Cascoded Current Source with compliance to $-V_S$+5V (using zener diode for bias).

In most applications, JFETs make the best cascoding devices, but bipolar transistors and MOSFETs can also be used. MOSFETs can provide equivalent AC and DC performance to JFETs. Bipolar devices may offer better high frequency performance, but have a limited DC output impedance. The output impedance of a bipolar cascoded current source is limited by changes in base current with changes in collector voltage. The maximum output impedance of a bipolar cascoded current source is $b \cdot R_O$, where b is the current gain of the bipolar device, and R_O is its output impedance

pedances exceeding 10GΩ can be easily implemented. Using the REF200 and a few external devices, sources of 200µA, 300µA, and 400µA can be strapped together.

The 200µA floating cascoded current source is shown in Figure 28. It is made using a cascoded current source and a cascoded current sink each biasing the other. Low voltage compliance is limited to about 8V by the sum of the gate reference voltages. High voltage compliance is limited by the lower voltage rated FET.

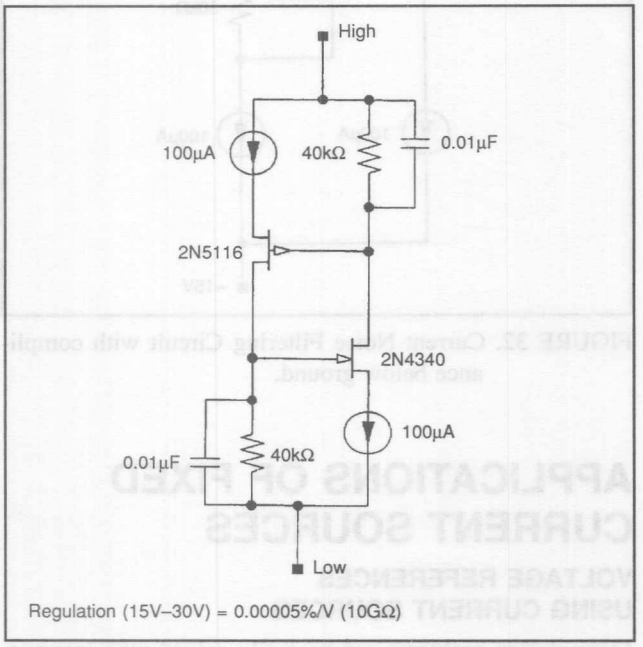

FIGURE 28. Cascoded 200µA Floating Current Source.

300µA Floating Cascoded Current Source Using REF200

The 300µA floating current source is shown in Figure 29. It is similar to the 200µA current source shown in Figure 28, except the current source in the cascoded sink section is derived from the mirror. The gate reference for the sink cascode is derived from the series combination of the mirror input and a 27kΩ resistor. The extra 100µA is obtained by summing the other 100µA current source into the sink cascode device. Compliance limits are the same as for the 200µA cascoded source.

400µA Floating Cascoded Current Source Using REF200

The 400µA floating cascoded current source is shown in Figure 30. It is the similar to the 300µA cascoded current source, except that the mirror is driven by a cascoded 200µA current source derived by the parallel combination of the two current sources in the REF200. The low voltage compliance of this circuit is about 1V better than the previous two circuits because the mirror compliance is about 1V better. High voltage compliance is still limited only by the breakdown of the lower rated FET.

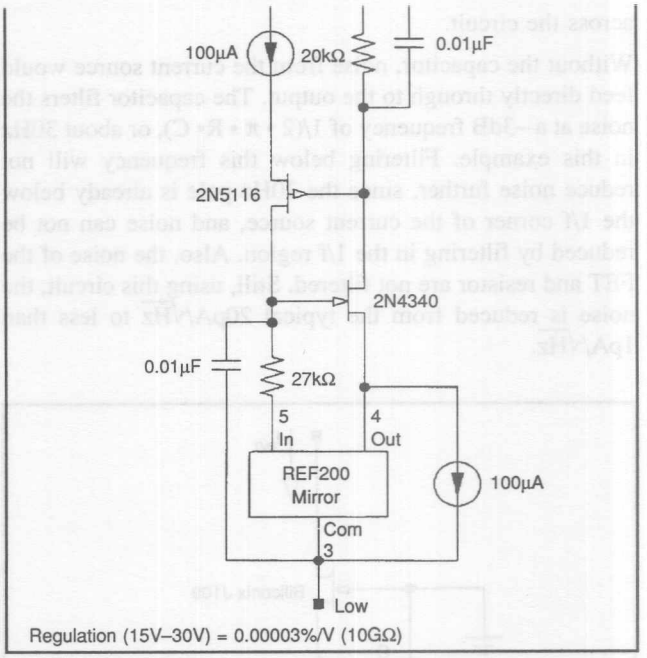

FIGURE 29. Cascoded 300µA Floating Current Source.

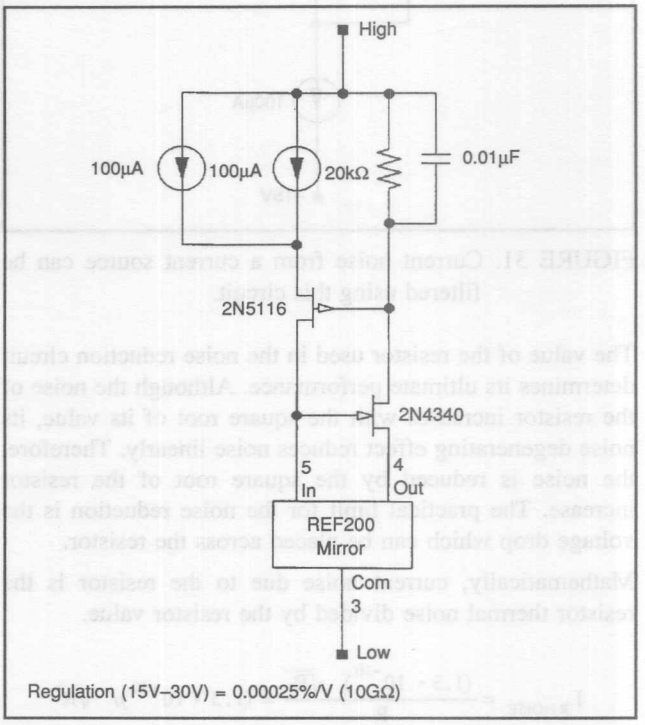

FIGURE 30. Cascoded 400µA Floating Current Source.

NOISE REDUCTION OF CURRENT SOURCES

In many modern systems, noise is the ultimate limit to accuracy. And in some systems, performance can be improved with a lower noise current source. Current source noise can be reduced by filtering, using the same basic principals used for noise reduction of voltage references. Reducing the noise bandwidth by filtering can reduce the total noise by the square root of the bandwidth reduction.

One current source noise reduction circuit is shown in Figure 31. It is basically a FET cascode circuit with the addition of an RC noise filtering circuit. The FET, as biased by the 100µA current source, forces an accurate DC voltage across the circuit.

Without the capacitor, noise from the current source would feed directly through to the output. The capacitor filters the noise at a –3dB frequency of $1/(2 \cdot \pi \cdot R \cdot C)$, or about 30Hz in this example. Filtering below this frequency will not reduce noise further, since the 30Hz pole is already below the 1/f corner of the current source, and noise can not be reduced by filtering in the 1/f region. Also, the noise of the FET and resistor are not filtered. Still, using this circuit, the noise is reduced from the typical 20pA/$\sqrt{\text{Hz}}$ to less than 1pA/$\sqrt{\text{Hz}}$.

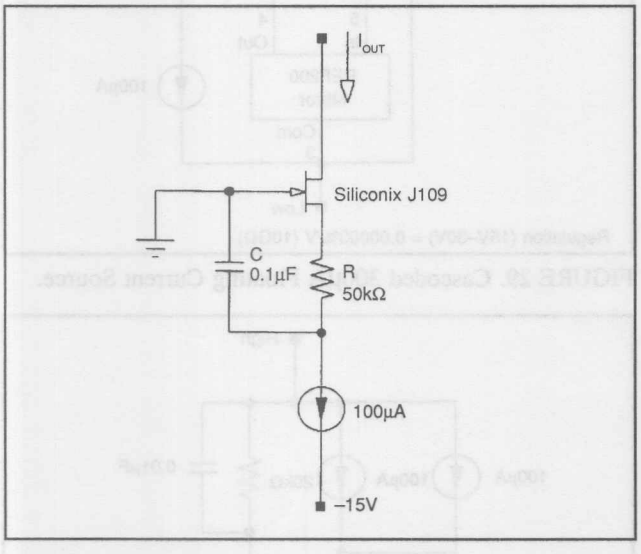

FIGURE 31. Current noise from a current source can be filtered using this circuit.

The value of the resistor used in the noise reduction circuit determines its ultimate performance. Although the noise of the resistor increases with the square root of its value, its noise degenerating effect reduces noise linearly. Therefore, the noise is reduced by the square root of the resistor increase. The practical limit for the noise reduction is the voltage drop which can be placed across the resistor.

Mathematically, current noise due to the resistor is the resistor thermal noise divided by the resistor value.

$$I_{R\,NOISE} = \frac{(1.3 \cdot 10^{-10})\ \sqrt{R}}{R} = (1.3 \cdot 10^{-10})/\ \sqrt{R}$$

With a 50kΩ resistor, the minimum theoretical noise is .6pA/$\sqrt{\text{Hz}}$, with 10kΩ, it is 1.3pA/$\sqrt{\text{Hz}}$. Noise measurements of the circuit using both 10kΩ and 50kΩ resistors and the Siliconix J109 FET agree with these theoretical numbers within 20%.

The noise reduction circuit in Figure 31 has a low voltage compliance limit near ground. For compliance below ground, use the circuit shown in Figure 32.

In addition to noise reduction, these circuits have the other advantages of a FET cascoded current sink; output impedance in the GΩ region, improved AC performance, and high voltage compliance limited only by the FET.

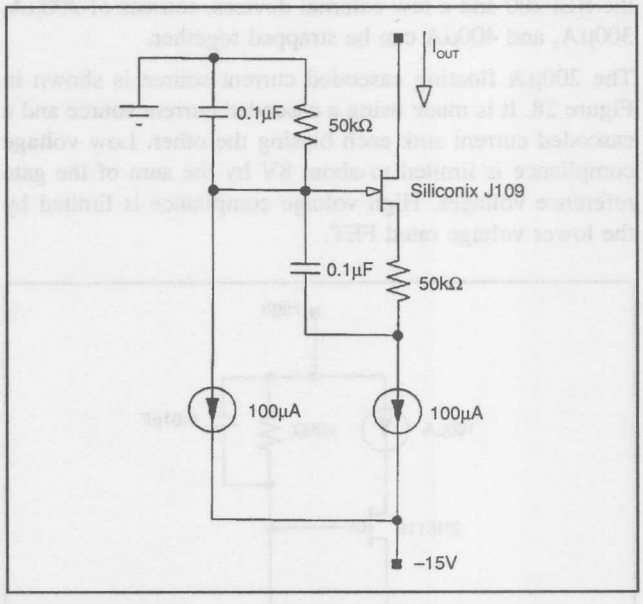

FIGURE 32. Current Noise Filtering Circuit with compliance below ground.

APPLICATIONS OF FIXED CURRENT SOURCES

VOLTAGE REFERENCES USING CURRENT SOURCES

Many design problems can be easily solved with inexpensive, easy-to-use current sources like the REF200. Although applications are endless, the collection of circuits that follows is intended to stimulate your thinking in several broad categories: fixed voltage references, floating voltage references, current excitation, fixed current references, steered current references, and biasing.

Current sources are a versatile means of forming voltage references. Why not just use a voltage reference? With a current source, a single resistor provides a programmable voltage source of any value. Low voltage references are often needed, and with this approach, it's as easy to get a 1mV reference as it is to get a 10V reference. Also, the voltage can be referenced anywhere—to the positive rail, the negative rail, or floating anywhere in between.

When impedances driven by the voltage reference are high, the voltage output from the resistor derived voltage reference can be used directly. The 100µV reference shown in Figure 33 can be used directly in voltage-to-frequency converter (VFC) auto-zero applications where an off-zero reference is needed (since zero frequency would take forever to measure, off-zero techniques are often used for calibrating VFCs). Where a lower output impedance is needed, a simple buffer can be added as shown in Figure 34.

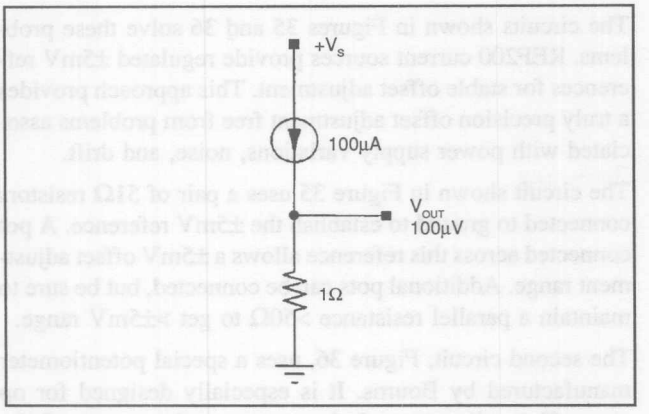

FIGURE 33. 100µV Reference for VFC off-zeroing.

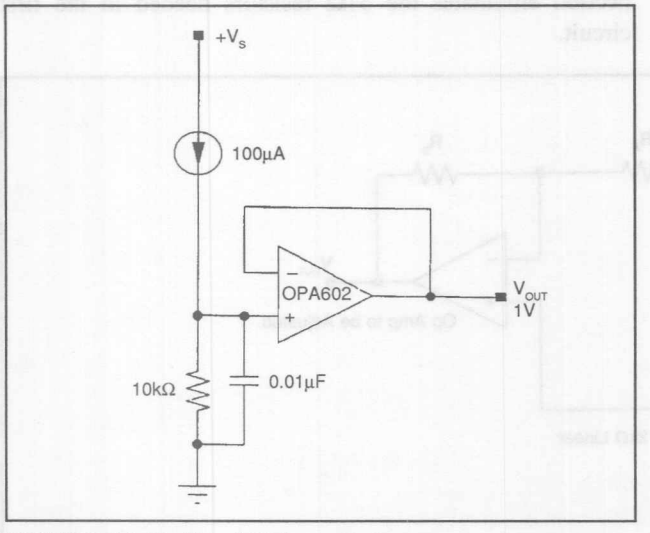

FIGURE 34. Buffered Voltage Reference.

For a floating voltage reference, simply drive the reference low side (grounded side of the voltage-setting resistor) as shown in Figure 34A. Notice that in addition to the swing limitations imposed by the op amp input common-mode range and output range, the reference high side swing is limited to 2.5V from the positive rail by the REF200's minimum compliance voltage. The low side swing is limited only by the op amp. If the reference voltage is more than about 3V this limitation can be eliminated by adding gain as shown in Figure 34B. In this example, the 1V across the reference setting-registor is amplified to 5V at the output. Since there is always 4V between the output and the op amp inputs, the high-side swing is not limited by the current source compliance or the op amp input common mode range. It is limited only by the op amp out put swing capability.

Where the voltage reference is lower than about 3V, the high side compliance will still be limited by the current source compliance. In these situations, consider the circuit shown in Figure 34C. In this case, the op amp noninverting input is driven while the current source connects to the other op amp input and a voltage setting resistor with its other terminal connected to the output. High-side compliance is limited only by the op amp. Another advantage of this circuit is its high input inpedance. The disavantage is limited low side compliance. Current source compliance limits swing to the negative rail to 2.5V — regardless of the op amp input common mode range.

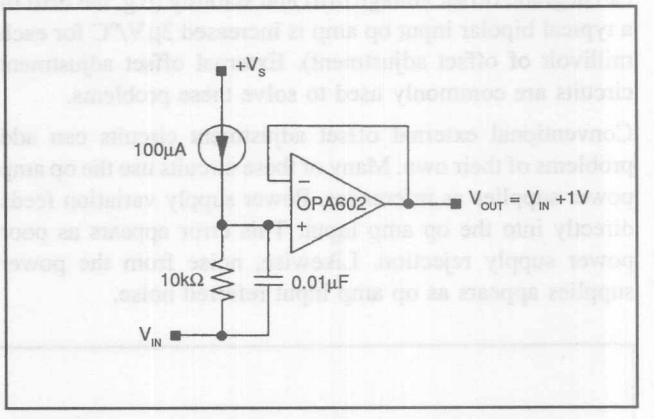

FIGURE 34A. Floating Voltage Reference.

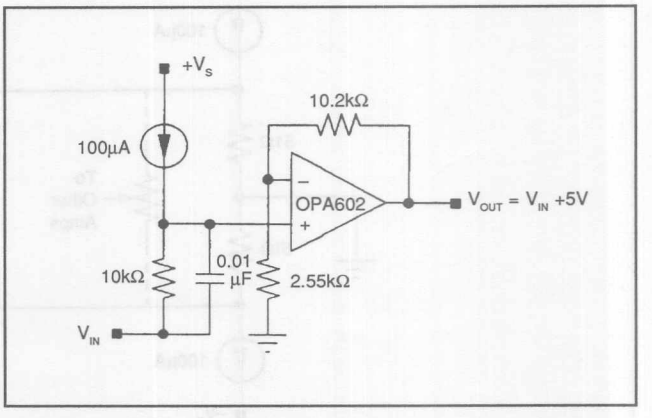

FIGURE 34B. Floating Voltage Reference with high-side compliance limited only by op amp output swing capability.

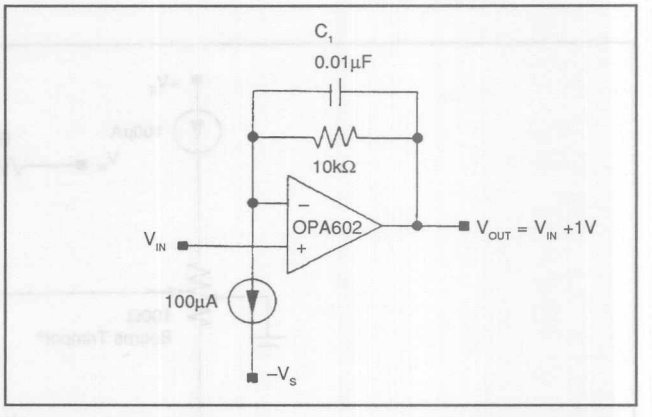

FIGURE 34C. Floating Low Voltage Reference with high impedance input drive and high-side output compliance limited only by op amp output swing capability.

OP AMP OFFSET ADJUSTMENT USING 5mV REFERENCE

Op amp offset adjustment circuits are another application for millivolt level references. Many op amps, especially duals and quads, have no built-in provision for offset adjustment. Even when offset adjustment pins are provided, using them can degrade offset voltage drift and stability (e.g. the drift of a typical bipolar input op amp is increased 3µV/°C for each millivolt of offset adjustment). External offset adjustment circuits are commonly used to solve these problems.

Conventional external offset adjustment circuits can add problems of their own. Many of these circuits use the op amp power supplies as references. Power supply variation feeds directly into the op amp input. This error appears as poor power supply rejection. Likewise, noise from the power supplies appears as op amp input referred noise.

The circuits shown in Figures 35 and 36 solve these problems. REF200 current sources provide regulated ±5mV references for stable offset adjustment. This approach provides a truly precision offset adjustment free from problems associated with power supply variations, noise, and drift.

The circuit shown in Figure 35 uses a pair of 51Ω resistors connected to ground to establish the ±5mV reference. A pot connected across this reference allows a ±5mV offset adjustment range. Additional pots can be connected, but be sure to maintain a parallel resistance >50Ω to get >±5mV range.

The second circuit, Figure 36, uses a special potentiometer manufactured by Bourns. It is especially designed for op amp offset adjustment. It has a tap at the center of the element which can be connected to ground. Using this connection eliminates the 51Ω resistors needed in the first circuit.

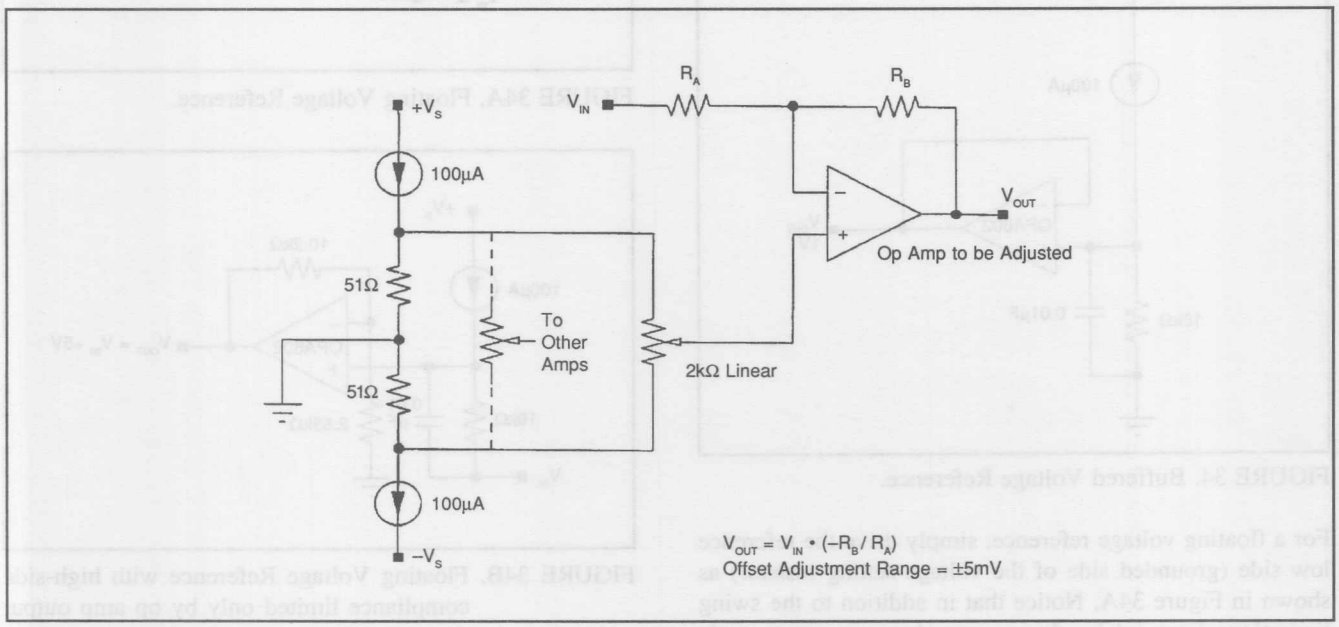

FIGURE 35. Op Amp Offset Adjustment Circuit uses the two 100µA current sources from a REF200 to provide accurate ±5mV references.

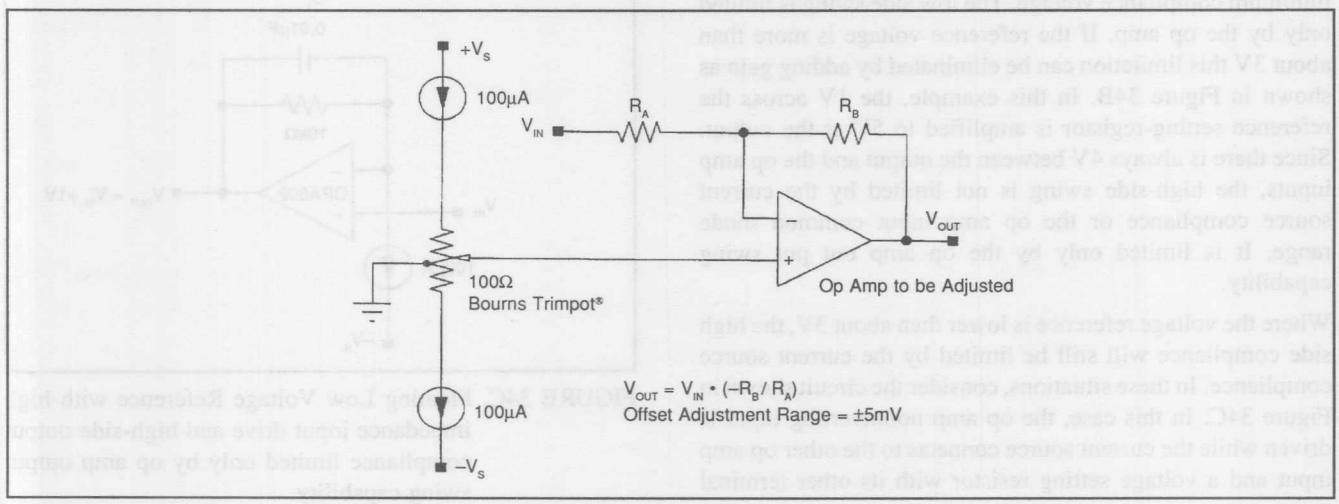

FIGURE 36. Op amp offset adjustment circuit using Bourns Trimpot®.

a floating reference application. Here, a pair of current sources is used to provide a floating bipolar window voltage driven by the V_{CENTER} input. V_O is low when V_I is either above V_{CENTER} + 100µA • R, or below V_{CENTER} – 100µA • R. Otherwise, V_O is high. By using different values for the programming resistors, the threshold can be set asymmetrically around V_{CENTER} if desired.

RTD EXCITATION USING CURRENT REFERENCE

Current sources are often used for excitation of resistor type sensors such as RTDs. If the RTD is located remotely, as it often is, voltage drops in the interconnecting wire can cause in the sense connection, there is no error due to wire resistance.

One problem is that the additional wiring can be very expensive. The three wire circuit shown in Figure 38 saves one wire. 200µA is used for excitation of a 1kΩ RTD, and a matching current from the current mirror is forced in the ground connection. The voltage drops through the two wires cancel thereby eliminating error.

Notice also, that one common wire (shown as a shield) can serve multiple sensors. Each additional RTD only needs one additional pair of wires.

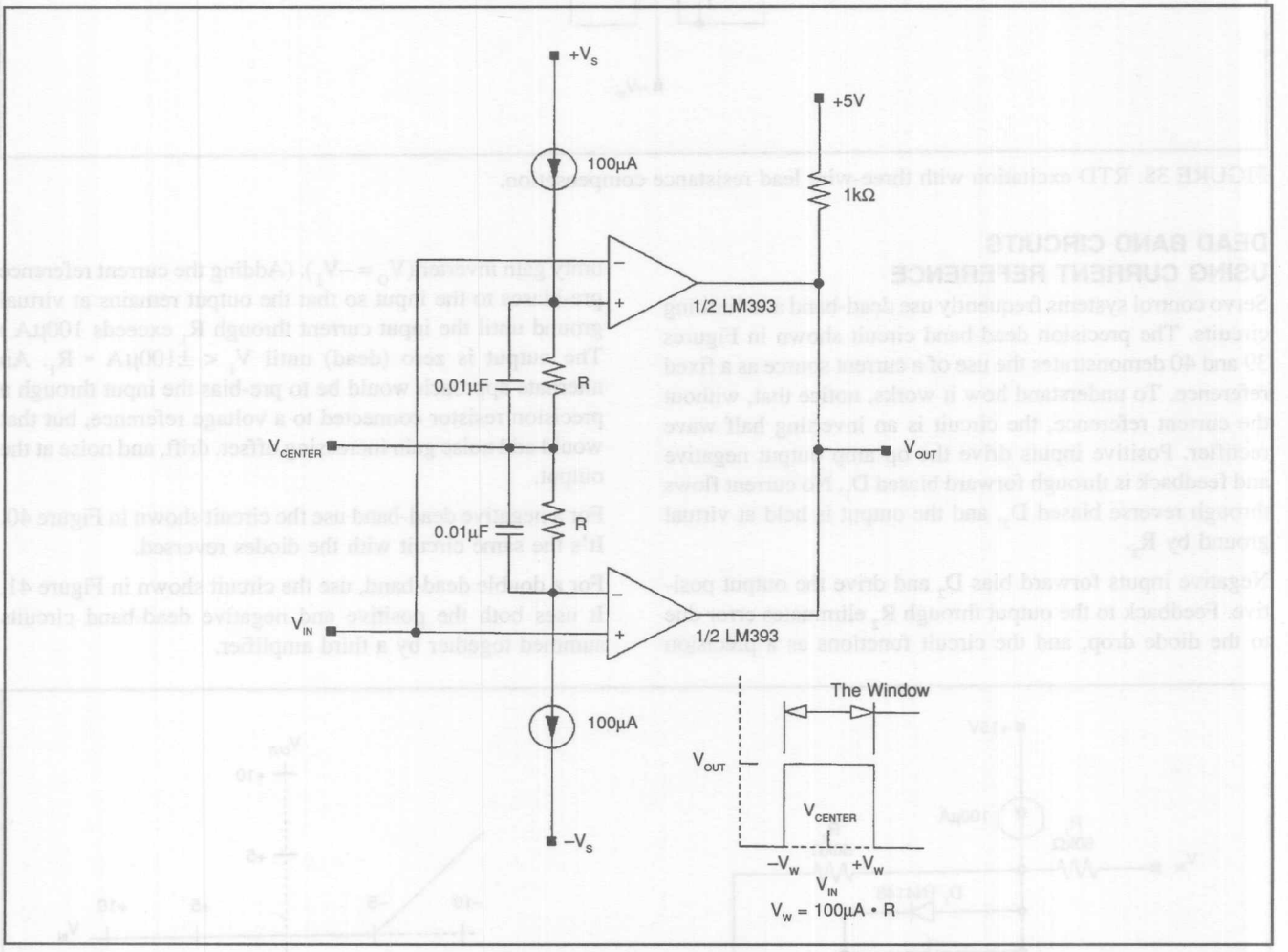

FIGURE 37. Window comparator with voltage programmable window center, and resistor programmable window width.

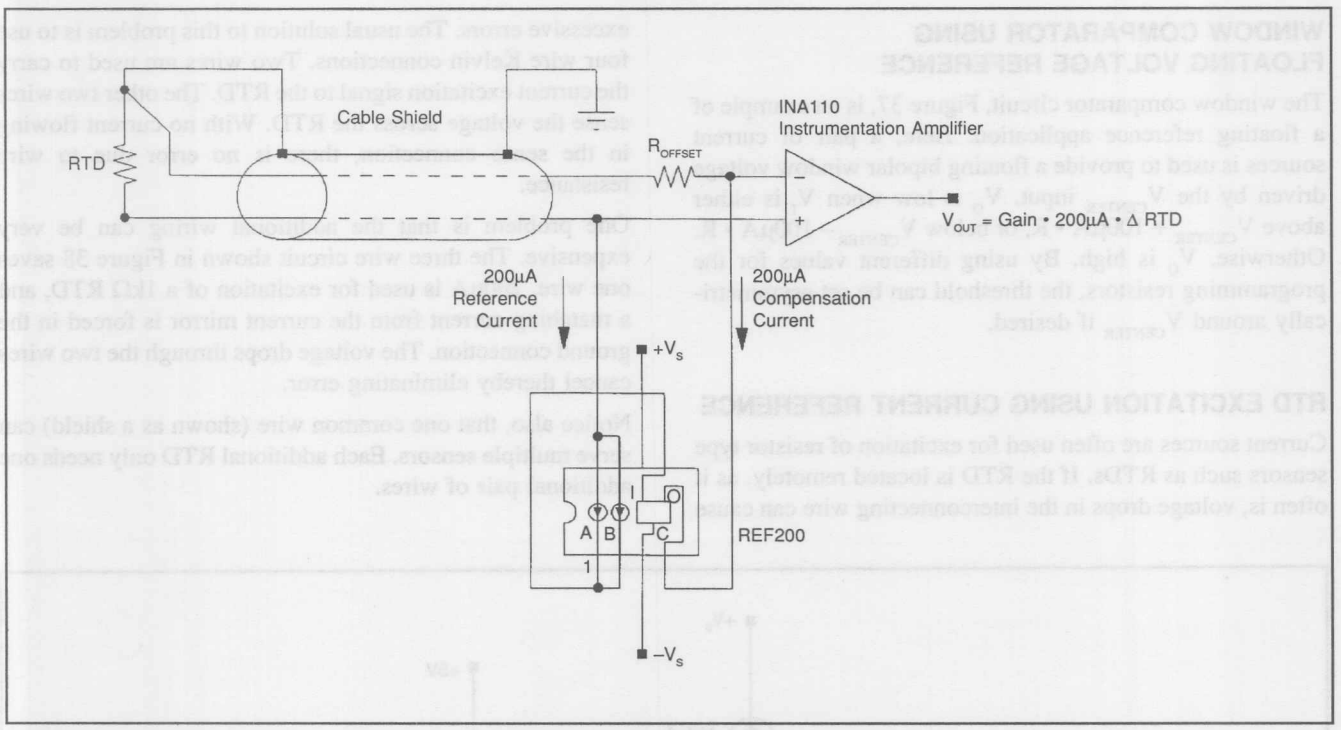

FIGURE 38. RTD excitation with three-wire lead resistance compensation.

DEAD BAND CIRCUITS USING CURRENT REFERENCE

Servo control systems frequently use dead-band and limiting circuits. The precision dead-band circuit shown in Figures 39 and 40 demonstrates the use of a current source as a fixed reference. To understand how it works, notice that, without the current reference, the circuit is an inverting half wave rectifier. Positive inputs drive the op amp output negative and feedback is through forward biased D_1. No current flows through reverse biased D_2, and the output is held at virtual ground by R_2.

Negative inputs forward bias D_2 and drive the output positive. Feedback to the output through R_2 eliminates error due to the diode drop, and the circuit functions as a precision unity gain inverter ($V_O = -V_I$). (Adding the current reference pre-biases to the input so that the output remains at virtual ground until the input current through R_1 exceeds 100µA.) The output is zero (dead) until $V_I < \pm 100\mu A \cdot R_1$. An alternate approach would be to pre-bias the input through a precision resistor connected to a voltage reference, but that would add noise gain increasing offset, drift, and noise at the output.

For a negative dead-band use the circuit shown in Figure 40. It's the same circuit with the diodes reversed.

For a double dead-band, use the circuit shown in Figure 41. It uses both the positive and negative dead-band circuits summed together by a third amplifier.

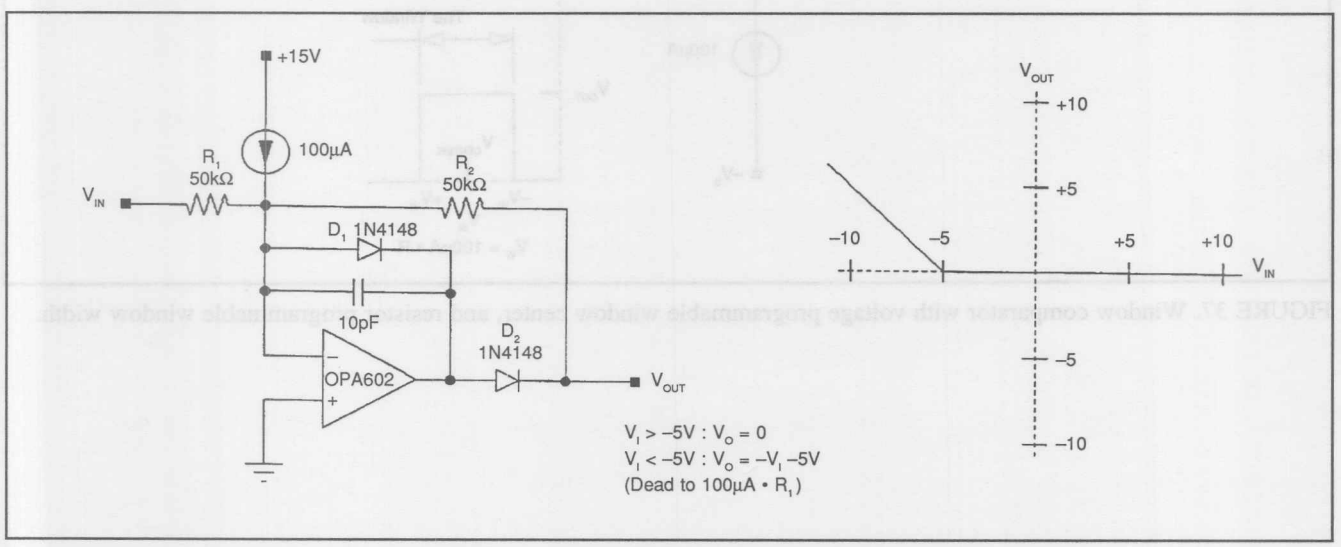

FIGURE 39. Precision positive dead-band circuit.

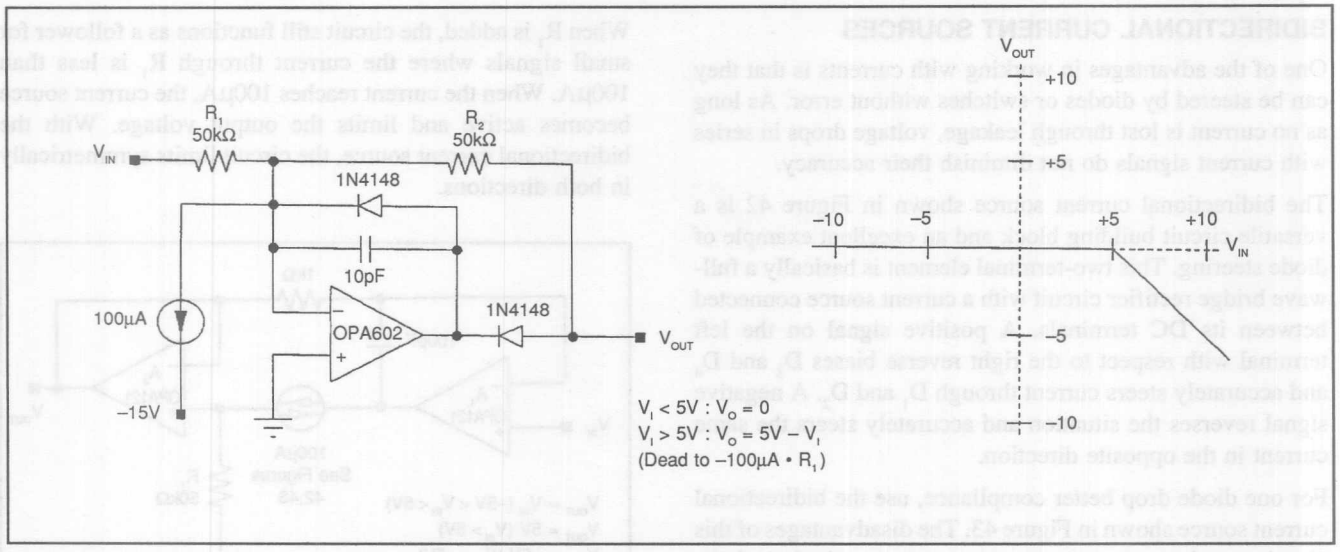

FIGURE 40. Precision negative dead-band circuit.

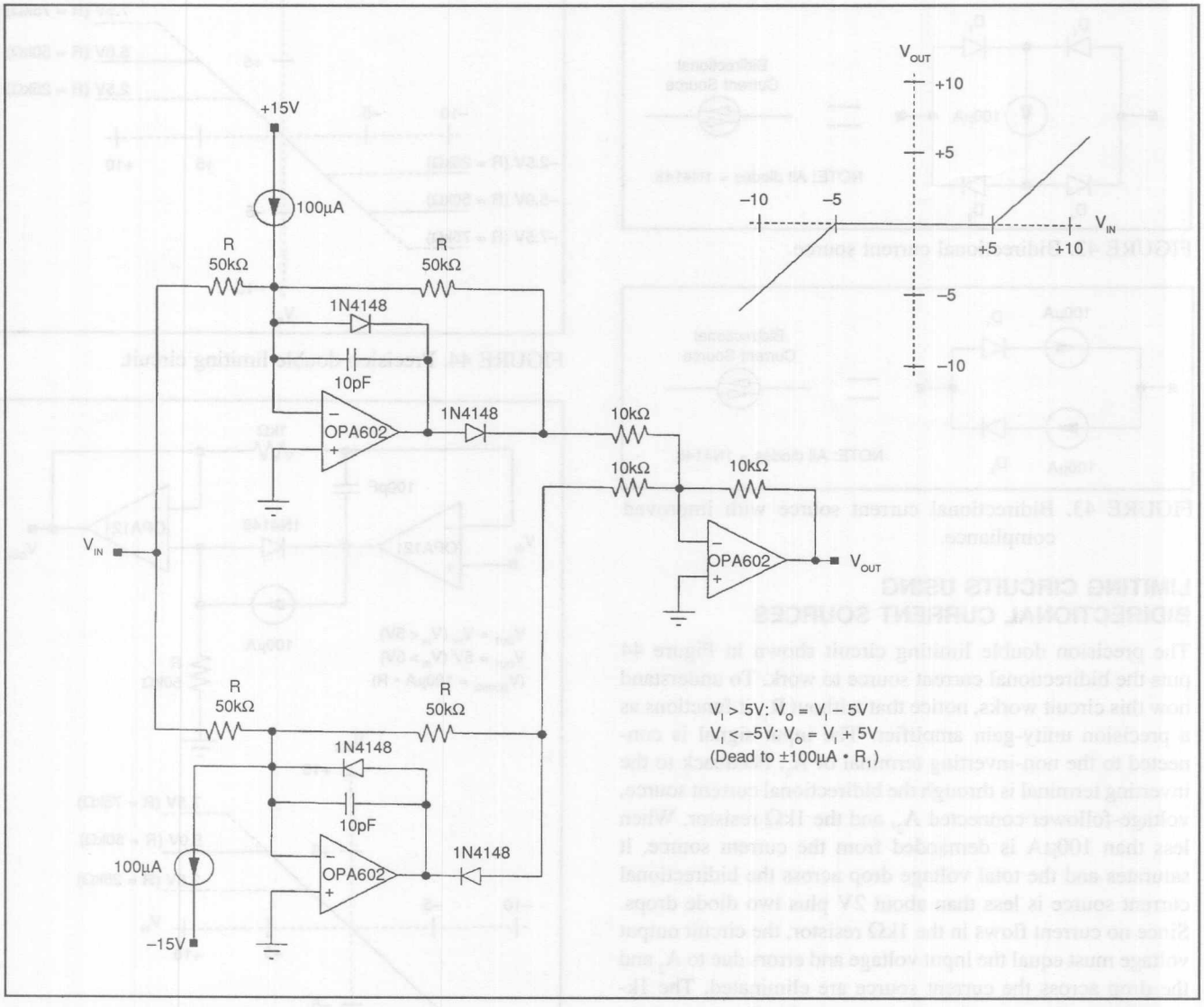

FIGURE 41. Precision double dead-band circuit.

BIDIRECTIONAL CURRENT SOURCES

One of the advantages in working with currents is that they can be steered by diodes or switches without error. As long as no current is lost through leakage, voltage drops in series with current signals do not diminish their accuracy.

The bidirectional current source shown in Figure 42 is a versatile circuit building block and an excellent example of diode steering. This two-terminal element is basically a full-wave bridge rectifier circuit with a current source connected between its DC terminals. A positive signal on the left terminal with respect to the right reverse biases D_3 and D_4 and accurately steers current through D_1 and D_2. A negative signal reverses the situation and accurately steers the same current in the opposite direction.

For one diode drop better compliance, use the bidirectional current source shown in Figure 43. The disadvantages of this circuit are that two current sources are required, and the inherent current matching of the previous circuit is lost.

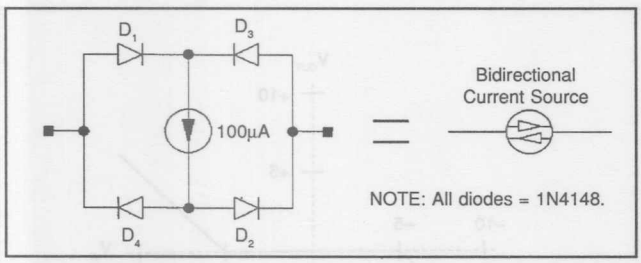

FIGURE 42. Bidirectional current source.

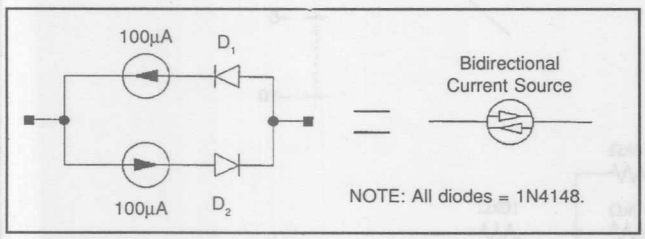

FIGURE 43. Bidirectional current source with improved compliance.

LIMITING CIRCUITS USING BIDIRECTIONAL CURRENT SOURCES

The precision double limiting circuit shown in Figure 44 puts the bidirectional current source to work. To understand how this circuit works, notice that without R_1, it functions as a precision unity-gain amplifier. The input signal is connected to the non-inverting terminal of A_1. Feedback to the inverting terminal is through the bidirectional current source, voltage-follower connected A_2, and the 1kΩ resistor. When less than 100µA is demanded from the current source, it saturates and the total voltage drop across the bidirectional current source is less than about 2V plus two diode drops. Since no current flows in the 1kΩ resistor, the circuit output voltage must equal the input voltage and errors due to A_2 and the drop across the current source are eliminated. The 1k-100pF network provides compensation for the extra phase shift in the feedback loop.

When R_1 is added, the circuit still functions as a follower for small signals where the current through R_1 is less than 100µA. When the current reaches 100µA, the current source becomes active and limits the output voltage. With the bidirectional current source, the circuit limits symmetrically in both directions.

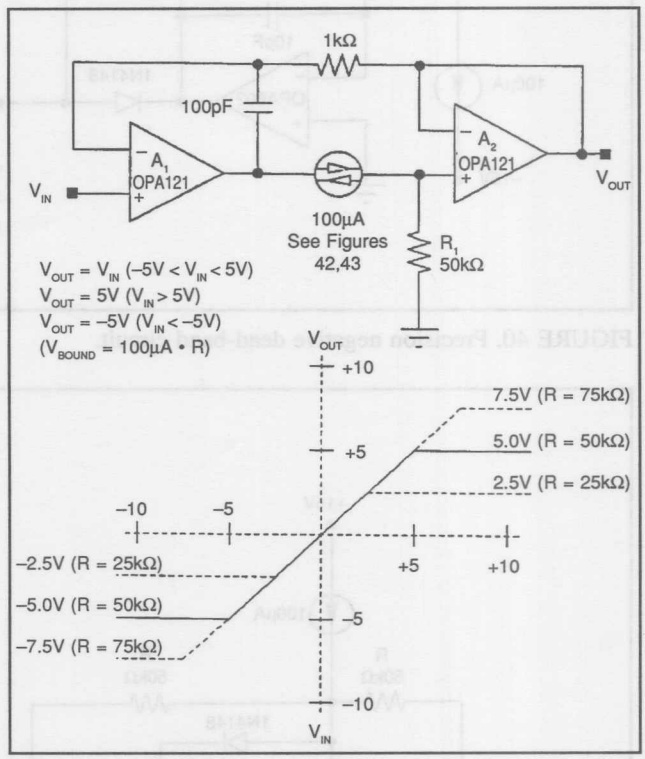

FIGURE 44. Precision double limiting circuit.

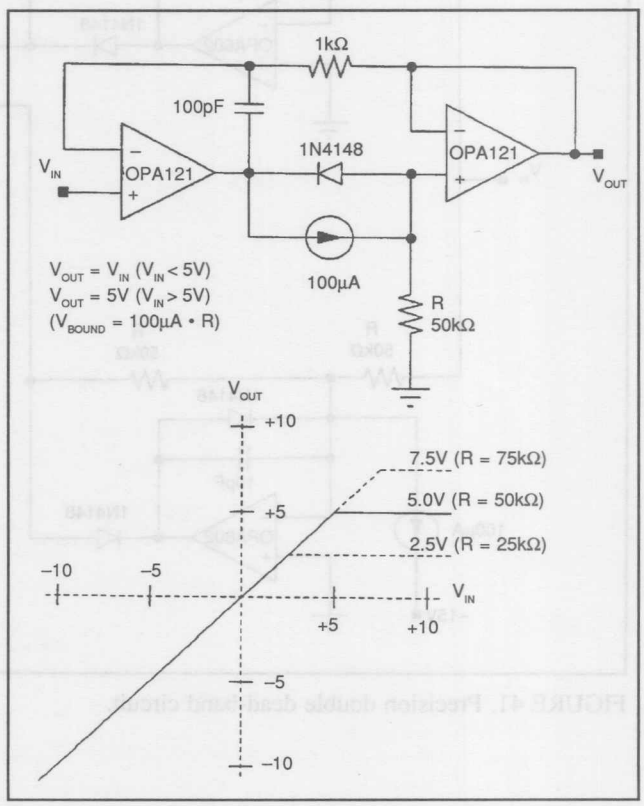

FIGURE 45. Precision limiting circuit.

direction, reverse the polarity of the current source and diode.

PRECISION TRIANGLE WAVEFORM GENERATOR USING BIDIRECTIONAL CURRENT SOURCES

The precision triangle waveform generator shown in Figure 46 makes use of two bidirectional current sources. One steers a precision current signal into the integrating capacitor connected to the inverting input of the op amp. The other steers a precision current into the 10kΩ resistor connected to the positive op amp terminal to provide ±1V hysteresis. The result is a relaxation oscillator with precision triangle and square wave outputs of ±1V.

The precision duty cycle modulator shown in Figure 47 is a variation of the triangle generator. Here the integrating capacitor is replaced by a true integrator formed by A_1 and C. This allows the summation of a ground referenced signal through the 100kΩ input resistor. With no input signal, the output is a square wave with 50% duty cycle. Input signals sum into the integrator through the 100kΩ resistor. The integrator then slews faster in one direction, and slower in the other. The result is a linear duty cycle modulation of the output signal. The modulator is said to be duty cycle rather than pulse width because the output frequency varies somewhat with input signal. For a constant frequency duty cycle modulator add a resistor in series with the inverting input of A_2 and drive that input with a resistor coupled clock signal.

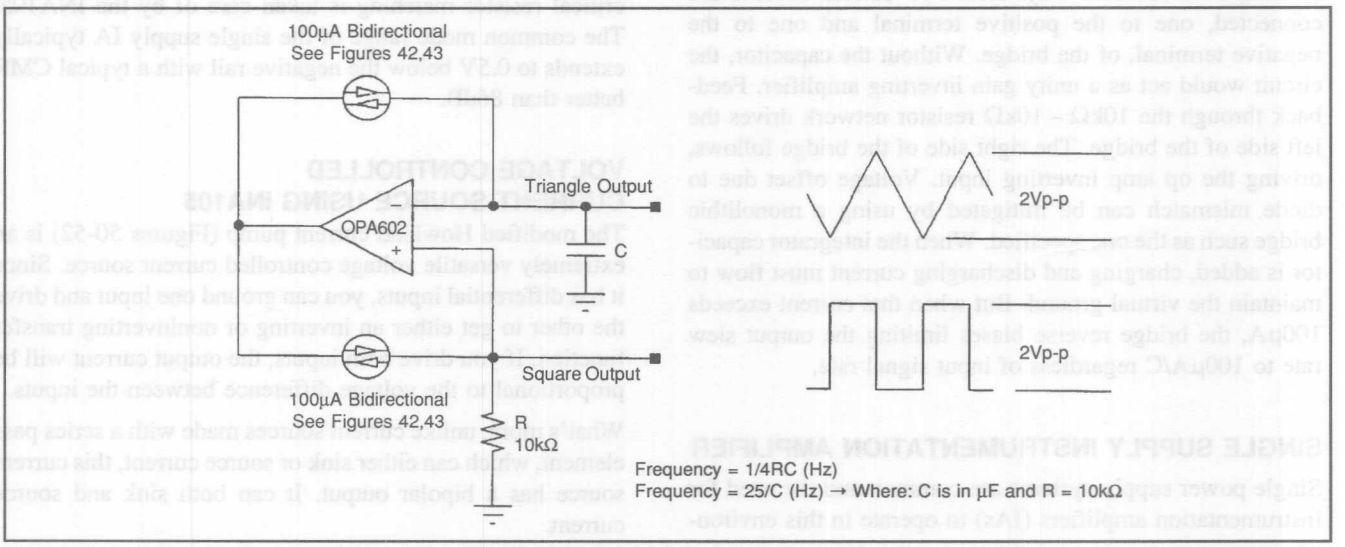

FIGURE 46. Precision triangle waveform generator.

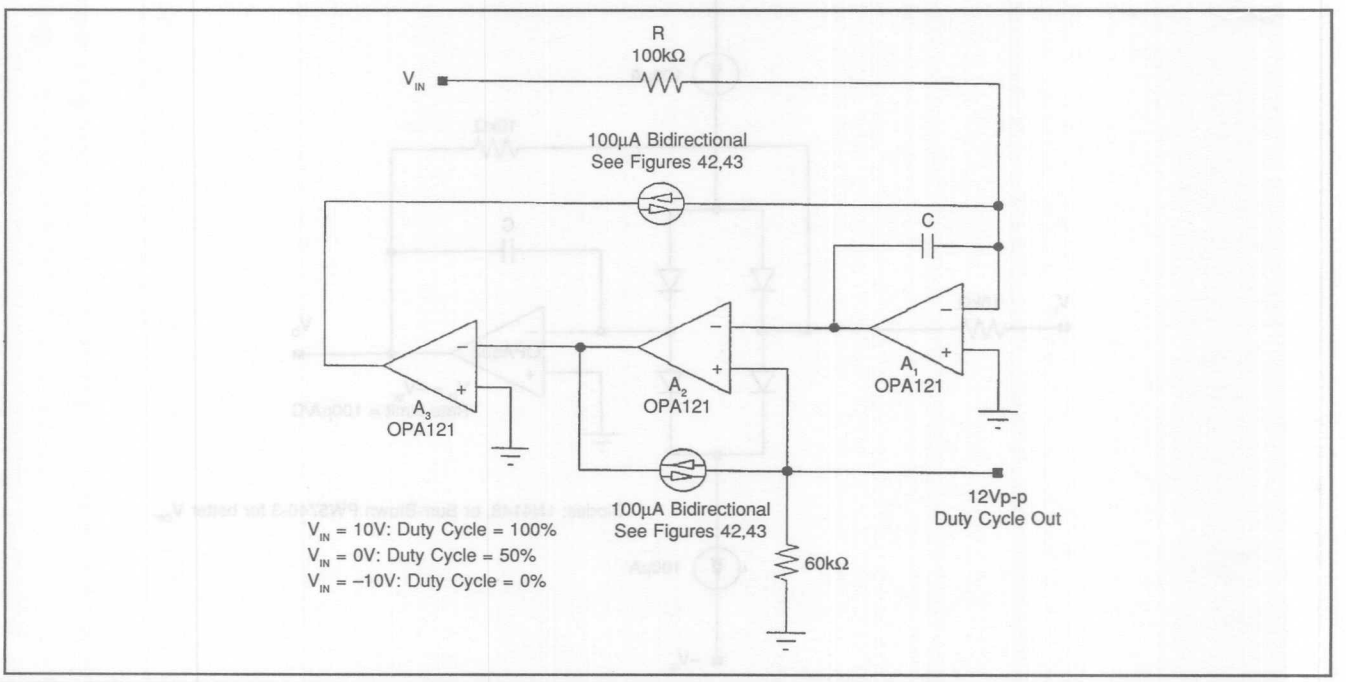

FIGURE 47. Precision duty-cycle modulation circuit.

Notice that the duty-cycle modulator has a true integrating input. This is in contrast to conventional modulators which simply use a comparator connected between the input signal and a precision triangle wave. With the conventional approach, at crossing, input noise feeds through at the comparator bandwidth resulting in jitter. Not only does the integrating input filter out input noise, it can be synchronized to input noise (such as 60Hz), completely notching out its effect. If integration takes place over one or more complete cycles of the noise signal, the undulations of the noise signal are exactly averaged out.

SLEW RATE LIMITER

In some applications, especially when driving inductors, it is necessary to limit the signal slew rate. The rate limiting circuit shown in Figure 48 uses a diode bridge for current steering in a different way. Here two current sources are connected, one to the positive terminal and one to the negative terminal, of the bridge. Without the capacitor, the circuit would act as a unity gain inverting amplifier. Feedback through the 10kΩ – 10kΩ resistor network drives the left side of the bridge. The right side of the bridge follows, driving the op amp inverting input. Voltage offset due to diode mismatch can be mitigated by using a monolithic bridge such as the one specified. When the integrator capacitor is added, charging and discharging current must flow to maintain the virtual ground. But when that current exceeds 100µA, the bridge reverse biases limiting the output slew rate to 100µA/C regardless of input signal rate.

SINGLE SUPPLY INSTRUMENTATION AMPLIFIER

Single power supply systems are common and the need for instrumentation amplifiers (IAs) to operate in this environment is critical. While single supply op amps have been available for many years, single supply IAs have not. What's more, single supply IAs can not be made by simply using single supply op amps in the traditional manner. In a conventional IA topology the outputs as well as the inputs would need to swing to the negative rail. Although some op amps come close, no amplifier output can swing all the way to its power supply rail, especially when driving a load.

The single supply IA circuit shown in Figure 49 solves this problem by simply level shifting the input signal up by a Vbe with a matched pair of matched PNP input transistors. The transistors are biased as emitter followers by the 100µA current sources in a REF200. The ensuing circuit is a traditional three op amp IA. OPA1013s are used for input amplifiers because they are designed for single supply operation and their output can also swing near the negative rail. The Burr-Brown INA105 is used as a difference amplifier. All critical resistor matching is taken care of by the INA105. The common mode range of the single supply IA typically extends to 0.5V below the negative rail with a typical CMR better than 86dB.

VOLTAGE CONTROLLED CURRENT SOURCE USING INA105

The modified Howland current pump (Figures 50-52) is an extremely versatile voltage controlled current source. Since it has differential inputs, you can ground one input and drive the other to get either an inverting or noninverting transfer function. If you drive both inputs, the output current will be proportional to the voltage difference between the inputs.

What's more, unlike current sources made with a series pass element, which can either sink or source current, this current source has a bipolar output. It can both sink and source current.

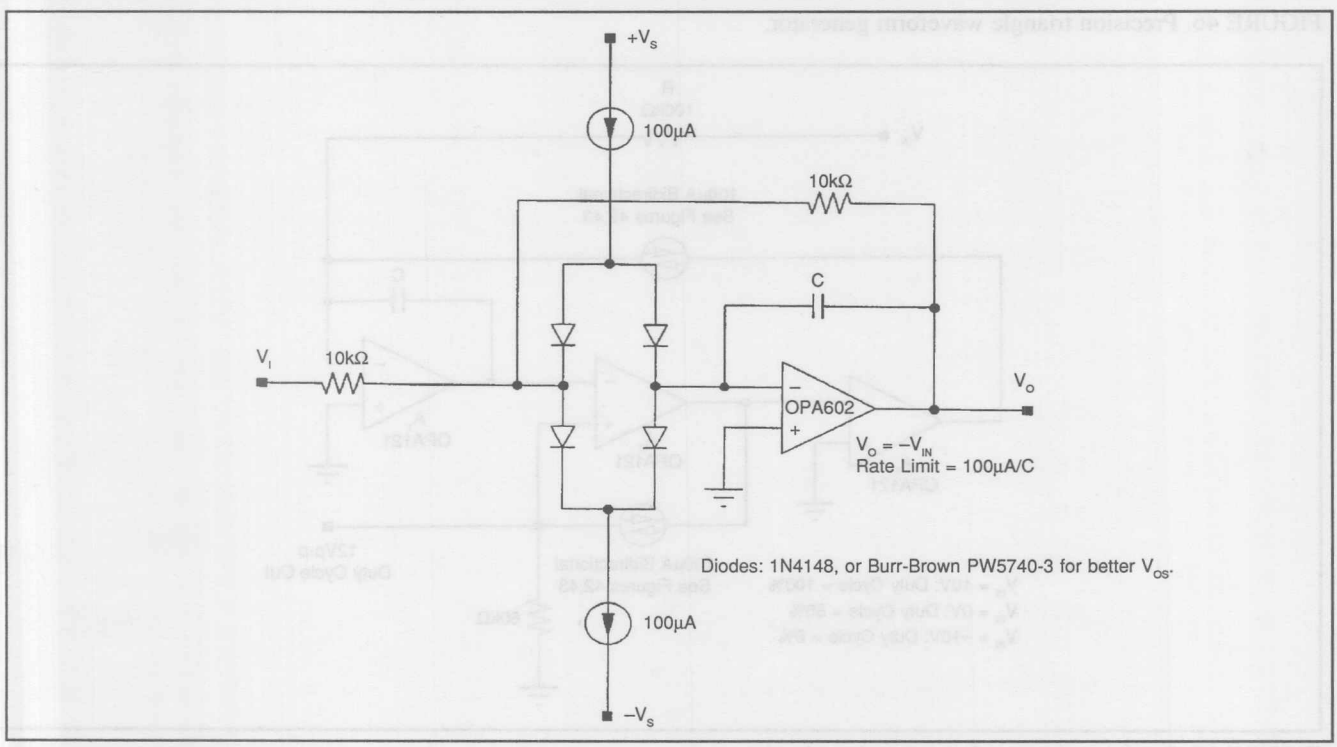

FIGURE 48. Rate limiting circuit.

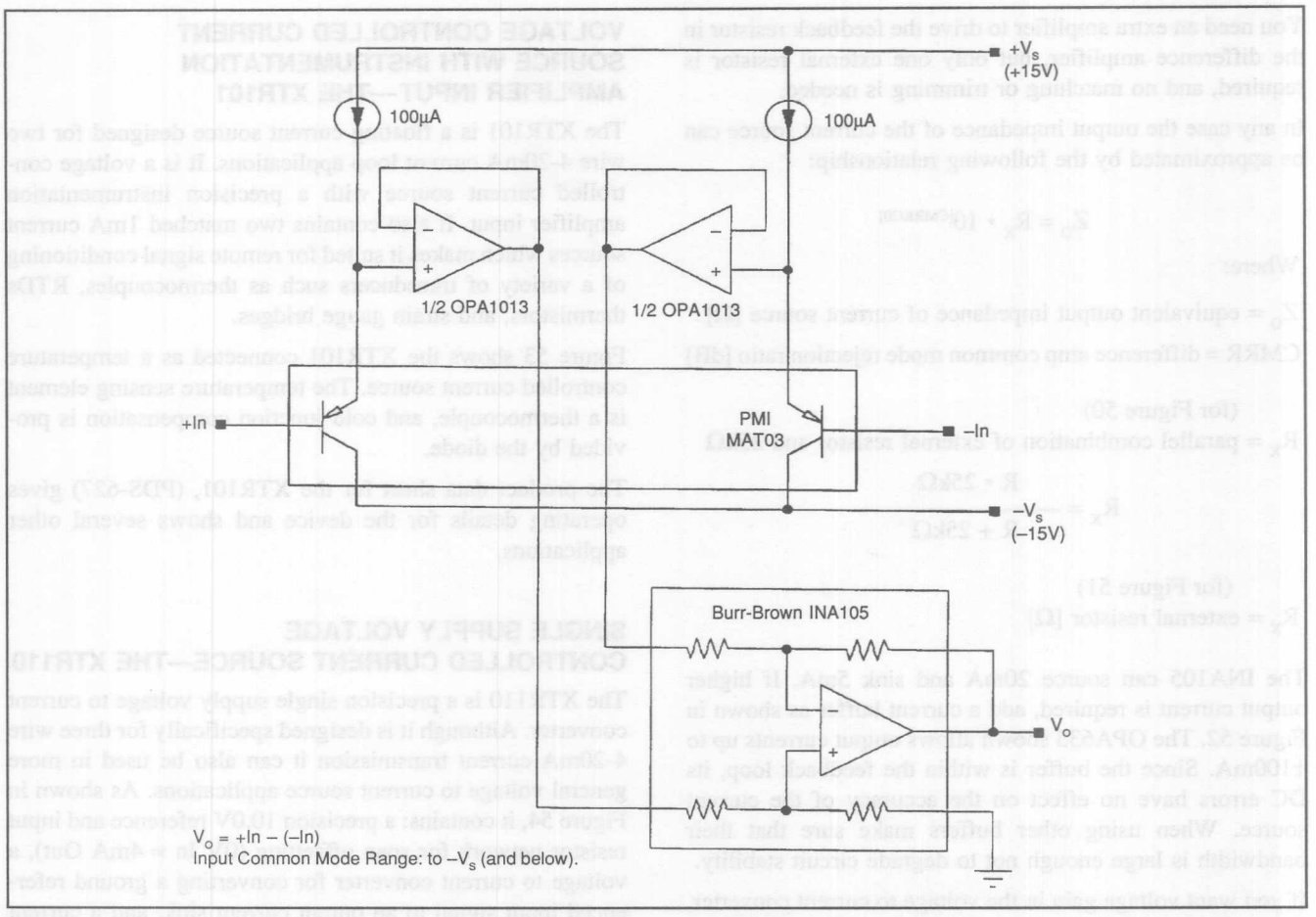

FIGURE 49. Single-supply instrumentation amplifier.

Use of this circuit was limited in the past due to the critical resistor matching and resistor TCR tracking requirements. By using the INA105 difference amplifier, the circuit can be easily implemented with the addition of two 1% resistors. Matching of the external resistors is important, but since they add to the internal 25kΩ resistors, the matching requirement is divided down by the ratio of resistance.

Output impedance of the current source is proportional to the common mode rejection (CMR) of the difference amplifier. Mismatch of feedback resistors in the difference amplifier caused by the external resistors will degrade CMR and lower the current source output impedance. Resistor match of 0.002% is required for 100dB CMR in a unity gain difference amplifier. Depending on the value of the external resistor and output impedance requirement, it may be necessary to trim the external resistor.

When the value of the external resister becomes large consider the alternate circuit shown in Figure. 51.

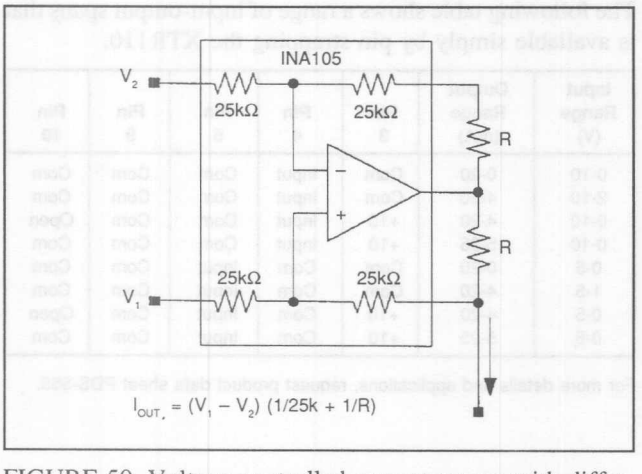

FIGURE 50. Voltage-controlled current source with differential inputs and bipolar output.

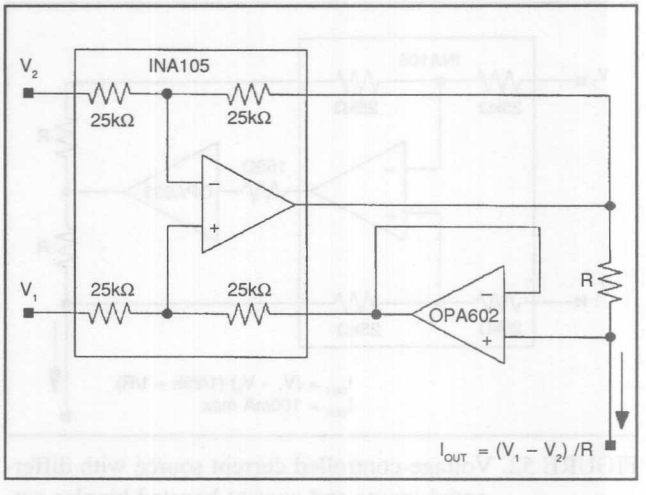

FIGURE 51. Voltage-controlled current source with differential inputs and bipolar output and circuit to eliminate feedback resistor error.

You need an extra amplifier to drive the feedback resistor in the difference amplifier, but only one external resistor is required, and no matching or trimming is needed.

In any case the output impedance of the current source can be approximated by the following relationship:

$$Z_O = R_X \bullet 10^{[CMRR/20]}$$

Where:

Z_O = equivalent output impedance of current source [Ω]

CMRR = difference amp common mode rejection ratio [dB]

(for Figure 50)

R_X = parallel combination of external resistor and 25kΩ

$$R_X = \frac{R \bullet 25k\Omega}{R + 25k\Omega}$$

(for Figure 51)

R_X = external resistor [Ω]

The INA105 can source 20mA and sink 5mA. If higher output current is required, add a current buffer as shown in Figure 52. The OPA633 shown allows output currents up to ±100mA. Since the buffer is within the feedback loop, its DC errors have no effect on the accuracy of the current source. When using other buffers make sure that their bandwidth is large enough not to degrade circuit stability.

If you want voltage gain in the voltage to current converter, use the INA106 for a gain-of-ten difference amplifier.

Don't forget that source impedance adds directly to the input resistors of the difference amplifier which can degrade its performance. A source impedance mismatch of 5Ω will degrade the CMRR of the INA105 to 80dB. If you are driving the circuit from an amplifier or other low impedance source, this should not be a problem. If you have higher source impedances, buffer the driven input(s) of the difference amplifier, or use an instrumentation amplifier such as the INA110 instead of a difference amplifier.

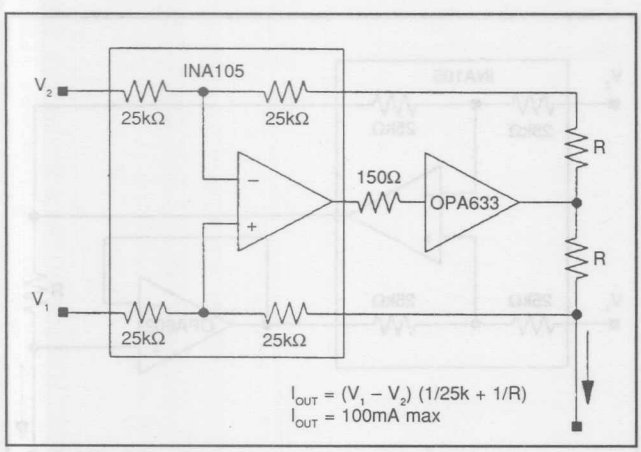

FIGURE 52. Voltage-controlled current source with differential inputs and current boosted bipolar output.

VOLTAGE CONTROLLED CURRENT SOURCE WITH INSTRUMENTATION AMPLIFIER INPUT—THE XTR101

The XTR101 is a floating current source designed for two wire 4-20mA current loop applications. It is a voltage controlled current source with a precision instrumentation amplifier input. It also contains two matched 1mA current sources which makes it suited for remote signal conditioning of a variety of transducers such as thermocouples, RTDs thermistors, and strain gauge bridges.

Figure 53 shows the XTR101 connected as a temperature controlled current source. The temperature sensing element is a thermocouple, and cold junction compensation is provided by the diode.

The product data sheet for the XTR101, (PDS-627) gives operating details for the device and shows several other applications.

SINGLE SUPPLY VOLTAGE CONTROLLED CURRENT SOURCE—THE XTR110

The XTR110 is a precision single supply voltage to current converter. Although it is designed specifically for three wire 4-20mA current transmission it can also be used in more general voltage to current source applications. As shown in Figure 54, it contains: a precision 10.0V reference and input resistor network for span offsetting (0V In = 4mA Out), a voltage to current converter for converting a ground referenced input signal to an output current sink, and a current mirror for turning the output of the current sink into a current source.

The current mirror has a gain ratio of 10:1 and uses an external pass transistor to minimize internal thermal feedback and improve accuracy. Since the mirror transistor is external, an external mirror ratio setting resistor can be added for an arbitrarily high output current.

Both the voltage to current converter, and the current mirror use single supply op amps so that the input and output signals can go to zero. In the case of the mirror op amp, the common mode range goes to the positive power supply rail rather than common.

The following table shows a range of input-output spans that is available simply by pin strapping the XTR110.

Input Range (V)	Output Range (mA)	Pin 3	Pin 4	Pin 5	Pin 9	Pin 10
0-10	0-20	Com	Input	Com	Com	Com
2-10	4-20	Com	Input	Com	Com	Com
0-10	4-20	+10	Input	Com	Com	Open
0-10	5-25	+10	Input	Com	Com	Com
0-5	0-20	Com	Com	Input	Com	Com
1-5	4-20	Com	Com	Input	Com	Com
0-5	4-20	+10	Com	Input	Com	Open
0-5	5-25	+10	Com	Input	Com	Com

For more details and applications, request product data sheet PDS-555.

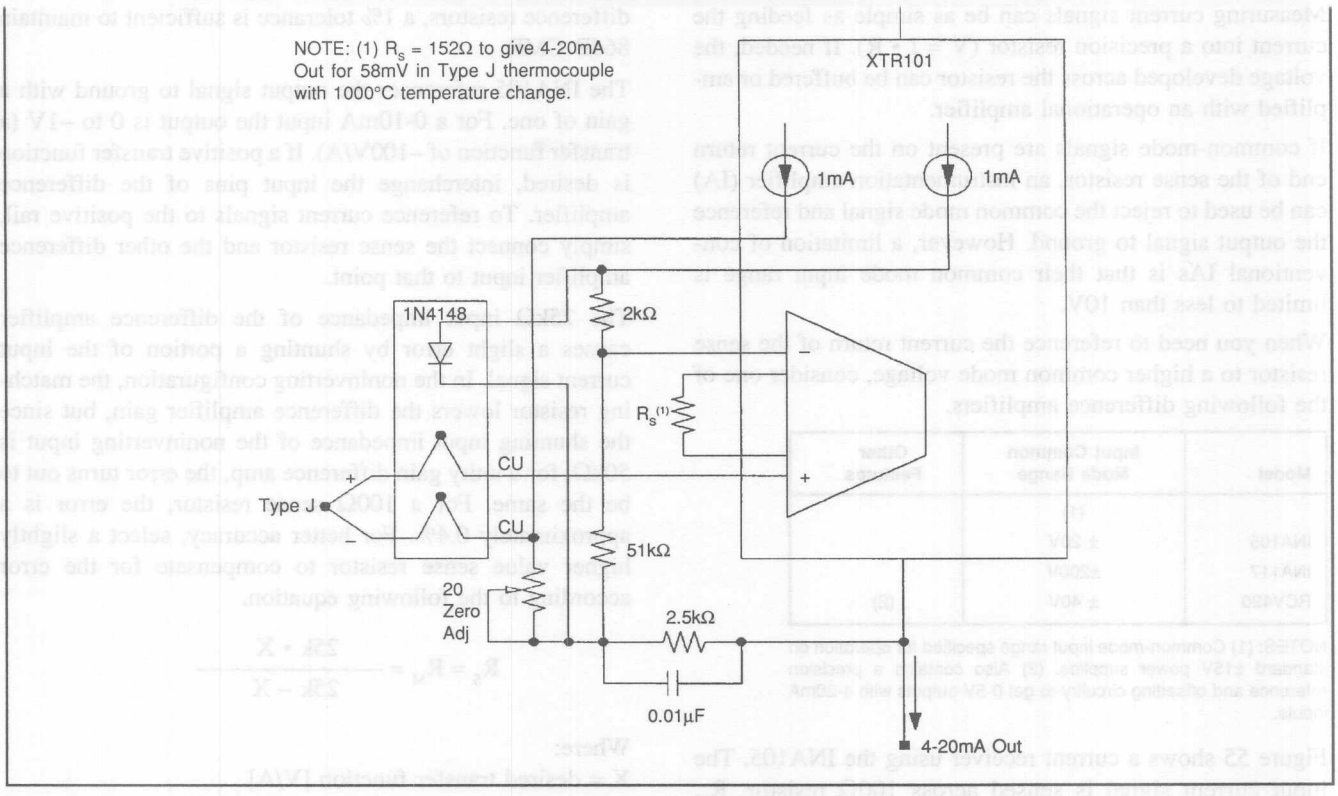

FIGURE 53. Temperature-controlled current source using XTR101.

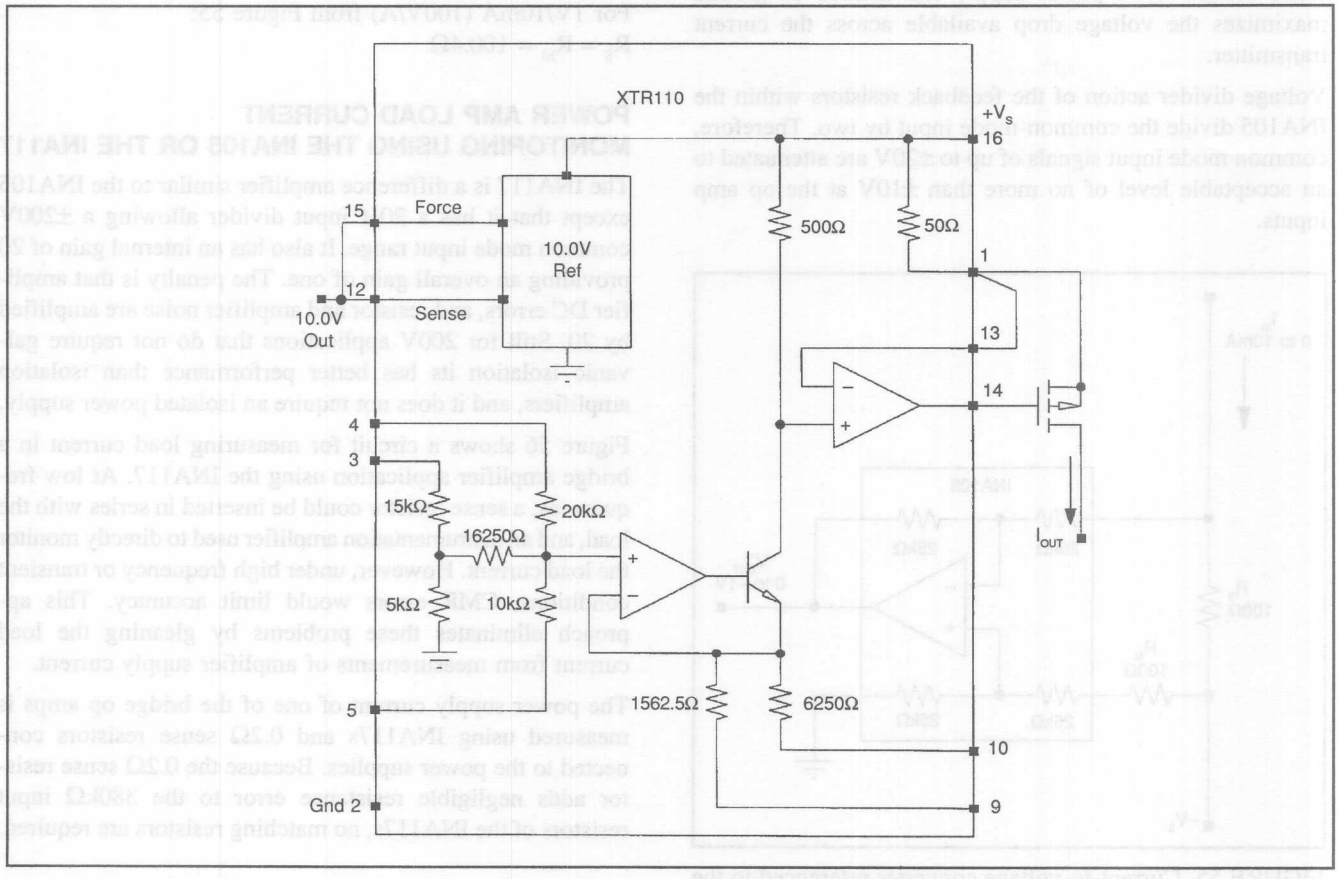

FIGURE 54. Precision single-supply voltage-to-current source transmitter—the XTR110.

CURRENT RECEIVER WITH COMPLIANCE TO BOTH POWER SUPPLY RAILS USING THE INA105

Measuring current signals can be as simple as feeding the current into a precision resistor (V = I • R). If needed, the voltage developed across the resistor can be buffered or amplified with an operational amplifier.

If common-mode signals are present on the current return end of the sense resistor, an instrumentation amplifier (IA) can be used to reject the common mode signal and reference the output signal to ground. However, a limitation of conventional IAs is that their common mode input range is limited to less than 10V.

When you need to reference the current return of the sense resistor to a higher common mode voltage, consider one of the following difference amplifiers.

Model	Input Common Mode Range	Other Features
	(1)	
INA105	± 20V	
INA117	±200V	
RCV420	± 40V	(2)

NOTES: (1) Common-mode input range specified for operation on standard ±15V power supplies. (2) Also contains a precision reference and offsetting circuitry to get 0-5V outputs with 4-20mA inputs.

Figure 55 shows a current receiver using the INA105. The input current signal is sensed across 100Ω resistor, R_S, connected to the negative power supply rail. Connecting the sense resistor to a power supply rail instead of ground maximizes the voltage drop available across the current transmitter.

Voltage divider action of the feedback resistors within the INA105 divide the common-mode input by two. Therefore, common mode input signals of up to ±20V are attenuated to an acceptable level of no more than ±10V at the op amp inputs.

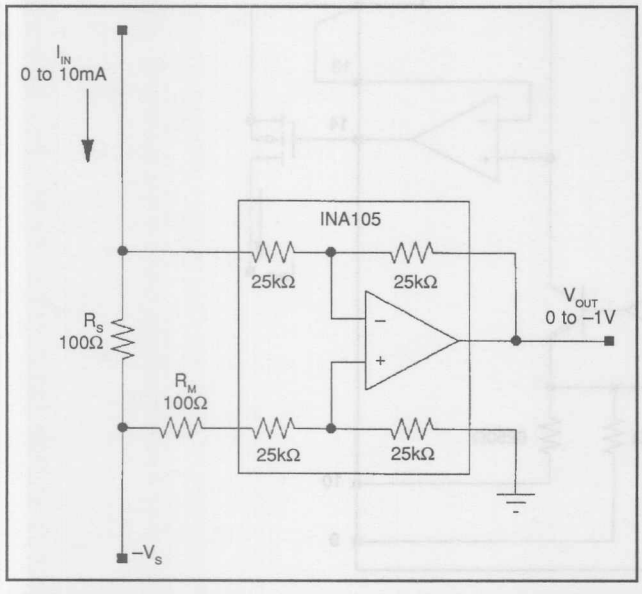

FIGURE 55. Current-to-voltage converter referenced to the negative power supply rail.

Matching resistor, R_M, preserves the resistance match of the INA105 and maintains its high common-mode rejection (CMR). Because 100Ω is small compared to the 25kΩ difference resistors, a 1% tolerance is sufficient to maintain 86dB CMR.

The INA105 references the output signal to ground with a gain of one. For a 0-10mA input the output is 0 to –1V (a transfer function of –100V/A). If a positive transfer function is desired, interchange the input pins of the difference amplifier. To reference current signals to the positive rail, simply connect the sense resistor and the other difference amplifier input to that point.

The 25kΩ input impedance of the difference amplifier causes a slight error by shunting a portion of the input current signal. In the noninverting configuration, the matching resistor lowers the difference amplifier gain, but since the shunting input impedance of the noninverting input is 50kΩ, for a unity gain difference amp, the error turns out to be the same. For a 100Ω sense resistor, the error is a approximately 0.4%. For better accuracy, select a slightly higher value sense resistor to compensate for the error according to the following equation.

$$R_S = R_M = \frac{25k \bullet X}{25k - X}$$

Where:
X = desired transfer function [V/A]

For example:
For 1V/10mA (100V/A) from Figure 55:
$R_S = R_M = 100.4\Omega$

POWER AMP LOAD CURRENT MONITORING USING THE INA105 OR THE INA117

The INA117 is a difference amplifier similar to the INA105 except that it has a 20/1 input divider allowing a ±200V common mode input range. It also has an internal gain of 20 providing an overall gain of one. The penalty is that amplifier DC errors, and resistor and amplifier noise are amplified by 20. Still for 200V applications that do not require galvanic isolation its has better performance than isolation amplifiers, and it does not require an isolated power supply.

Figure 56 shows a circuit for measuring load current in a bridge amplifier application using the INA117. At low frequencies, a sense resistor could be inserted in series with the load, and an instrumentation amplifier used to directly monitor the load current. However, under high frequency or transient conditions, CMR errors would limit accuracy. This approach eliminates these problems by gleaning the load current from measurements of amplifier supply current.

The power supply current of one of the bridge op amps is measured using INA117s and 0.2Ω sense resistors connected to the power supplies. Because the 0.2Ω sense resistor adds negligible resistance error to the 380kΩ input resistors of the INA117s, no matching resistors are required.

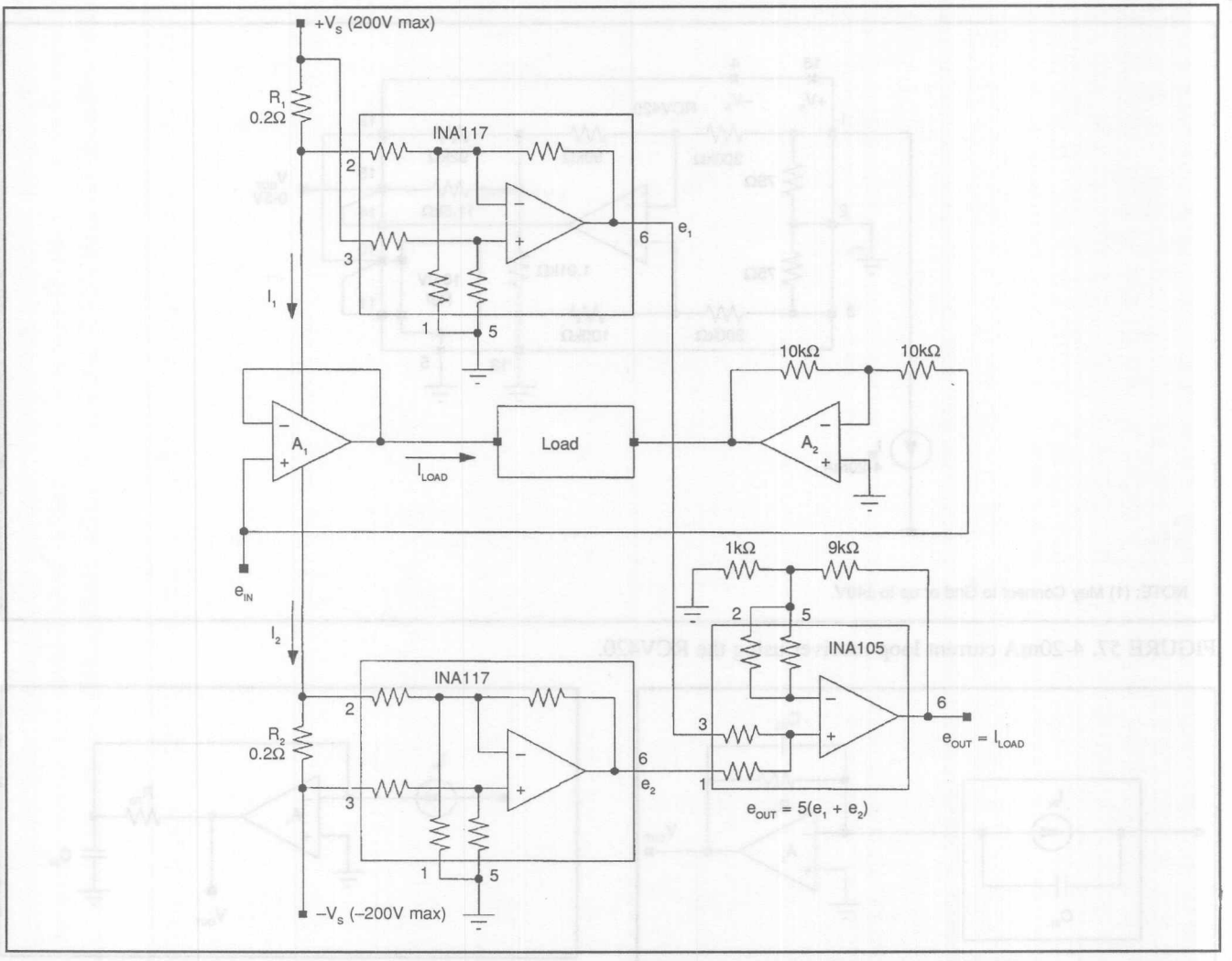

FIGURE 56. Bridge amplifier load current monitor using the INA117.

To understand how the circuit works, notice that since no current flows into the inputs of A_1:

$$I_{LOAD} = I_1 - I_2$$

If

$$R_1 = R_2 = R$$

Then

$$e_1 = I_1 \cdot R,$$

$$e_2 = -I_2 \cdot R,$$

and

$$e_1 + e_2 = I_{LOAD} \cdot R$$

The INA105 is connected as a noninverting summing amplifier with a gain of 5 (the accurate matching of the two 25kΩ input resistors makes a very accurate summing amplifier).

Then

$$e_O = 5(e_1 + e_2) = 5(I_{LOAD} \cdot R),$$

since

$$R = 0.2\Omega,$$

$$e_O = I_{LOAD}\ [1V/A]$$

4 to 20mA CURRENT LOOP RECEIVER WITH 0 to 5V OUTPUT USES THE RCV420

The RCV420 is a current-to-voltage converter designed specifically for conversion of 4-20mA input currents into 0-5V outputs. A pair of precision 75Ω sense resistors are provided internally allowing both inverting and noninverting transfer functions. Input common mode signals up to ±40V can be accommodated due to the internal 4/1 input attenuator. Also, the precision 10.0V reference used for span offseting is available to the user.

Figure 57 shows a typical application. For more details and applications, request product data sheet PDS-837.

VIRTUAL GROUND CURRENT-TO-VOLTAGE CONVERTER

When current-to-voltage conversion with no voltage burden is needed, use the transimpedance amplifier Figures 58—61. In this circuit, an op amp drives the current input node to virtual ground by forcing a current equal to I_{IN} through the feedback resistor, R_{FB}. Notice that the transfer function is inverted:

$$V_{OUT} = -I_{IN} \cdot R_{FB}$$

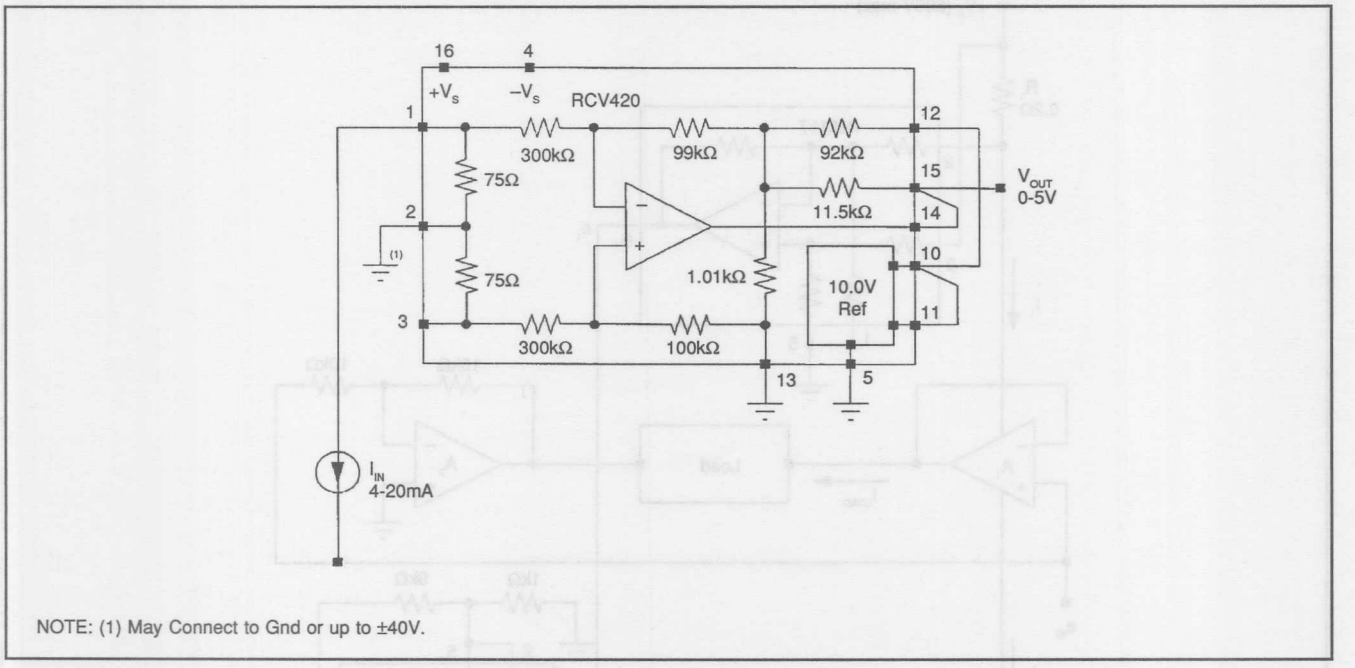

FIGURE 57. 4-20mA current loop receiver using the RCV420.

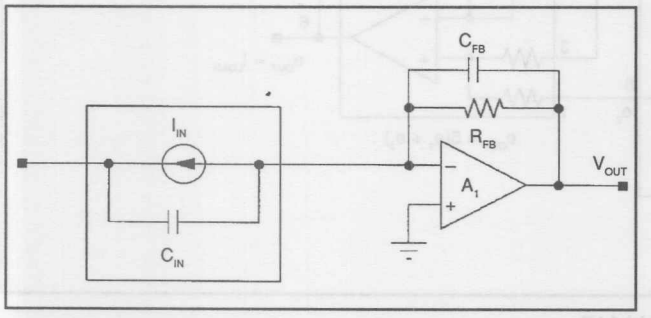

FIGURE 58. Virtual ground current-to-voltage converter.

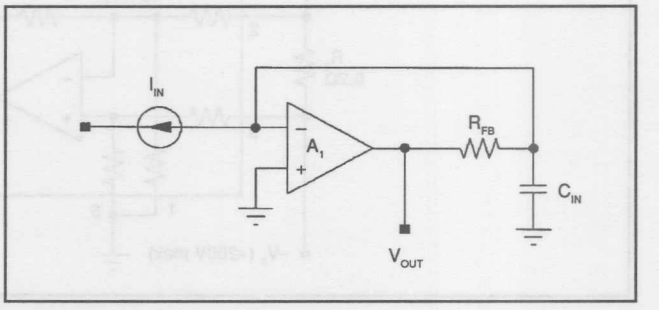

FIGURE 59. Virtual ground current-to-voltage converter redrawn to Illustrate phase delay due to input capacitance and feedback resistor.

The feedback capacitor, C_{FB}, may be needed for circuit stability. To see why, consider the redrawn circuit, Figure 59. C_{IN} represents the input capacitance of the circuit and includes input source capacitance, and op amp input capacitance. Notice that R_{FB} and C_{IN} form a single pole filter in the feedback path to the op amp input. Phase delay through this circuit subtracts from the op amp phase margin which may result in instability, especially with the large values of R_{FB} often used in these circuits. If $C_{FB} \geq C_{IN}$, the phase delay will be less than 20° assuring stability with most unity-gain-stable amplifiers.

PHOTODIODE AMPLIFIER USING VIRTUAL GROUND I/V CONVERTER

The photodiode amplifier shown in Figure 60 is a common application of the transimpedance (current-to-voltage) amplifier. In this application, the shunt capacitance of the photodiode reacting with the relatively large feedback resistor creates excess noise gain. The 1pF feedback capacitor minimizes the peaking and improves stability as discussed previously. Capacitors with the small values often required may be difficult to obtain. By using a capacitor divider circuit shown in Figure 60A, a larger value capacitor can be used. In this example, the 10pF capacitor, C_1, is reduced to an effective value of 1pF by the R_4, R_5 10/1 divider. The 100pF capacitor, C_3, keeps the impedance of the divider low beyond the C_1, $R_4 \parallel R_5$ zero to maintain C_1's effect. It also produces a second-order (40dB/decade) roll-off approximately one decade beyond the $C_1/10$, R_2 pole.

The addition of two passive components to the standard configuration as shown in Figure 61 introduces a second pole that significantly reduces noise. The modification also has other advantages.

The added pole of the improved circuit is formed with R_3 and C_2. Because the pole is placed within the feedback loop, the amplifier maintains its low output impedance. If the pole were placed outside the feedback loop, an additional buffer would be required. The extra buffer would add additional noise and DC error.

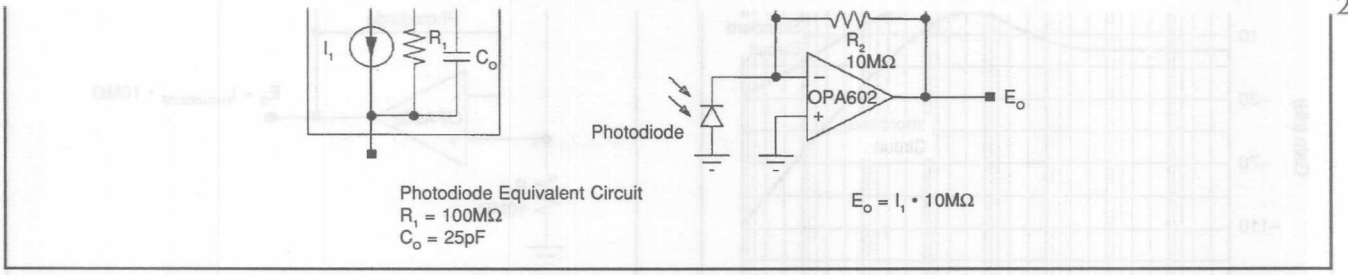

FIGURE 60. Standard transimpedance photodiode amplifier.

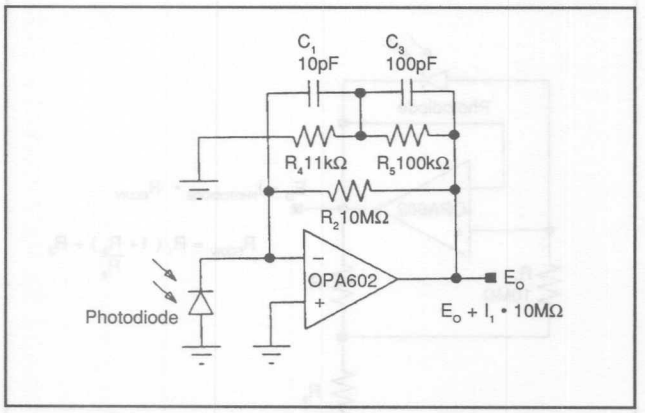

FIGURE 60A. Standard Transimpedance Amplifier with capacitor divider and added feedback pole.

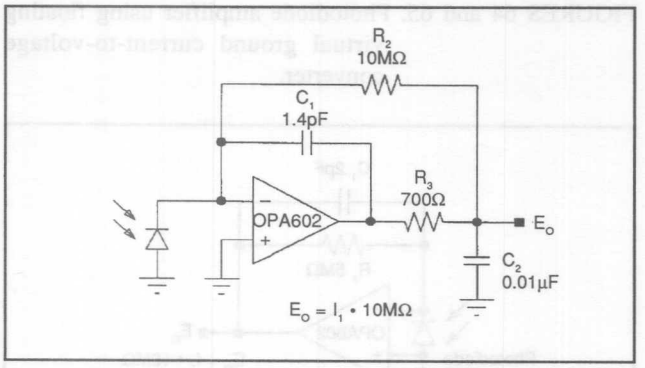

FIGURE 61. Improved transimpedance photodiode amplifier.

The signal bandwidth of both circuits is 16kHz:

$$f_{-3dB} = \frac{1}{2 \cdot \pi \cdot R_2 \cdot C_1}\ [Hz] \rightarrow \text{standard circuit}$$

$$f_{-3dB} = \frac{1}{2 \cdot \pi \cdot (R_2 \cdot C_1 \cdot R_3 \cdot C_2)^{1/2}}\ [Hz] \rightarrow \text{improved circuit}$$

Where, for the improved circuit:
$C_1 \cdot R_2 = 2(C_2 \cdot R_3)$
and $R_2 >> R_3$

In the standard circuit, a single 16kHz pole is formed by the 1pF capacitance in the feedback loop. The improved circuit exhibits two pole response. With $C_1 \cdot R_2 = 2 \cdot C_2 \cdot R_3$, the transfer function is two pole Butterworth (maximally flat in the passband). Figure 62 shows the transimpedance frequency response of the two circuits. At DC, the gain is 140dB or 10V/µA. The frequency response of both circuits is 3dB down at 16kHz. The conventional circuit rolls off at 20dB/decade, while the improved circuit rolls off at 40dB/decade.

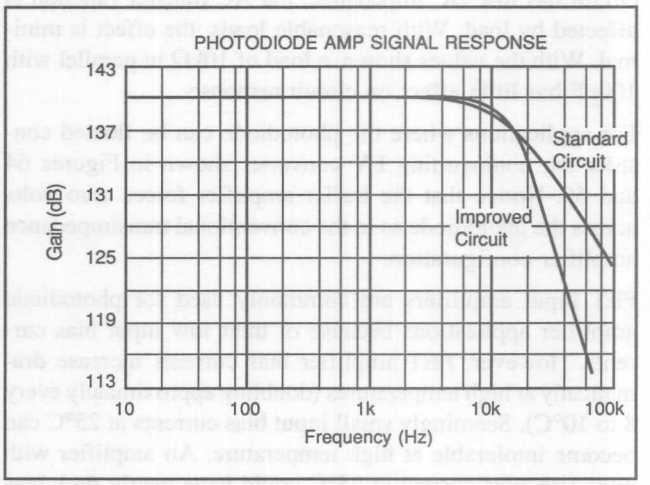

FIGURE 62. Transimpedance signal response of standard and improved photodiode amplifier.

Figure 63 shows the noise gain of both circuits. The noise problem is due to the noise gain zero formed by the relatively high photodiode shunt capacitance, C_O, reacting with the high 10MΩ feedback resistor. The noise zero occurs at:

$$f_Z = \frac{(R_1 + R_3)}{2 \cdot \pi \cdot R_1 \cdot R_3 \cdot (C_0 + C_1)} \sim 673\text{Hz in this example.}$$

Both curves show peaking in the noise gain at about 673Hz due to the zero formed by the photodiode shunt capacitance. The added pole of the improved circuit rolls off the noise gain at a lower frequency, which reduces the noise above 20kHz. Since the signal bandwidth is 16kHz, the region of the spectrum above 20kHz contains only noise, not signal. With the values show, the improved circuit has 3 times less noise. With the OPA602 (voltage noise = 12nV/$\sqrt{Hz}$), and including resistor noise, the improved circuit has 1Hz to 100MHz noise of 68µVrms vs 205µVrms for the standard circuit.

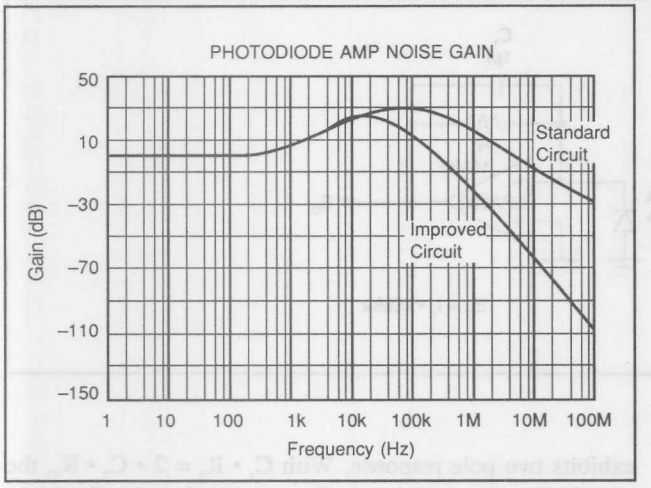

FIGURE 63. Noise gain of standard and improved photodiode amplifier.

Another advantage of the improved circuit is its ability to drive capacitive loads. Since the output of the circuit is connected to a large capacitor, C_2, driving a little extra capacitance presents no stability problems. Although the circuit has low DC impedance, the AC transfer function is affected by load. With reasonable loads, the effect is minimal. With the values shown, a load of 10kΩ in parallel with 100pF has little effect on circuit response.

For applications where the photodiode can be floated consider the noninverting I/V converter shown in Figures 64 and 65. Notice that the buffer amplifier forces zero volts across the photodiode as in the conventional transimpedance amplifier configuration.

FET input amplifiers are commonly used for photodiode amplifier applications because of their low input bias currents. However, FET amplifier bias currents increase dramatically at high temperatures (doubling approximately every 8 to 10°C). Seemingly small input bias currents at 25°C can become intolerable at high temperature. An amplifier with only 1pA bias current at 25°C could have nearly 6nA bias current at 125°C.

The difference between input bias currents, offset curent, is often much better than the absolute bias current. The typical bias current of an OPA156, for example, is 30pA, while its offset current is 3pA.

If amplifier bias current is a problem consider the circuit shown in Figure 66. The added bias current cancellation resistor R_2 cancels the effect of matching op amp input bias currents. This can provide a ten-to-one or better improvement in performance since voltage offset is due only to I_{OS} (offset current) reacting with 5MΩ.

A word of caution. Many amplifiers, especially bipolar input amplifiers, achieve low bias current with internal bias current cancellation circuitry. There may be little or no difference between their I_B and I_{OS}. In this case external bias current cancellation will not improve performance.

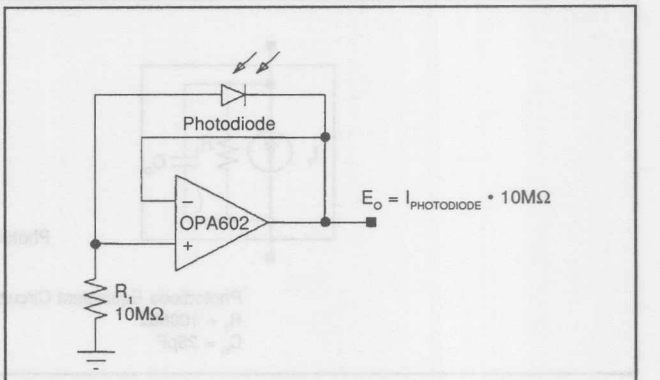

FIGURE 64.

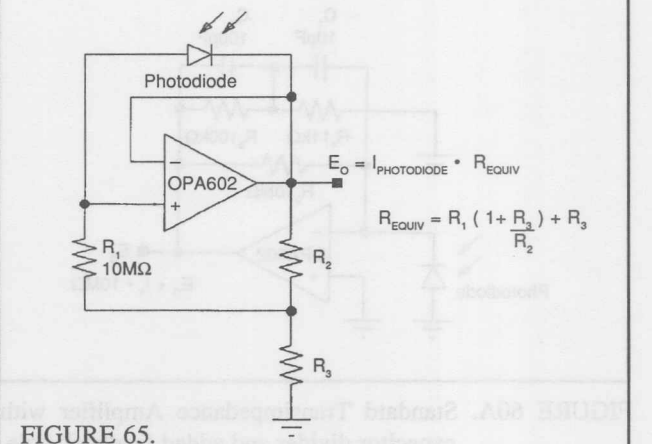

FIGURE 65.

FIGURES 64 and 65. Photodiode amplifier using floating virtual ground current-to-voltage converter.

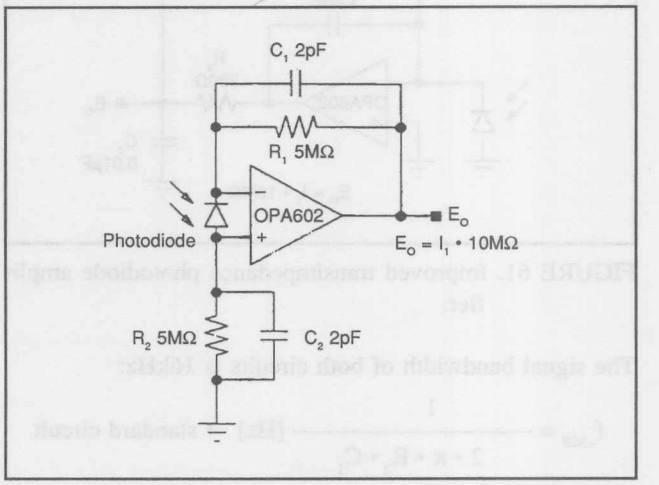

FIGURE 66. Differential Photodiode Transimpedance Amplifier gives bias current cancellation.

GLOSSARY

ABBREVIATIONS, DEFINITIONS

Bidirectional Current Source—A floating current source that provides a constant current independent of the polarity of applied voltage bias.

Current Source—This may be a general term for any current source, current sink, or floating current source. In this text it usually refers to a current generating device referenced to a positive fixed potential such as $+V_S$ of a power supply. The load must be connected between the current source and a more negative potential.

Current Sink—Current generating device referenced to a negative fixed potential such as $-V_S$ of a power supply. The load must be connected between the current sink and a more positive potential.

***Difet*®**—Burr-Brown's trademark for an integrated circuit process which uses dielectric (DI) instead of reverse biased junctions (JI) to isolate devices. This technique eliminates the substrate leakage inherent in JI processes. The result is lower input bias currents for FET input amplifiers, and potential for higher temperature operation and radiation hardness.

Floating Current Source—A current generating device with both ends uncommitted. The load may be connected to either end, or a floating current source may be connected arbitrary between two loads. The current sources in the REF200 are floating current sources. A floating current source may require external power supplies. The floating current sources in the REF200 are self powered, and require no external power supply.

IA—Instrumentation Amplifier. An IA is not an op amp. Unlike an op amp, an IA amplifies the signal at its inputs by a fixed gain while rejecting the common mode signal. An op amp amplifies the signal at its inputs by its open loop gain (ideally infinity). An op amp therefore requires feedback components to make a useful amplifier. It normally takes three op amps and seven precision resistors to make an IA.

I_B—Bias current. The DC current that flows into or out of the input terminals of an amplifier.

IC—Integrated circuit. Often implies monolithic integrated circuit, which is a single-chip electronic circuit.

I_{OS}—Offset current. The difference in I_B of the two inputs of an amplifier.

Op Amp—Operational amplifier. An operational amplifier is a very high gain direct current amplifier with differential inputs. It is intended for applications where the transfer function is determined by external feedback components.

RTD—Resistor Temperature Device. A precision temperature transducer using platinum as the active element. Values at 0°C of 100Ω, 500Ω, and 1000Ω are standard. Due to the high cost of platinum 1kΩ RTDs are becoming more popular.

TCR—Temperature coefficient of resistance. The change of DC resistance with temperature of a resistor. Usually expressed in parts per million per °C [ppm/°C].

TCR Tracking—The match or tracking over temperature of the TCR of two or more resistors.

Transconductance Amplifier—A voltage to current converter.

Transimpedance Amplifier—A current to voltage converter.

CLASSICAL OP AMP OR CURRENT-FEEDBACK OP AMP? THIS COMPOSITE OP AMP GIVES YOU THE BEST OF BOTH WORLDS

By Tim Kalthoff, Tony Wang, and R. Mark Stitt (602) 746-7445

Classical op amps such as the OPA627 have excellent performance in applications where the required gain bandwidth is low compared to the gain-bandwidth product of the op amp. However, increasing closed-loop gain decreases the error-reducing loop gain. Furthermore, starting at relatively low frequencies, the loop gain rolls-off at 20dB/decade of signal frequency increase. In combination these effects can produce significant errors, especially at higher frequencies where the loop gain can be very low.

Current-feedback op amps, such as the OPA603, have good dynamic performance at both low and high gains. This is because the feedback components set both closed-loop gain and open-loop gain, making loop gain and dynamic performance relatively independent of closed-loop gain. Unfortunately, the DC performance (V_{OS}, dV_{OS}/dT, CMR, etc) of current feedback amplifiers is poor compared to classical op amps.

A composite amplifier using a classical amplifier and the OPA603 current-feedback amplifier can combine the best qualities of both amplifiers.

Figures 1 and 2 show noninverting and inverting composite amplifiers. Table I shows suggested component values for selected gains and measured performance results.

DC performance of the composite amplifier is excellent. Since the OPA603 is in the feedback of the OPA627, the composite amplifier retains the excellent DC characteristics of the OPA627. In fact, since the OPA627 does not drive the load directly, its DC accuracy can be better than the OPA627 alone. Thermal feedback within an amplifier driving large loads will cause errors due to internal thermal gradients and package self-heating. The composite amplifier with an OPA603 can drive 150Ω loads to ±10V with no thermal feedback to the OPA627.

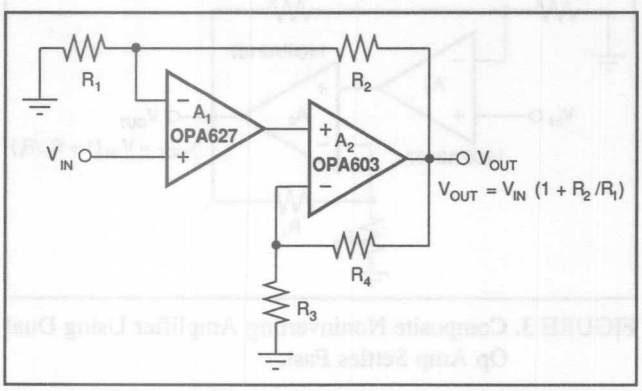

FIGURE 1. Composite Noninverting Amplifier with Precision of OPA627 and Speed of OPA603.

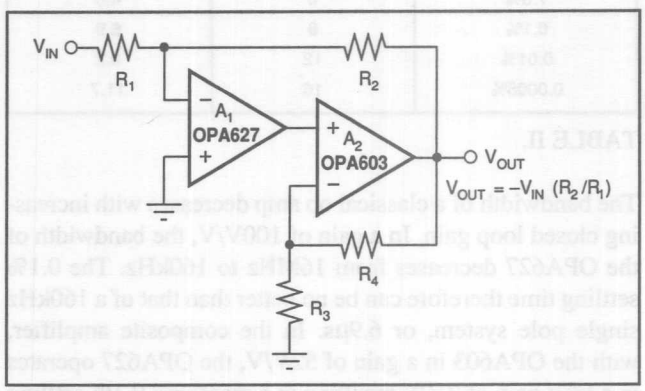

FIGURE 2. Composite Inverting Amplifier with Precision of OPA627 and Speed of OPA603.

OVERALL GAIN [V/V]	GBW [Hz]	A_1	OPA603 GAIN [V/V]	R_1 (1) [Ω]	R_2 [Ω]	R_3 (4) [Ω]	R_4 [Ω]	SLEW RATE [V/μs]	SETTLING (0.1%) (2) [ns]	SETTLING (0.01%) (2) [ns]
5	90M	OPA627	3	255	1020	499	1020	100	265	520
10	180M	OPA627	6	110	1000	200	1020	240	240	500
20	330M	OPA627	12	52.3	1000	93.1	1020	620	200	520
50	750M	OPA627	26	49.9	2430	40.2	1020	730	320	530
100	1.5G	OPA627	52	49.9	4990	20	1020	730	330	(3)
200	2.5G	OPA637	18	49.9	10k	60.4	1020	580	350	(3)
500	6.0G	OPA637	42	49.9	25k	24.3	1020	590	580	(3)
1000	10.0G	OPA637	85	49.9	50k	12.1	1020	510	640	(3)

NOTES: (1) R_1 shown is for noninverting composite amplifier. For inverting amplifier, R_1 = Gain/R_2. (2) Settling time for 10V output step. (3) Output noise exceeds 0.01% at this gain. (4) For intermediate gains, use the higher value R_3.

TABLE I. Measured Results for Selected Composite-Amplifier Examples.

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The gain of the composite amplifier is set by R_1 and R_2 alone. Errors due to R_3 and R_4 do not affect the gain of the composite amplifier. The gain of the second amplifier, set by R_3 and R_4, should be within ±5% to assure expected dynamic performance.

Slew rate and full-power response of the classical amplifier are boosted in the composite amplifier. Since the OPA603 adds gain at the output of the OPA627, the slew rate of the OPA627 is increased by the gain of the OPA603. For example, in the gain-of-100 composite amplifier, the slew rate and full-power response of the OPA627 is increased from 40V/µs min (600kHz) to over 700V/µs (11MHz).

Settling time of the classical amp is preserved, even at higher gains. Settling time of a classical op amp is limited by the time needed to slew to its final value plus the time for its internal circuitry to settle to the desired accuracy. Settling time for a classical op amp is no better than predicted by a single-pole response:

$$T_S = \frac{\ln(100/\%)}{2 \cdot \pi \cdot f_{UGBW}}$$

Where:
T_S = Settling time [µs]
f_{UGBW} = Amplifier unity-gain bandwidth [MHz]
ln(100/%) = Number of time constants needed to settle to desired accuracy, e.g:

ACCURACY (%)	BITS (TO 1/2LSB)	NUMBER OF TIME CONSTANTS
1.0%	6	4.6
0.1%	9	6.9
0.01%	12	9.2
0.0008%	16	11.7

TABLE II.

The bandwidth of a classical op amp decreases with increasing closed loop gain. In a gain of 100V/V, the bandwidth of the OPA627 decreases from 16MHz to 160kHz. The 0.1% settling time therefore can be no better than that of a 160kHz single pole system, or 6.9µs. In the composite amplifier, with the OPA603 in a gain of 52V/V, the OPA627 operates in a loop gain of 2V/V resulting in a measured 0.1% settling time of 330ns.

Care must be taken when selecting the feedback amplifier, A_2, used in the composite. Excessive phase shift through A_2 will cause instability. The OPA603 has sufficient bandwidth to ensure stability when used with amplifiers as fast as the OPA627 (16MHz).

If the bandwidth and settling time advantages of the composite amplifier are needed, but not the slew rate boost, it is possible to make a composite amplifier using a dual op amp such as the OPA2107 as shown in Figures 3 and 4. It is best to use a dual op amp because of the inherent matching of dynamic characteristics. To ensure stability and the best transient response, set the gain of A_1 two times the gain of A_2 using the following relationship:

$$\text{Gain} = 1 + (R_2/R_1) \text{ noninverting}$$
$$\text{Gain} = -(R_2/R_1) \text{ inverting}$$
$$R_4 = 10k\Omega$$

For Figures 3 and 4,

$$R_3 = \frac{R_4}{\sqrt{R_2/(2 \cdot R_1)) - 1}}$$

For example, if Gain = 100, R_4 = 10kΩ, and R_3 = 1.65kΩ.

Cascading two gain stages (each with a gain of 10V/V) would give an overall transfer function of 100V/V and slightly better settling time, but the gain would depend on the accuracy of R_3 and R_4 in addition to R_1 and R_2. The table below shows predicted 0.01% settling time for the three cases.

CONFIGURATION	SETTLING TIME TO 0.01%
Single Amplifier	20µs
Composite Amplifier	4.6µs
Cascaded Amplifier	4.1µs[1]

NOTE: (1) For cascaded amplifier stages, the combined settling time is the square root of the sum of the squares of the individual settling times.

TABLE III. Predicted Settling Time for Gain-of-100 Amplifiers Using OPA2107 Dual Op Amp (Unity Gain Bandwidth = 5MHz).

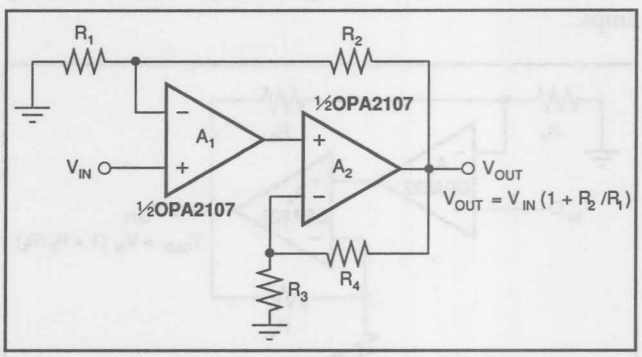

FIGURE 3. Composite Noninverting Amplifier Using Dual Op Amp Settles Fast.

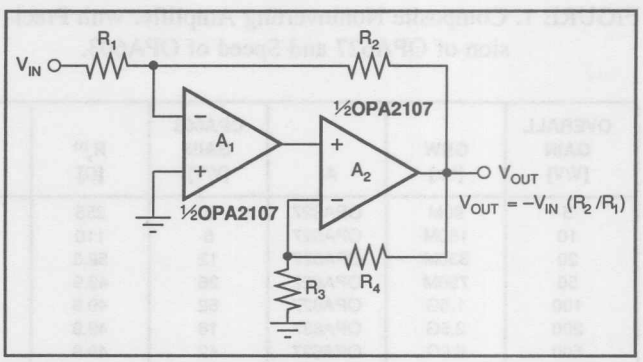

FIGURE 4. Composite Inverting Amplifier Using Dual Op Amp Settles Fast.

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FEEDBACK PLOTS DEFINE OP AMP AC PERFORMANCE

By Jerald G. Graeme (602) 746-7412

(Originally published in EDN magazine as "Feedback Plots Offer Insight into Operational Amplifiers" and "Bode Plots Enhance Feedback Analysis of Operational Amplifiers" on 1/19/89 and 2/2/89, respectively.)

Feedback plots simplify the analysis of an op amp's closed-loop AC performance by showing bandwidth and stability conditions as a function of the op amp's gain and phase response. These plots also provide insight into noise performance and the special feedback requirements of circuits such as integrating converters, photodiode amplifiers, composite amplifiers and active feedback circuits.

Engineers routinely use Bode plots[1] to determine the bandwidth and frequency stability of voltage-gain op amp circuits. A Bode plot provides a visual representation of an op amp's transfer response and its potential stability. Moreover, such plots define the circuit's pole and zero locations at the intercepts of the response-curve extensions.

The Bode plot of Figure 1, for example, shows the interaction of the magnitude response of the open-loop gain (|A|) and the reciprocal of the feedback factor (1/β). The fraction of the output that feeds back to the input is β. The voltage-divider action of Figure 1's feedback network determines the value of β; for moderate resistance values, $\beta = R_1/(R_1 + R_2)$. For this noninverting example, the feedback equation, $A_{CL} = A/(1 + A\beta)$, defines the closed-loop voltage gain. Aβ is the loop gain, and where it is high:

$$A_{CL} \approx 1/\beta = (R_1 + R_2)/R_1$$

Aβ represents the amplifier gain available to maintain the ideal closed-loop response. At the point where the loop gain no longer matches the feedback demand, the closed-loop curve deviates from the ideal. The Bode plot graphically defines this limit by plotting the 1/β curve with the gain-magnitude response curve of the op amp. Because the 1/β line represents the feedback demand, closed-loop requirements will be satisfied as long as this line is below the amplifier-gain curve. Where this condition is no longer true, the actual response drops, following the amplifier's open-loop response downward. The rate of descent for the roll-off is –20dB/decade (for most op amps) and is characteristic of a single-pole response. In Figure 1, the heavier line on the gain-magnitude plot depicts the resulting closed-loop curve.

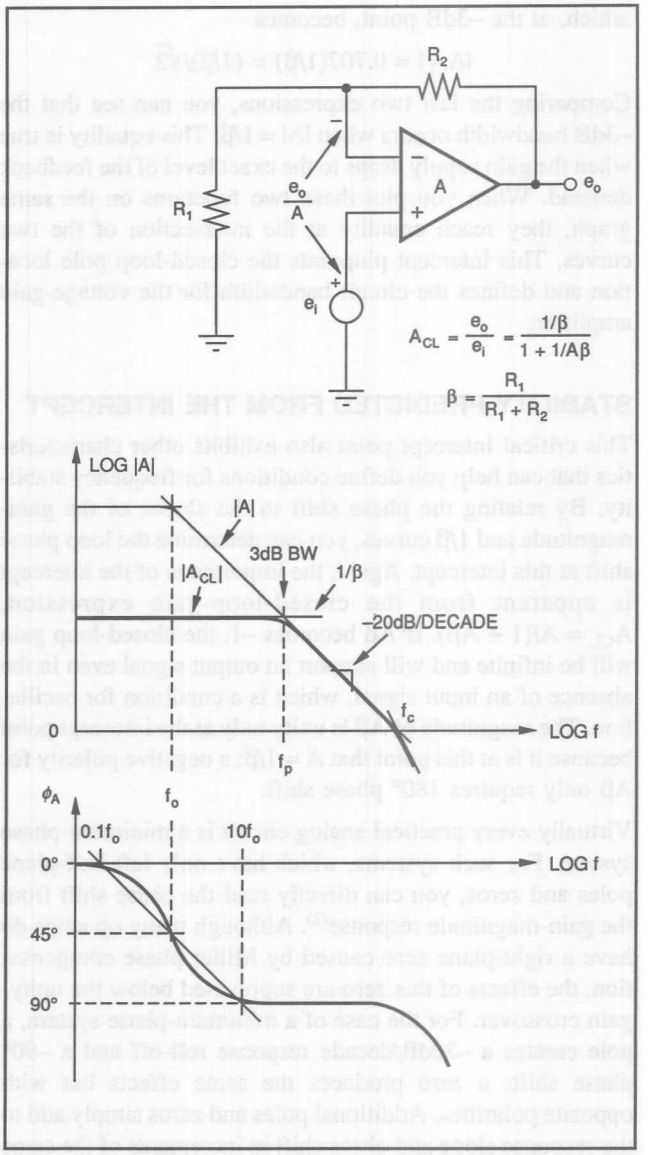

FIGURE 1. This feedback analysis provides a summary of loop conditions in the 1/β curve and defines the underlying poles, zeros, and phase shift.

INTERCEPT DEFINES BANDWIDTH

For a basic voltage-gain amplifier, the location of the f_p pole determines the closed-loop bandwidth. In this case, a single-pole roll-off determines the point at which the gain magnitude goes below 3dB (equivalent to 0.707 of its low-frequency level). To find this point relative to the Bode plots, rewrite the closed-loop gain as

$$A_{CL} = (1/\beta)/(1/A\beta + 1)$$

The bandwidth-defining gain error is a result of the 1/Aβ term in the denominator. Because β is constant for the circuit in Figure 1, the amplifier gain (A) determines the frequency dependence of the loop gain. For a typical op amp, the gain-

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bandwidth product is constant after the first break frequency occurs and $A = jf_c/f = j|A|$ where f_c is the amplifier's unity-gain crossover frequency. For this common condition,

$$A_{CL} = (1/\beta)/(1 + 1/(j|A|\beta)$$

The bandwidth is defined in terms of the absolute value (magnitude) of A_{CL}:

$$|A_{CL}| = (1/\beta)/\sqrt{(1 + 1/(|A|^2\,\beta^2))}$$

which, at the –3dB point, becomes

$$|A_{CL}| = 0.707(1/\beta) = (1/\beta)/\sqrt{2}$$

Comparing the last two expressions, you can see that the –3dB bandwidth occurs when $|A| = 1/\beta$. This equality is true when the gain supply drops to the exact level of the feedback demand. When you plot these two functions on the same graph, they reach equality at the intersection of the two curves. This intercept pinpoints the closed-loop pole location and defines the circuit bandwidth for the voltage-gain amplifier.

STABILITY PREDICTED FROM THE INTERCEPT

This critical intercept point also exhibits other characteristics that can help you define conditions for frequency stability. By relating the phase shift to the slopes of the gain-magnitude and $1/\beta$ curves, you can determine the loop phase shift at this intercept. Again, the importance of the intercept is apparent from the closed-loop-gain expression, $A_{CL} = A/(1 + A\beta)$. If $A\beta$ becomes –1, the closed-loop gain will be infinite and will support an output signal even in the absence of an input signal, which is a condition for oscillation. The magnitude of $A\beta$ is unity only at the intercept point because it is at this point that $A = 1/\beta$; a negative polarity for $A\beta$ only requires 180° phase shift.

Virtually every practical analog circuit is a minimum-phase system. For such systems, which have only left-half-plane poles and zeros, you can directly read the phase shift from the gain-magnitude response[2]. Although many op amps do have a right-plane zero caused by Miller phase compensation, the effects of this zero are suppressed below the unity-gain crossover. For the case of a minimum-phase system, a pole creates a –20dB/decade response roll-off and a –90° phase shift; a zero produces the same effects but with opposite polarities. Additional poles and zeros simply add to the response slope and phase shift in increments of the same magnitude.

Relying on the feedback phase shift's correlation with the response slope, you can determine its value at the critical intercept from the gain-magnitude and $1/\beta$ curves. For the example of Figure 1, the gain-magnitude curve has a slope of –20dB/decade and the $1/\beta$ curve has a zero slope for a net 90° feedback phase shift at the intercept. This situation leaves a phase margin of 90° out of the 180° that would cause oscillation. Because the intercept is well removed from the open-loop-response break frequencies, the analysis of this example is easier to understand. The intercept occurs after the amplifier's first pole develops the full 90° phase shift, but well before the second pole has any effect.

APPROXIMATING PHASE MARGIN

In cases where the intercept is less than one decade from a response break, the Bode approximation of the phase shift shows a linear slope that has a maximum error of 5.7°[1]. For Figure 1, the phase-shift approximation starts at 0° one decade before the break frequency f_o. From there, it increases linearly on the log scale to 45° at the break frequency and then to 90° one decade above it.

Using this approximation, you can combine the stability criteria for loop-gain magnitude and feedback phase shift to obtain the rate-of-closure indicator. Rather than computing phase shifts from slopes, you can use this indicator to deal with the slopes directly. Rate-of-closure is simply the difference in slopes of the gain-magnitude curve and the $1/\beta$ curve when they intercept. This difference reflects the combined phase shift around the feedback loop. For Figure 1, the rate-of-closure is 20dB/decade, which corresponds to a stable 90° phase shift.

In other cases, the slope of the $1/\beta$ curve is not zero, giving a 40dB/decade rate-of-closure that indicates an oscillatory 180° of phase shift. Rate-of-closure alone is an exact stability indicator where the intercept is at least one decade away from all other break frequencies. In still other cases, the Bode phase approximation modifies the rate-of-closure result.

FEEDBACK FACTOR IS A VOLTAGE DIVIDER RATIO

To use feedback relationships to perform circuit analysis, you should consider the feedback network separately. This separation parallels the nature of the op amp's open-loop gain, which is a characteristic of the amplifier in the absence of the feedback network. You only need to retain the loading effects between the amplifier and the feedback network to determine their individual responses[2]. Then, by putting the two responses on the same plot, you can see how they will work together.

Figure 2 shows a generalized feedback condition defined by Z_1 and Z_2. The equations of Figure 2a directly determine the circuit response for high loop gain and moderate impedances. Nonetheless, the input impedance of the amplifier alters the simplified results of these equations by shunting the feedback network. The inclusion of this loading effect on the feedback network completes the $1/\beta$ analysis in the circuit of Figure 2b. Here, the op amp input resistance (R_i), differential input capacitance (C_{id}), and common-mode input capacitance (C_{icm}) all shunt impedance Z_1. Except for conditions where the feedback impedances have low values, you need to include these amplifier characteristics in your analysis.

Where there is impedance in series with the amplifier's noninverting input, you must add this too-along with the shunting effect of the input's C_{icm} capacitance. You can then find the feedback factor from the divider action, e_i/e_o. For the $1/\beta$ curve, this result is inverted and, in the logarithmic format of computer simulations, becomes simply

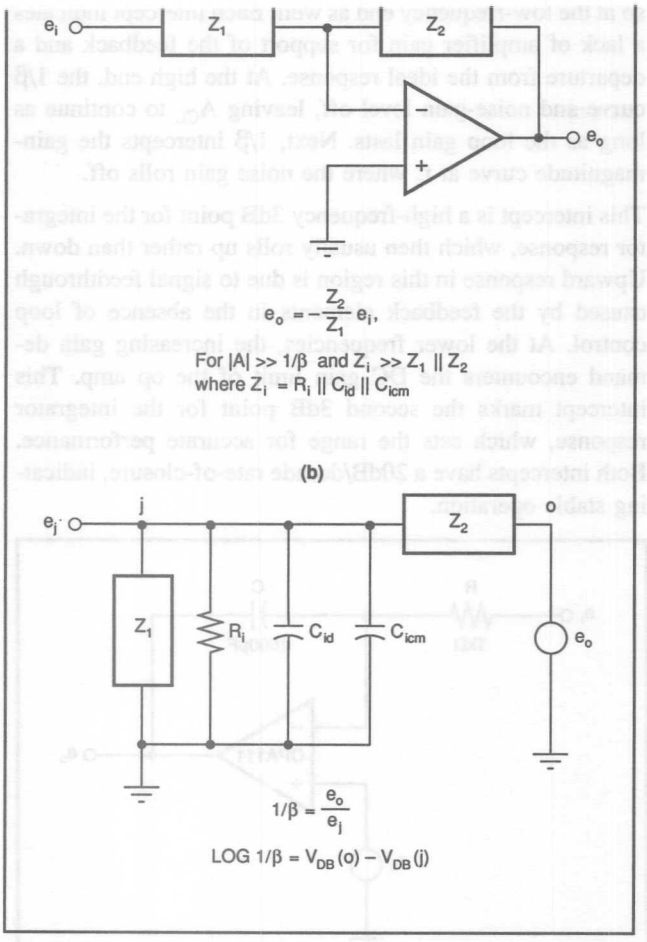

FIGURE 2. To determine the 1/β curve for the generalized circuit of (a), you can draw a voltage-divider circuit that represents the feedback network and the shunting effects of the amplifier input (b).

$V_{DB}(o) - V_{DB}(j)$. By adding this curve to the plot of the amplifier's gain-magnitude response, you can display the characteristics of the critical intercept for subsequent feedback interpretation.

NOISE GAIN AND 1/ß

The 1/β curve also communicates performance information across the entire response range of the op amp. For example, it displays loop gain, which provides an indication of gain accuracy vs frequency and the ultimate bandwidth limit. Furthermore, the 1/β curve demonstrates that the circuit's signal bandwidth can be different from its noise bandwidth. Note that the previous feedback-network analysis returns Z_1 to ground as it would in a noninverting op amp configuration, even though the op amp shown is in the inverting mode.

Underlying the difference between noise and signal bandwidth is the concept of noise gain, which is the source of some of the more common op amp application problems.

in magnitude as well as in sign, nevertheless, the feedback conditions remain the same. In both cases, your feedback analysis is concerned with the gain-error voltage developed between the op amp inputs. This error signal always receives the gain of the noninverting connection, as you would see if you performed superposition analysis. Superposition of the signal between the amplifier inputs grounds the signal source, producing the noninverting configuration.

The same condition holds true for the input voltage noise of an op amp, resulting in the noise-gain characteristic for the 1/β curve. In practice, the noise gain and the 1/β curve are the same—until they intercept with the gain-magnitude curve. After that, the noise gain rolls off with the amplifier open-loop response but the 1/β curve continues on its path. For the noninverting voltage amplifier, the noise gain and the closed-loop gain, A_{CL}, are the same.

NOISE BANDWIDTH

In inverting configurations, this correspondence does not hold true, giving rise to frequent surprises during attempts at noise filtering. The simplest case of the inverting amplifier, where it is common practice to bypass the feedback resistor, serves to illustrate the inverting relationship (Figure 3). Bypassing the feedback resistor is intended to limit noise bandwidth, and it does indeed remove noise presented as an input signal. However, the circuit will continue to pass amplifier noise across the entire op amp bandwidth. C_f shunts the signal supplied through R_1 for the desired lowpass roll-off of the op amp's e_o/e_i response. To the op amp noise voltage, e_n, C_f merely presents the unity feedback of a voltage-follower. Noise gain drops to unity but continues out to the open-loop roll-off of the op amp. This leveling off of 1/β also shows why the op amp must be unity-gain stable, even though the circuit gain has been rolled off well below the amplifier response. With 1/β following the unity gain axis, the critical intercept occurs at f_c.

While the continued noise gain is at a lower level, it covers much of the amplifier bandwidth, which can result in a dramatic increase in output noise. For example, if you're using the 2MHz Burr-Brown OPA111 shown and choose C_f to obtain a 2kHz roll-off, only 0.1% of the amplifier bandwidth will be enclosed in the intended system response. Although the logarithmic scale of the frequency axis may be visually deceptive, the remaining 99.9% of the bandwidth is still available to the amplifier's voltage noise. For an initial gain of 10, the output noise that this amplifier produces is more than doubled by the bandwidth effect. Many active-filter configurations are subject to the same limitation.

The only way to avoid excessive noise bandwidth is to restrict the frequency range of the op amp. By doing so, the control of the noise response switches from the 1/β curve to the amplifier roll-off. Where the op amp has provision for external phase compensation, this control is a simple matter and permits you to remove bandwidth from signal and noise

alike. However, because most op amps lack an external-phase-compensation facility, passive filtering within the feedback loop offers a broader solution[3]. Such filtering introduces a capacitive shunt to ground following the amplifier but within the feedback loop.

You can also demonstrate the extended noise bandwidth of an integrating converter using a feedback plot but, more importantly, the curves illustrate the dynamic-range limit for integrator-based instrumentation. In Figure 4, the integrator 1/β curve also levels off at the unity-gain line for continued noise gain out to where the op amp rolls off. Be aware that this action has far less noise significance for the integrator because of its increasing gain at lower frequencies. Integrators designed for operation to 1kHz or even higher are generally unaffected by the added noise bandwidth.

Nevertheless, the feedback plot for the integrator demonstrates a unique bandwidth limitation involving two critical intercepts. Not only does the 1/β curve intercept the gain-magnitude curve at the high-frequency extreme, but it does so at the low-frequency end as well. Each intercept indicates a lack of amplifier gain for support of the feedback and a departure from the ideal response. At the high end, the 1/β curve and noise-gain level off, leaving A_{CL} to continue as long as the loop gain lasts. Next, 1/β intercepts the gain-magnitude curve at f_c where the noise gain rolls off.

This intercept is a high-frequency 3dB point for the integrator response, which then usually rolls up rather than down. Upward response in this region is due to signal feedthrough caused by the feedback elements in the absence of loop control. At the lower frequencies, the increasing gain demand encounters the DC gain limit of the op amp. This intercept marks the second 3dB point for the integrator response, which sets the range for accurate performance. Both intercepts have a 20dB/decade rate-of-closure, indicating stable operation.

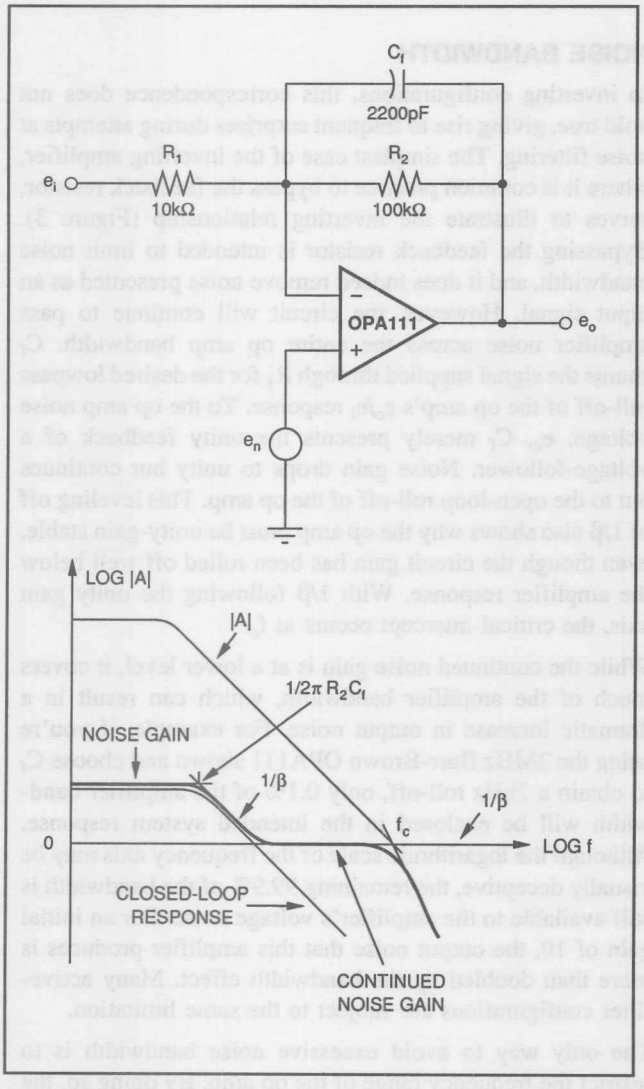

FIGURE 3. Highlighting the difference between closed-loop gain and noise gain, this inverting op amp configuration demonstrates the greater bandwidth that is often available to amplifier noise.

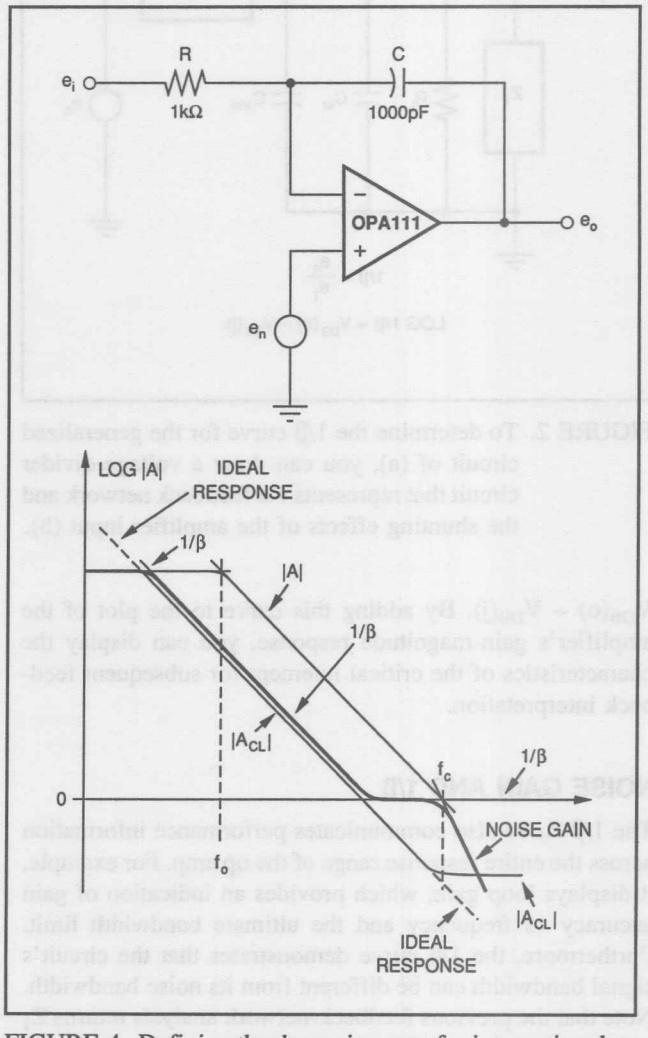

FIGURE 4. Defining the dynamic range for integrating data converters, the integrator 1/β curve displays upper and lower intercepts with the gain-magnitude response.

TWO BANDWIDTH LIMITS FOR INTEGRATORS

Between the two integrator-response limits is the usable dynamic range for dual-slope A/D and V/F converters. The gain error limits this dynamic range; the plots are a graphic representation of this error. The gain error is inversely related either to a circuit's loop gain or the difference between the amplifier's open-loop gain and the feedback demand of 1/β. On the response plots, the loop gain is the vertical distance between the two curves. For the Figure 4 integrator, this separation decreases following 1/βs encounter with the unity-gain axis. From there, the separation finally reduces to zero at f_c. The gain error then becomes the distance between the dashed continuation of the ideal integrator response and the actual A_{CL} response. Graphically, this distance is the source of the large-signal limitation for integrating converters where higher signals correspond to the upper frequencies.

At the other end of the converter range, lower-level signals demand low-frequency integrator operation that encounters a similar limitation. Below the frequency of the op amp's first pole, f_o, the separation between the 1/β and gain-magnitude curves again drops, signaling reduced loop gain. Moving further down in frequency, the 1/β curve finally crosses the op amp's DC-gain level, and the actual response flattens again. For integrating-type converters, this action defines a range of performance that is accurate to within 3dB from f_c down to the lower intercept. To extend the dynamic range, you move the lower intercept downward either with a lower integrator-time-constant or with boosted DC gain.

A higher accuracy dynamic range results from the unique loop-gain conditions of the integrator. The loop gain is constant for the integrator from f_o to its unity-gain crossing. The gain error in this range is constant as marked by the uniform separation of the gain-magnitude and 1/β curves. You can compensate for such an error by making a fixed adjustment to the feedback network, leaving gain-accuracy bounded by the stability of the network. This limit permits you to adjust the more restricted dynamic range to 0.01% levels. For the OPA111 op amp and a 100kHz integrator crossover frequency, this more precise dynamic range has a span of 100,000:1.

INPUT CAPACITANCE ALTERS 1/ß

The previous discussion of the inverter and the integrator considered the feedback network independent of the amplifier input shunting. Although engineers frequently use this simplification, they often encounter unexpected results. Because of the feedback factor, most first-time users of op amps with large feedback-resistance values are surprised by the response curve. Transient-response ringing or even oscillation sometimes occurs; the common cure is a capacitive bypass of the feedback resistor. The 1/β curve can display the problem and provide some guidance in the selection of the bypass capacitor.

Underlying the problem is the op amp input capacitance's effect on the feedback factor. By including this capacitance with the voltage divider formed by the feedback resistors, you can achieve the results of the 1/β curve in Figure 5. This curve rises at high frequencies, increasing the rate-of-closure and flagging the need for closer stability analysis. The phase margin drops as 1/β rises and, at the limit, goes to zero if the 1/β rise spans one decade of frequency. Generally, the span is much smaller than that and the Bode phase approximation evaluates the actual conditions. The key to minimizing the effect on the feedback factor is the low input capacitance that the small input FETs of the OPA128 device provide. The net 3pF of input capacitance leaves the response undisturbed until the parallel combination of the two resistors reaches 50kΩ.

The capacitive bypassing of R_2 increases the high-frequency feedback, which counteracts the shunting of C_{ia} by leveling off the 1/β curve. The selection of this capacitor is better illustrated by Figure 6's photodiode amplifier. You can reduce the non-obvious bandwidth of this application to an equation. The circuit contends with diode capacitances at the input up to 20,000pF. As a result, the break in the 1/β curve is generally far removed from the intercept, making the rate-of-closure analysis accurate without requiring any adjustment of the phase-shift approximation.

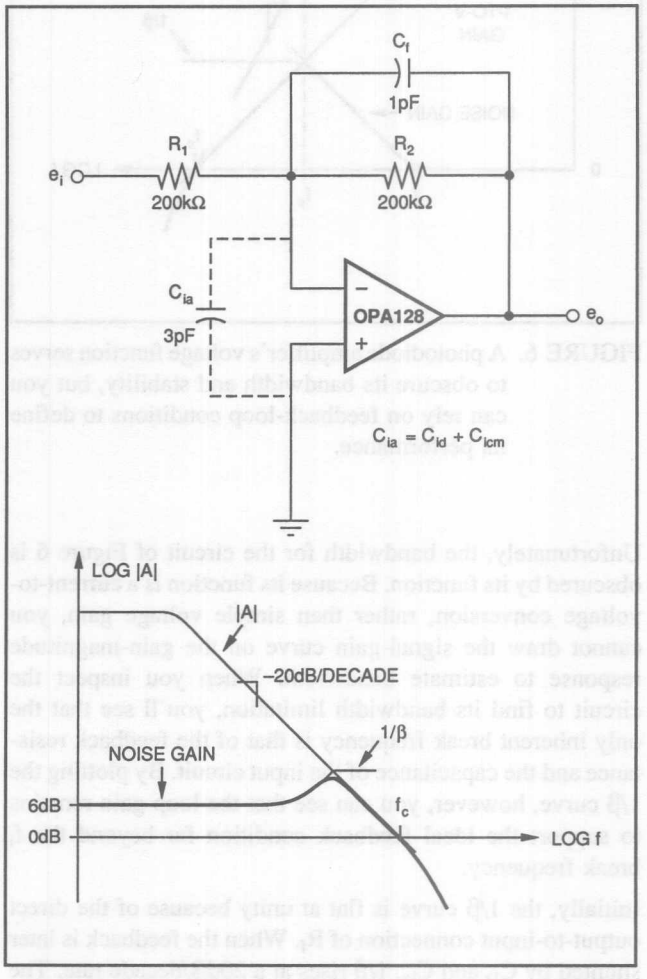

FIGURE 5. Higher feedback resistances will react with the op amp's input capacitance to produce a peaking effect, which the 1/β curve anticipates.

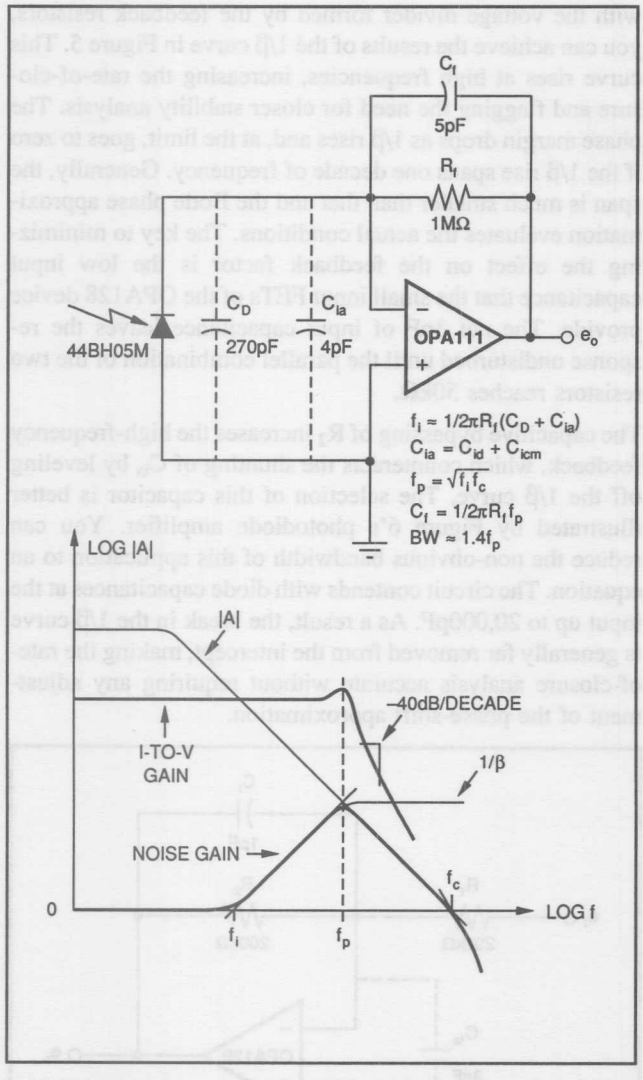

FIGURE 6. A photodiode amplifier's voltage function serves to obscure its bandwidth and stability, but you can rely on feedback-loop conditions to define its performance.

Unfortunately, the bandwidth for the circuit of Figure 6 is obscured by its function. Because its function is a current-to-voltage conversion, rather than simple voltage gain, you cannot draw the signal-gain curve on the gain-magnitude response to estimate bandwidth. When you inspect the circuit to find its bandwidth limitation, you'll see that the only inherent break frequency is that of the feedback resistance and the capacitance of the input circuit. By plotting the 1/β curve, however, you can see that the loop gain remains to support the ideal feedback condition far beyond the f_i break frequency.

Initially, the 1/β curve is flat at unity because of the direct output-to-input connection of R_f. When the feedback is later shunted by C_D and C_{ia}, 1/β rises at a 20dB/decade rate. The transition between these regions occurs at

$$f_i \approx 1/2\pi R_f(C_D + C_{ia})$$

where $C_{ia} = C_{id} + C_{icm}$.

The intercept with the gain-magnitude curve marks the end of the response rise for the noise gain. This curve has a –20dB/decade slope so, if left uncompensated, the rate-of-closure at the intercept will be 40dB/decade. Thus, the plot indicates two poles at that intercept frequency, f_p. This intercept is the point at which there is no longer sufficient amplifier gain for the feedback-factor demand, and it indicates response roll-off independent of the op amp function. Any amplifier function would then roll off with a slope equal to the rate-of-closure.

COMPENSATION BREAKS AT THE INTERCEPT

Because the rate-of-closure is 40dB/decade, you should examine phase shift at the intercept to determine the phase compensation necessary for stability. When the various break frequencies are well removed from the intercept, the rate-of-closure accurately reflects 180° of phase shift for the uncompensated loop. To avoid oscillation and to achieve good damping characteristics, you must reduce this phase shift by at least 45° through roll-off of the 1/β curve.

According to the Bode phase approximation, this phase shift is the amount of phase introduced at a break frequency. Choosing C_f to break with R_f at the intercept frequency, f_p, yields 45° of phase margin. Accompanying this phase condition is a 3dB peak in the signal response, which for a 2-pole response pushes the –3dB bandwidth out to $1.4f_p$. For the OPA111 and the feedback elements shown, the 3dB response extends to 48kHz. (You can extend this analysis to lower capacitance levels, and the common solution mentioned above will still suffice-even for the high-feedback-resistance case of Figure 5.)

As long as C_f breaks with R_f at the frequency of the intercept, the 1/β rise contributes no more than 45° of phase shift. In the range where the op amp phase shift is 90°, this rise leaves a stable 45° phase margin. Nevertheless, as the op amp approaches its crossover frequency, f_c, its contribution to phase shift moves toward 135°. The rule of thumb for selecting C_f remains valid, however, because any intercept near f_c must be a result of a 1/β rise of short duration. The added phase shift of the amplifier, accompanied by a necessary decrease in feedback phase shift at the intercept, results in a net zero effect. By simple sketching of the phase approximations for the 1/β and gain-magnitude curves, you can show this transition.

GEOMETRY DEFINES INTERCEPT

To select the compensation capacitance, it is desirable to reduce the graphical analysis to an equation. Luckily, the response plots provide an elegantly simple solution. Straight-line extensions of the 1/β and gain-magnitude curves form a triangle with the horizontal axis. These extensions have equal but opposite slopes, which form an isosceles triangle. The peak of the triangle, located over the center of its base, lies at the average of the base end points. Mathematically, this average point is equal to

$$\text{Log } f_p = (\text{Log } f_i + \text{Log } f_c)/2$$

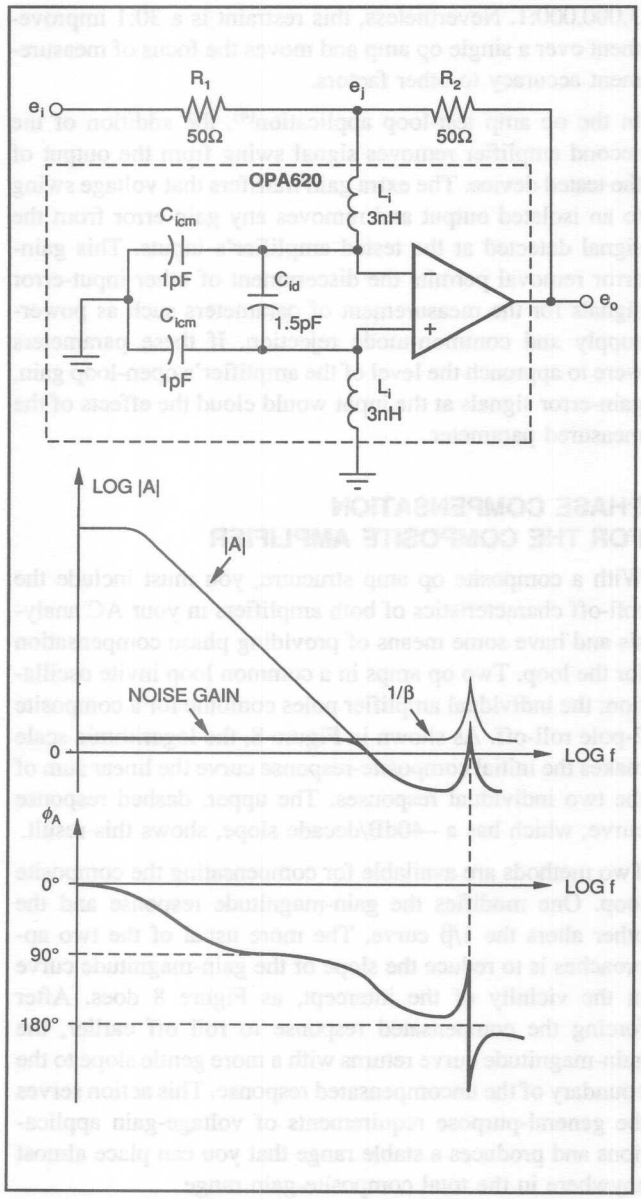

FIGURE 7. Although amplifier gain and phase plots suggest instability, the 1/β curve shows stable conditions for a circuit with input-lead inductance.

Given the expressed logarithmic nature of the frequency axis, you can reduce this relationship to the simple geometric mean of the two characteristic frequencies:

$$f_p = \sqrt{f_i\, f_c}$$

where $f_i = 1/2\pi R_f(C_D + C_{id} + C_{icm})$, and f_c equals the unity-gain bandwidth of the op amp.

GAIN AND PHASE CAN BE MISLEADING

For a third input-circuit effect, the 1/β curve demonstrates stable conditions where typical gain and phase plots would point to oscillation. In addition to input capacitance, op amps have input inductance; this combination produces a high-frequency resonance. The inductance is small but inescapable, being associated with internal input wires and being compounded by external wiring.

For very high-frequency amplifiers, like the OPA620 wideband amplifier of Figure 7, sufficient amplifier gain exists at the resonant frequency to give the appearance of zero gain margin. A comparison of the output signal (e_o) with that at the summing junction (e_j) produces the plot's gain and phase responses. Following unity crossover, the gain curve rises again above the unity axis; this rise generally guarantees oscillation for lower gain levels. Adding to stability concerns is the phase plot, which swings wildly through 180° during the gain peak.

By adding the 1/β curve to the plot, you can see that this curve does not intersect the gain peak but merely rides over it. Without an intercept there is no oscillation, regardless of the phase shift, because the loop gain is insufficient. Loop-gain demand rises in synchronization with the gain peak because the resonant circuit also alters the feedback network.

In many cases, the gain peaking results from conditions in the amplifier output rather than from the input circuit. In such a case, no corresponding modification of feedback occurs, and an intercept and oscillation result. However, for Figure 7, the gain margin remains high, as you can see by the separation between the 1/β curve and the gain response when the phase reaches 180°. This separation remains large throughout the region of higher phase shift, indicating good relative stability.

COMPOSITE AMPLIFIERS

Whereas the normal op amp feedback loop involves only one amplifier, designers often need to extend the feedback loop to work with composite circuits that use two or more op amps for increased gain. By adhering to conventional feedback principles, you can implement phase compensation for the extended loop and rely on a Bode plot to provide a visual representation of the increased gain and the opportunity for extended bandwidth.

For instance, with two op amps in the same loop as in Figure 8, you can achieve increased gain without incurring any added offset and noise error. The input-error effects of the second amplifier are divided by the open-loop gain of the first amplifier. The net open-loop gain of this composite circuit becomes the product of the individual op amp gains and greatly reduces the overall gain error and nonlinearity.

In Figure 8, the two op amps are those of the dual OPA2111, which imposes only a modest cost increase over a single device. You could, of course, select individual op amps to provide specific performance characteristics. In the latter case, you might select the input amplifier for good DC and noise performance and the output amplifier for its load-driving and slewing performance. For example, the output amplifier could handle the load current and the resulting power dissipation, thus producing no thermal feedback to the input of the composite circuit. Moreover, it could also fulfill the high-slew-rate demands of the application. The input amplifier in this case would only swing through small signals.

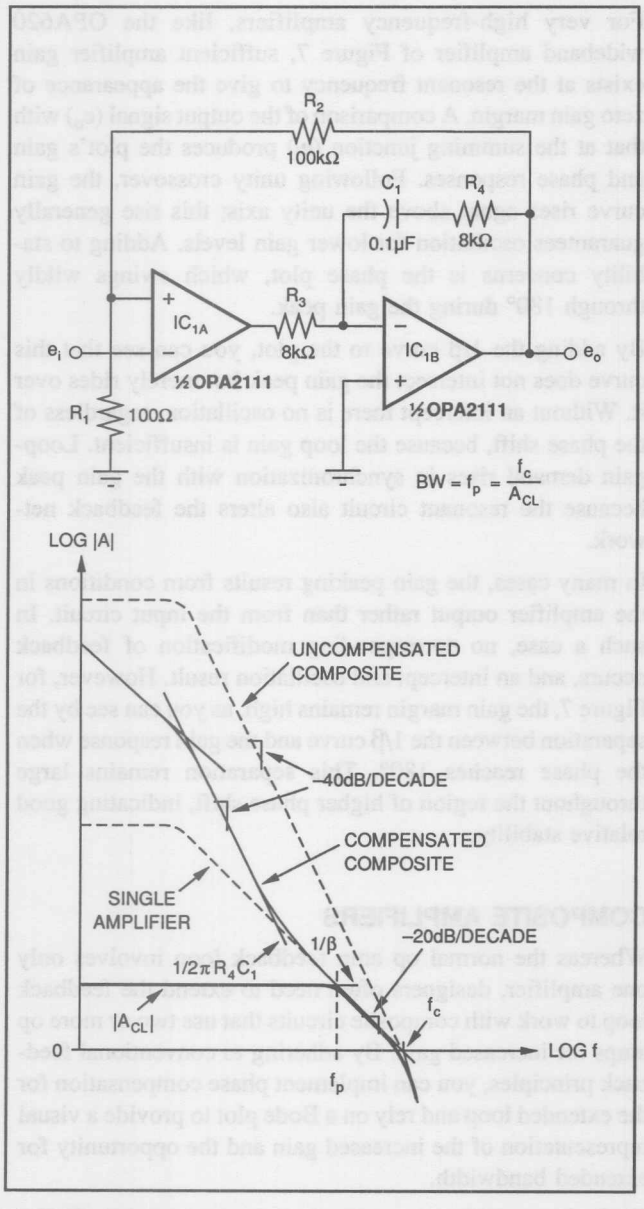

FIGURE 8. To utilize the boosted gain of the composite amplifier, traditional phase-compensation techniques tailor the gain-magnitude slope to obtain a stable region with a 1/β intercept.

An integrator and a common op amp test loop can demonstrate the benefits of using a composite amplifier. By extending the composite open-loop gain to higher levels, you can expand the dynamic range for integrating analog functions. The low-frequency intercept moves back by a factor equal to the added amplifier gain. This change is so extreme that other error effects will surface well before the gain error from the intercepts. For two op amps in the same loop each having 100dB open-loop gain, the composite gain is 200dB. At this gain level, an input error of 1nV will develop the full 10V output swing. Long before the circuit reaches that limit, noise becomes a prime AC constraint and typically restrains lower-level accuracy over a dynamic range of about 3,000,000:1. Nevertheless, this restraint is a 30:1 improvement over a single op amp and moves the focus of measurement accuracy to other factors.

In the op amp test-loop application[4], the addition of the second amplifier removes signal swing from the output of the tested device. The extra gain transfers that voltage swing to an isolated output and removes any gain error from the signal detected at the tested amplifier's inputs. This gain-error removal permits the discernment of other input-error signals for the measurement of parameters such as power-supply and common-mode rejection. If these parameters were to approach the level of the amplifier's open-loop gain, gain-error signals at the input would cloud the effects of the measured parameter.

PHASE COMPENSATION FOR THE COMPOSITE AMPLIFIER

With a composite op amp structure, you must include the roll-off characteristics of both amplifiers in your AC analysis and have some means of providing phase compensation for the loop. Two op amps in a common loop invite oscillation; the individual amplifier poles combine for a composite 2-pole roll-off. As shown in Figure 8, the logarithmic scale makes the initial composite-response curve the linear sum of the two individual responses. The upper, dashed response curve, which has a –40dB/decade slope, shows this result.

Two methods are available for compensating the composite loop. One modifies the gain-magnitude response and the other alters the 1/β curve. The more usual of the two approaches is to reduce the slope of the gain-magnitude curve in the vicinity of the intercept, as Figure 8 does. After forcing the compensated response to roll off earlier, the gain-magnitude curve returns with a more gentle slope to the boundary of the uncompensated response. This action serves the general-purpose requirements of voltage-gain applications and produces a stable range that you can place almost anywhere in the total composite-gain range.

Figure 8 achieves this compensation by creating a modified integrator response for IC_{1B}. Because this integrator is an inverting circuit, the inputs of IC_{1A} are reversed to retain only one phase inversion in the loop. Capacitor C_1 blocks the local DC feedback, and the overall gain is still the product of the two open-loop gains. The integrator response that R_3 and C_1 established for IC_{1B} rolls off this composite gain. Next, the first open-loop pole of IC_{1A} returns the compensated response slope to –40dB/decade. At a higher frequency, a response zero provides the region of reduced slope thanks to the inclusion of R_4. Above the break frequency of R_4 and C_1, R_4 transforms the response of IC_{1B} from an integrator to an inverting amplifier with a gain of $-R_4/R_3$.

Where this gain is unity, the compensated response drops to and follows the open-loop response of IC_{1A} as shown. For gain levels other than unity, you have different options, which you can explore by using other response plots and defining the particular stable conditions you have in mind.

Having control of this gain becomes particularly useful as the 1/β intercept approaches the uncompensated unity-gain crossover point. In this region, the second poles of the two op amps increase the phase shift. In such cases, you have to make the magnitude of the internal R_4/R_3 gain less than unity to force the compensated response to cross over earlier. Generally, when you have two op amps of the same type, making $R_4 = R_3/3$ will yield a unity-gain stable composite amplifier.

The net phase correction that you can achieve with this technique depends on the frequency-response range for which you maintain the –20dB/decade slope. This span begins with the R_4C_1 break frequency and ends with the intercept of the composite open-loop response. After this intercept, the lack of open-loop gain returns the response to that of the uncompensated composite amplifier. To ensure a phase margin of 45° or more, you can use the guidance that the Bode phase approximation provides; the plot shows that this reduced slope region must last for three decades of frequency and must intercept the 1/β curve after running for at least a decade.

COMPOSITE AMPLIFIERS EXTEND BANDWIDTH

Although most engineers are familiar with this type of phase compensation, it is too restrictive of bandwidth at higher gains. For applications requiring higher gains, you can greatly extend the bandwidth and reduce the settling time by 40:1 by using a different phase-compensation technique. The general-purpose $R_4 = R_3$ case of Figure 8 sets a constant closed-loop gain-bandwidth product. Looking at the curves, you can see that the closed-loop bandwidth is the same as that for IC_{1A} itself when $BW = f_p = f_c/A_{CL}$. Even so, the large separation between the compensated and uncompensated responses shows a significant sacrifice in bandwidth—expressly for the accommodation of phase compensation. Uncompensated, the gain-magnitude response has a gain-bandwidth product that increases with closed-loop gain and that provides a potential bandwidth of $f_p = f_c/\sqrt{A_{CL}}$. Comparing the last two expressions shows that the potential for bandwidth improvement equals $\sqrt{A_{CL}}$, which is significant at higher gains.

COMPENSATE THE 1/ß CURVE

You can take advantage of quite a bit of this bandwidth-improvement opportunity by compensating the 1/β curve instead of the gain-magnitude response curve. By referring back to the rate-of-closure stability criteria discussed previously, you would see that both curves contribute to the rate-of-closure parameter even though the gain-magnitude curve is generally the focus of phase-compensation efforts. To satisfy the rate-of-closure criteria, all that is necessary is to control the difference between the slopes, regardless of the slopes of the individual curves. So, instead of reducing the gain-magnitude slope, increase the 1/β slope (Figure 9). A simple capacitive bypass of feedback resistor R_2 accomplishes this slope increase for a final 20dB/decade rate-of-closure.

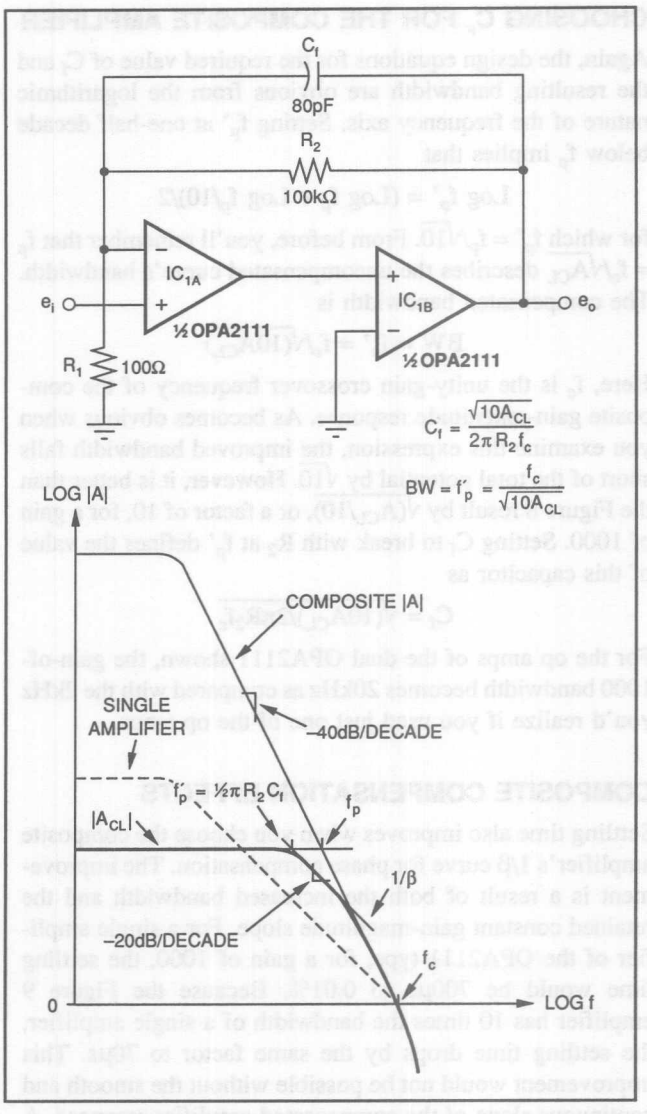

FIGURE 9. For greater bandwidth in high-gain circuits, you can provide phase compensation for the 1/β response to retain a smooth open-loop response for fast settling.

An integrator configuration, on the other hand, with its special characteristics, inherently produces the –20dB/decade slope for 1/β and achieves optimum bandwidth and dynamic range.

Two factors distinguish this feedback-factor compensation technique for higher gains. Greater bandwidth is open for reclaiming, and the associated 1/β curves are well above the unity-gain axis. From higher levels, the 1/β roll-off is developed well before its intercept with the gain-magnitude curve. Starting this roll-off a decade ahead of the final intercept produces a 45° phase adjustment for a like amount of phase margin. The slopes of the two curves show that, in order to accomplish this phase adjustment, C_f must break with R_2 one-half decade below the initial intercept frequency, f_p. Then, the 2:1 difference in slopes will place the new intercept one-half decade above f_p for the required full decade of the 1/β roll-off.

CHOOSING C_F FOR THE COMPOSITE AMPLIFIER

Again, the design equations for the required value of C_f and the resulting bandwidth are obvious from the logarithmic nature of the frequency axis. Setting f_p' at one-half decade below f_p implies that

$$\text{Log } f_p' = (\text{Log } f_p + \text{Log } f_p/10)/2$$

for which $f_p' = f_p/\sqrt{10}$. From before, you'll remember that $f_p = f_c/\sqrt{A_{CL}}$ describes the uncompensated curve's bandwidth. The compensated bandwidth is

$$BW = f_p' = f_c/\sqrt{(10A_{CL})}$$

Here, f_c is the unity-gain crossover frequency of the composite gain-magnitude response. As becomes obvious when you examine this expression, the improved bandwidth falls short of the total potential by $\sqrt{10}$. However, it is better than the Figure 8 result by $\sqrt{(A_{CL}/10)}$, or a factor of 10, for a gain of 1000. Setting C_f to break with R_2 at f_p' defines the value of this capacitor as

$$C_f = \sqrt{(10A_{CL})/2\pi R_2 f_c}$$

For the op amps of the dual OPA2111 shown, the gain-of-1000 bandwidth becomes 20kHz as compared with the 2kHz you'd realize if you used just one of the op amps.

COMPOSITE COMPENSATION EFFECTS

Settling time also improves when you choose the composite amplifier's 1/β curve for phase compensation. The improvement is a result of both the increased bandwidth and the retained constant gain-magnitude slope. For a single amplifier of the OPA2111 type, for a gain of 1000, the settling time would be 700µs to 0.01%. Because the Figure 9 amplifier has 10 times the bandwidth of a single amplifier, the settling time drops by the same factor to 70µs. This improvement would not be possible without the smooth and continuous slope of the compensated-amplifier response. A response having an intermediate pole and zero, such as Figure 8 does, has low-frequency response terms that are slow to settle following a transient. Known as an integrating frequency doublet, this pole/zero combination is notorious for its poor settling time[5]. By providing phase compensation for the 1/β curve, you ensure that the smooth gain-magnitude curve is left undisturbed, therefore achieving the optimum settling time.

At lower gains, the benefit of the 1/β compensation technique diminishes as does its control of phase. Because lower gains have 1/β curves closer to the unity-gain axis, they have less room for 1/β roll-off. To produce an intercept with the gain-magnitude curve after a decade of 1/β roll-off requires a minimum closed-loop gain of 10. Op amp phase shifts impose further limits by growing from 90° to 135° as they approach the unity-gain crossover frequency. In the practical case, this phase-compensation method needs gains of 30 or more for good stability.

This type of phase compensation does have an unusual aspect: Too great a compensating capacitance will have a surprising effect. Whereas increasing such capacitance normally yields more damping and a more stable response, making C_f too large will cause instability. As C_f increases, the resulting intercept moves toward f_c and encounters the added phase shift of the secondary-amplifier poles. Even greater values of C_f will drop the 1/β curve to its limit at the unity-gain axis. From there, it proceeds along the axis to the magnitude-curve intercept that guarantees oscillation. Only a range of compensation-capacitor values provides stability with this second approach; the 1/β curves display this range for sensitivity-analysis purposes. Because of the capacitor's window of stable values, a random selection of C_f followed by a stability test is likely to miss the bandwidth opportunity of this technique.

PHASE ONLY MATTERS AT THE INTERCEPT

Another concept fundamental to op amp feedback in composite-amplifier circuits becomes apparent when you examine phase shift and stability. Composite amplifiers such as the one in Figure 10 produce a –40dB/decade slope over wide ranges both before and after the 1/β intercept. Because this slope corresponds to a 180° phase shift, frequent concern over stability conditions arises at points other than that of the critical intercept. Beyond the 1/β intercept, the loop gain is less than 1 and therefore it is easy to see that the circuit cannot sustain oscillation. Yet, prior to the intercept, the gain of the feedback loop is very high and would seem capable of causing the circuit to oscillate.

In reality, the high loop gain is a protection against, rather than a promoter of, oscillation. Sustained oscillation depends on the op amp's gain-error signal. In Figure 10, the gain error, e_o/A, appears between the op amp inputs and receives amplification from the closed-loop gain, A_{CL}. Here, A_{CL} is that of the noninverting configuration, the noise gain that reacts with any input-referred error signal. To sustain oscillation, the amplified error signal must independently deliver the output signal. This action requires that $(-e_o/A)A_{CL} = e_o$. Note that e_o appears on both sides of this equation; it should therefore be obvious that any solution must conform to very specific constraints. This equation expresses both polarity and magnitude constraints; the composite amplifier's 180° phase shift satisfies the sign change.

For the magnitude constraint, two possible solutions exist. The first is $e_o = 0$, which is the stable state for the composite amplifier in the questioned region. There, the loop gain makes the signal e_o/A too small to independently support an output signal. In the plots of Figure 10, e_o/A starts at a very low level due to the high loop gain at low frequencies. As you move up in frequency, the gain-error signal rises while the amplifier-response slope signals its polarity inversion through the 180° phase shift. This inversion increases the output signal but cannot sustain it until the gain-error signal reaches a sufficient level. This critical level is a prerequisite for oscillation.

This level applies to the second solution for the magnitude constraint. At this level, A/A_{CL} has unity magnitude and maintains the balance for the previous feedback equation's magnitude requirement. Unity loop gain occurs at the 1/β

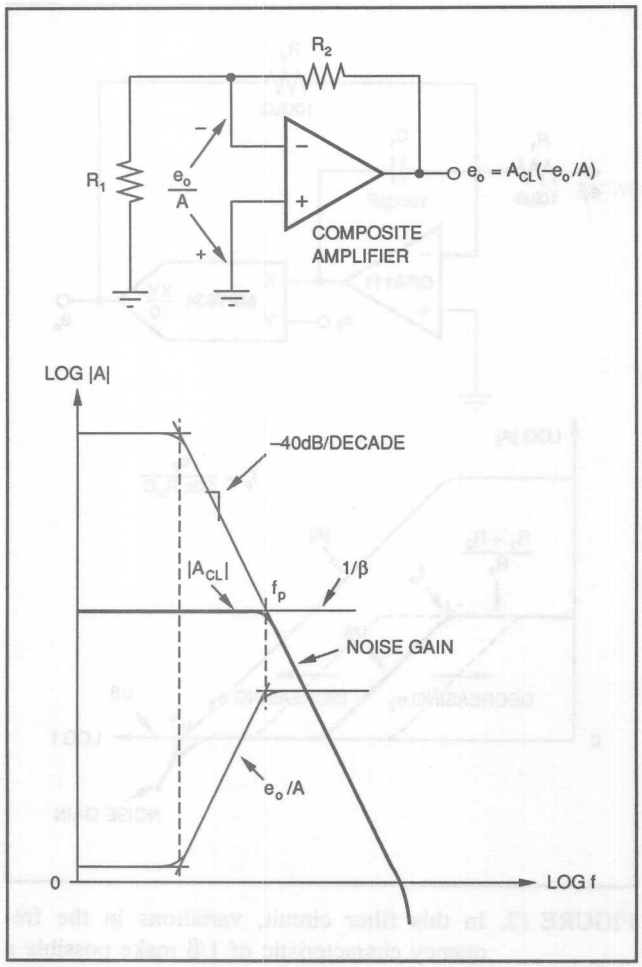

FIGURE 10. A phase shift of 180° causes oscillation only where the gain-error, e_o/A, is capable of independently supporting the output signal.

intercept where the open-loop and noise-gain curves meet. Without phase-compensation intervention, this intercept satisfies both the phase and magnitude requirements for oscillation. Beyond this point, e_o and A fall off together, leaving the e_o/A signal constant and unable to support oscillation with the reduced gain. At the point where the magnitude of the gain error and the feedback phase shift must both reach specific levels to support oscillation, the intercept becomes critical. Before or after the intercept, the loop phase shift can be at any level and the gain-error magnitude will not be sufficient to cause instability.

Unfortunately, despite the composite amplifier's very specific requirements for oscillation, the greatly varied applications of op amps make this critical condition all to easy to encounter. To contend with this problem, you can rely on the 1/β curve to present a visual prediction of the problem and provide insight into a solution.

ACTIVE FEEDBACK VARIES 1/ß

Some applications demand that you include a second active element in the feedback loop to produce a varying feedback factor. In these applications, both the magnitude and the

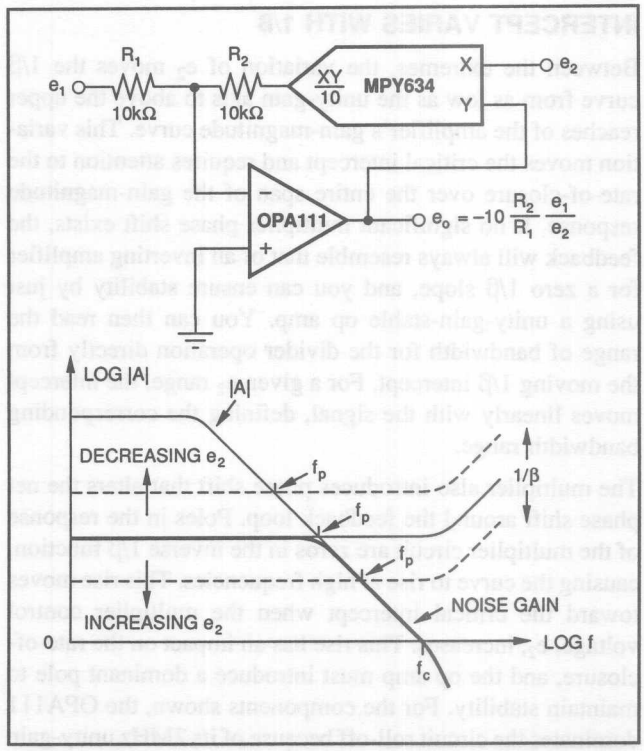

FIGURE 11. For this common analog divider, a variable feedback magnitude allows a range of conditions that define bandwidth and stability.

frequency characteristics of 1/β become variables. Fortunately, the gain- and feedback-response curves offer a means of quickly evaluating the range of conditions resulting from the changing feedback.

The most common way to provide magnitude variation in the feedback factor is to use a low-cost analog divider realization. Placing a multiplier in the feedback loop of an op amp (Figure 11) makes feedback a function of a second signal and therefore produces divider operation. With signal dependent feedback, the bandwidth and stability conditions also become variables.

Figure 11 shows the divider connection[6] and demonstrates the effect of voltage-controlled feedback on 1/β. The amplifier's feedback inverts the function of the multiplier by placing the feedback signal under the control of the e_2 signal. Then, the multiplier's transfer function of XY/10 delivers $e_o(e_2/10)$ to R_2. This action scales the feedback signal by comparing e_2 to 10V reference level to obtain

$$\beta = (e_2/10)\, R_1/(R_1 + R_2)$$

With the feedback factor under control of this signal, the 1/β curve moves across the full range of the gain-magnitude response. As e_2 nears zero, the 1/β curve approaches infinity, leaving the op amp essentially in an open-loop configuration. At the other extreme, a full-scale 10V value for e_2 delivers a feedback signal to R_2 that equals e_o almost as if the multiplier were not present. Then, the net response is that of a simple inverting amplifier with a feedback factor of $R_1/(R_1 + R_2)$ and an inverting gain of $-R_2/R_1$.

INTERCEPT VARIES WITH 1/ß

Between the extremes, the variation of e_2 moves the 1/β curve from as low as the unity-gain axis to above the upper reaches of the amplifier's gain-magnitude curve. This variation moves the critical intercept and requires attention to the rate-of-closure over the entire span of the gain-magnitude response. If no significant multiplier phase shift exists, the feedback will always resemble that of an inverting amplifier for a zero 1/β slope, and you can ensure stability by just using a unity-gain-stable op amp. You can then read the range of bandwidth for the divider operation directly from the moving 1/β intercept. For a given e_2 range, the intercept moves linearly with the signal, defining the corresponding bandwidth range.

The multiplier also introduces phase shift that alters the net phase shift around the feedback loop. Poles in the response of the multiplier circuit are zeros in the inverse 1/β function, causing the curve to rise at high frequencies. This rise moves toward the critical intercept when the multiplier control voltage, e_2, increases. This rise has an impact on the rate-of-closure, and the op amp must introduce a dominant pole to maintain stability. For the components shown, the OPA111 dominates the circuit roll-off because of its 2MHz unity-gain crossover frequency. This frequency is well below the 10MHz bandwidth of the MPY634 multiplier, placing the op amp in control. Other options that use a separate feedback path to restrict the op amp bandwidth are also available[3].

VARIABLE 1/ß FREQUENCY RESPONSES

Other ways of providing variable feedback are also available. For example, you can have the signal control the frequency-rather than the magnitude-characteristics of the feedback. The result is a variable slope at the intercept, as is the case with the voltage-controlled lowpass filter in Figure 12. The basic elements of the lowpass filter are the op amp, the resistors, and the capacitor. If you replace the multiplier with a short circuit, these elements form a fixed-frequency roll-off. Essentially, this shorted condition is established when e_2 = 10V and when the gain through the multiplier is unity. Capacitor C_1 then breaks with R_2 to define the filter roll-off just as if the resistor and capacitor were directly in parallel.

For levels of e_2 below full scale, the multiplier serves as a voltage-controlled attenuator to effectively alter the filter time constant. Attenuating the feedback voltage to R_2 lowers the signal current to the summing node, which has the same effect as increasing the resistor's value. Increased effective resistance corresponds to a decrease in the resistor's break frequency with C_1. This break defines the variable filter roll-off when

$$f_p = e_2/20\pi R_2 C_1$$

The maneuvering of the 1/β curve through this operation deserves closer inspection. The circuit exhibits a signal-dependent transition between the two different loops, which alternately control the feedback. At low frequencies, C_1 is effectively an open circuit, and the controlling feedback path

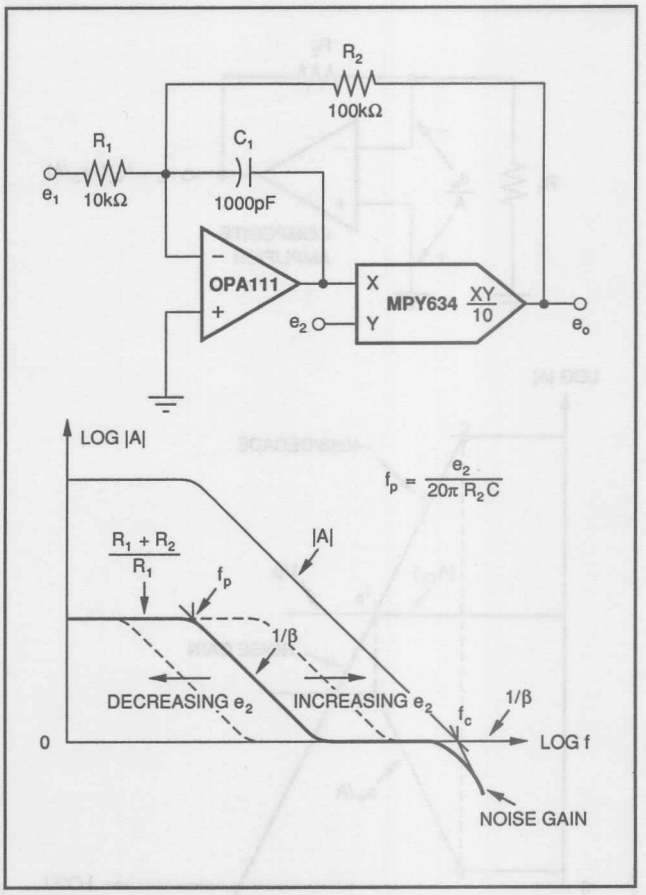

FIGURE 12. In this filter circuit, variations in the frequency characteristic of 1/β make possible a changing 1/β slope at the intercept.

is through the op amp and the multiplier. This composite structure has resistive feedback that defines a signal gain of $-R_2/R_1$ and a noise gain of $(R_1 + R_2)/R_1$. The latter relationship equals 1/β at low frequencies and the curve of interest starts at this level with a zero slope. At the high-frequency end, the composite structure is overridden when C_1 acts as a short circuit, which results in a unity feedback factor around the op amp. This short circuit absorbs all feedback current from R_2 without any corresponding change in the amplifier output voltage. The feedback loop of the composite structure is then disabled, switching feedback control to just the op amp. With C_1 then providing a unity feedback factor to the op amp, the 1/β curve follows the unity-gain axis at high frequencies.

Once the 1/β levels are fixed at the extremes, the multiplier determines the nature of the transition between the two. In the transition region, feedback currents from R_2 and C_1 compete for control of the summing node of the op amp input. The contest for dominance is analogous to the frequency-dependent control of impedance with a parallel RC circuit. In both cases, the 3dB point, where each element carries the same magnitude of current, defines the transition of control. The Figure 12 filter achieves equal element currents when the impedance of C_1 and the effective impedance of R_2 are equal. This equality defines the voltage-

controlled roll-off frequency of the filter as previously expressed. At this frequency, 1/β also rolls off and drops at –20dB/decade to the high-frequency limit of the unity-gain axis.

RATE-OF-CLOSURE VARIES WITH 1/ß

The stability conditions of the Figure 12 circuit depend on the particular feedback loop or the combination of elements that are in control at the intercept point. For the lower-frequency filter cutoff frequencies illustrated, the op amp's bypass capacitor takes control before the intercept and defines the relevant feedback conditions. Because the 1/β curve follows the unity axis at the upper end, you can guarantee stability by ensuring that the op amp be unity-gain stable. For higher-frequency cutoff frequencies, the 1/β transition moves toward the gain-magnitude curve of the op amp. Circuit response cannot move beyond this limit, so the op amp roll-off becomes the upper boundary of filter operation.

When the cutoff frequency approaches this boundary, the intercept rate-of-closure varies, prompting stability analysis. First, the zero of the 1/β curve approaches the intercept, where it increases the slope of the curve. Because this action reduces the rate-of-closure, stability is improved and a more detailed analysis is unnecessary. A continued increase in the cutoff frequency moves the 1/β curve further to the right where its pole interacts at the intercept. This break frequency returns the rate-of-closure to 20dB/decade, thus retaining stability. Beyond this point, the intercept occurs at the flat lower end of the 1/β curve, and no further change in the rate-of-closure takes place.

Utilizing these various feedback conditions and a unity-gain-stable op amp, you can design a composite circuit that fulfills its primary stability requirement over the entire operating range. In addition, however, you may sometimes require a multiplier having a bandwidth much greater than that of the op amp, as the two previous examples demonstrate. Without a wide-bandwidth multiplier, 1/β would begin to rise near the higher-frequency intercepts and increase the rate-of-closure. The OPA111 avoids this complication when using the MPY634 multiplier by maintaining a dominant op amp pole.

Other applications may involve feedback peaking and op amps that are not unity-gain stable-log amps and active filters, for example. For these and other variations requiring feedback analysis, the test remains the same. Look for the critical condition where the rate-of-closure is 40dB/decade. Where conditions approach this level, conduct further analysis and compare phase-compensation alternatives for optimization.

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–20dB/decade to the high-frequency limit of the unity-gain axis.

RATE-OF-CLOSURE VARIES WITH 1/β

The stability conditions of the Figure 12 circuit depend on the particular feedback loop or the combination of elements that are in control at the intercept point. For the lowest-frequency filter cutoff frequencies illustrated, the op amp's bypass capacitor takes control before the intercept and defines the relevant feedback conditions. Because the 1/β curve follows the unity axis at the upper end, you can guarantee stability by ensuring that the op amp be unity-gain stable. For higher-frequency cutoff frequencies, the 1/β transition moves toward the gain-magnitude curve of the op amp. Circuit response cannot move beyond this limit, so the op amp roll-off becomes the upper boundary of filter operation.

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Utilizing these various feedback conditions and a unity-gain-stable op amp, you can design a composite circuit that fulfills its primary stability requirement over the entire

that of the op amp, as the two previous examples demonstrate. Without a wide-bandwidth multiplier, 1/β would begin to rise near the higher-frequency intercepts and increase the rate-of-closure. The OPA111 avoids this complication when using the MEY03-1 multiplier by maintaining a dominant op amp pole.

Other applications may involve feedback peaking and op amps that are not unity-gain stable-log amps and active filters, for example. For these and other variations requiring feedback analysis, the test remains the same. Look for the critical condition where the rate-of-closure is 40dB/decade. Where conditions approach this level, conduct further analysis and compare phase-compensation alternatives for optimization.

REFERENCES

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INCREASING INA117 DIFFERENTIAL INPUT RANGE

By R. Mark Stitt (602) 746-7445

The INA117 is a monolithic difference amplifier with the unique ability to accept up to ±200V common-mode input signals while operating on standard ±15V power supplies. Because the gain of the INA117 is set at 1V/V, and because the output would saturate into the rails at about ±12V, the maximum specified differential input range is ±10V.

Since the common-mode input range is ±200V, it makes sense that some designers would also like to use the part for differential inputs greater than ±10V. Figure 1 shows the recommended circuit. Adding resistors to the input may seem simpler, but there are some problems with that approach.

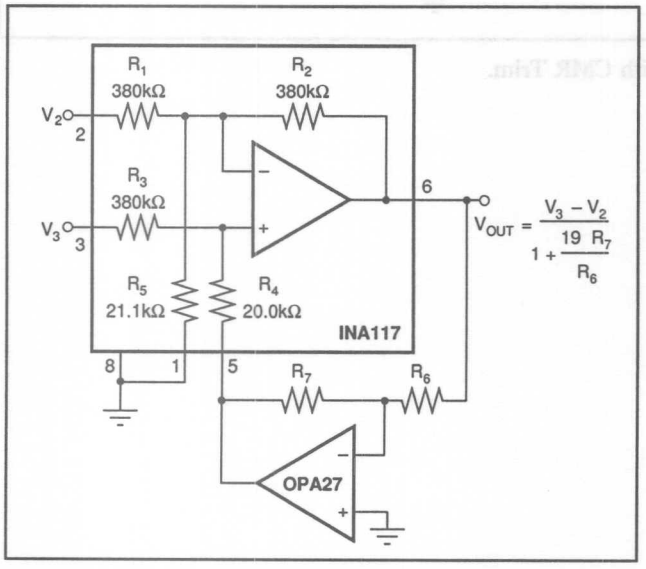

FIGURE 1. INA117 with Increased Differential Input Range.

The performance of the INA117 depends on extremely precise resistor matching (0.005% for 86dB CMR). Resistors added to the input must be adjusted to at least this accuracy to maintain high performance. Both gain error and CMR must be adjusted. Maintaining 86dB CMR over temperature requires 1ppm/°C resistor TCR tracking. Significant resistance added external to the INA117 would require the same performance.

By using the circuit shown in Figure 1, internal resistor matching is preserved, and the INA117 CMR and CMR drift with temperature are maintained. Gain can be set independently of CMR by adjusting the inverter resistors, R_6, R_7. Gain drift is preserved so long as R_6 and R_7 track with temperature. Furthermore, noise at the output is improved by the gain reduction factor whereas, it is unchanged with the other approach.

To understand how the circuit works, consider the INA117 to be a four-input summing amplifier as shown in Figure 2.

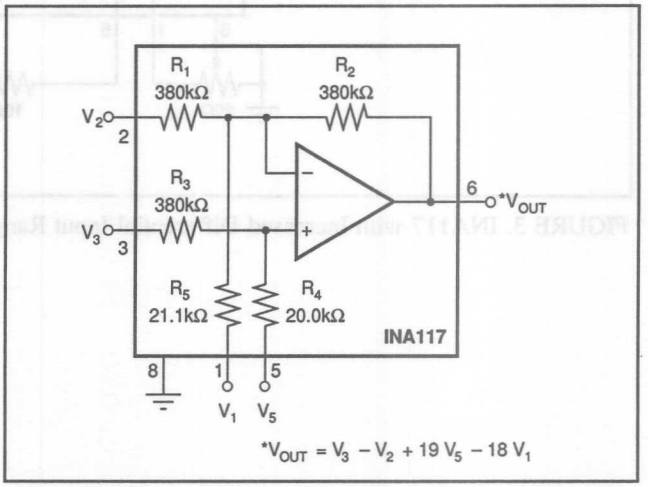

FIGURE 2. INA117 Shown as a Four-Input Summing Amplifier.

CMR is preserved and the gain is reduced if a small portion of the output signal is inverted and fed back to pin 5 with V_1 set to zero (V_1 grounded).

Where: $V_{OUT} = V_3 - V_2 + 19 \bullet V_5 - 18 \bullet V_1$

If, $V_5 = -V_{OUT} \bullet R_7/R_6$, then

$$V_{OUT} = \frac{V_3 - V_2}{1 + \frac{19 \bullet R_7}{R_6}}$$

SELECTED-GAIN EXAMPLES

GAIN (V/V)	R_7 (kΩ)	R_6 (kΩ)
1/2	1.05	20.0
1/4	3.16	20.0
1/5	4.22	20.0

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If CMR adjustment is desired, add a 10Ω fixed resistor and a 20Ω pot as shown in Figure 3. Adjust CMR by shorting together pins 2 and 3 of the INA117 and driving them with a 500Hz square wave while observing the output on a scope. Using a square wave rather than a sine wave allows the AC signal to settle out so that the DC CMR can be seen. The CMR trim will change the gain slightly, so trim CMR first, then trim gain with R_6, R_7 if desired.

The INA117 is now available in three standard 8-pin packages: hermetic TO-99, plastic DIP, and the small surface-mount SOIC package.

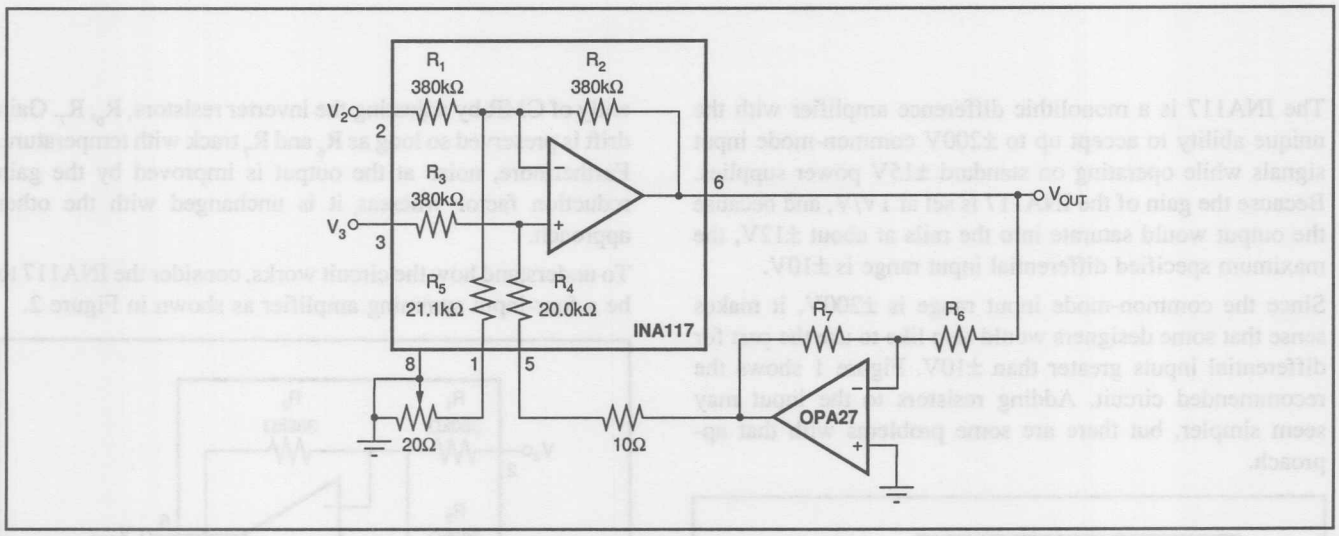

FIGURE 3. INA117 with Increased Differential Input Range with CMR Trim.

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AC COUPLING INSTRUMENTATION AND DIFFERENCE AMPLIFIERS

FEATURING CIRCUITS FOR:

INA117 ±200V DIFFERENCE AMPLIFIER • INA106-BASED ±100V DIFFERENCE AMPLIFIER • INA105 AND INA106 G = 1, 10 DIFFERENCE AMPLIFIERS • INA101, INA102, INA103, INA110, INA120 INSTRUMENTATION AMPLIFIERS

By R. Mark Stitt (602) 746-7445

The need to glean AC signals from DC in the presence of common-mode noise frequently occurs in signal conditioning applications. AC coupling to an instrumentation amplifier (IA) or difference amplifier can be used to accurately extract the AC signal while rejecting DC and common-mode noise.

Adding capacitors and resistors to AC couple the inputs of an instrumentation amplifier or difference amplifier seems like an obvious approach for AC coupling, but it has problems. The DC restoration circuits shown in this bulletin have the same transfer function but without the foibles.

Common-mode rejection of a difference amplifier depends on extremely precise matching of input source impedance. Adding RC networks to the inputs of either an IA or a difference amplifier can significantly degrade the CMR, especially for AC inputs. Even if the CMR is trimmed, maintaining performance over temperature can be a problem.

The DC restoration circuits shown solve this problem by placing a low-pass network in the feedback to the reference pin of the IA or difference amplifier. The low-pass pole translates into a high-pass function as referred to the input with f_{-3dB} = Gain/2•π•R•C. The Gain term refers to the Gain from the reference pin to the output of the IA or difference amplifier. The selection guide shows this Gain term as the "High-pass multiplier".

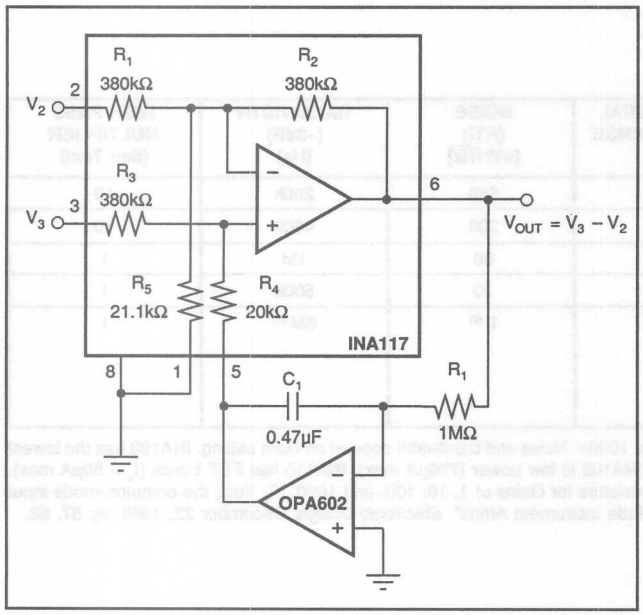

FIGURE 1. AC-Coupled INA117.

The DC-restored INA117 is shown in Figure 1. With the values shown, the high-pass zero is ≈6.5Hz.

The INA117BM has a CMR of 86dB min. If improved CMR is required for the DC restored INA117, use the circuit shown in Figure 2. Since the trim resistors are small, they will not degrade the stability or drift performance of the INA117.

The INA117 has a common-mode input range and differential offset range of up to ±200V. If a lower common-mode and differential offset range of ±100V is acceptable, the INA106 can be used for lower noise and twice the small signal bandwidth (400kHz vs 200kHz).

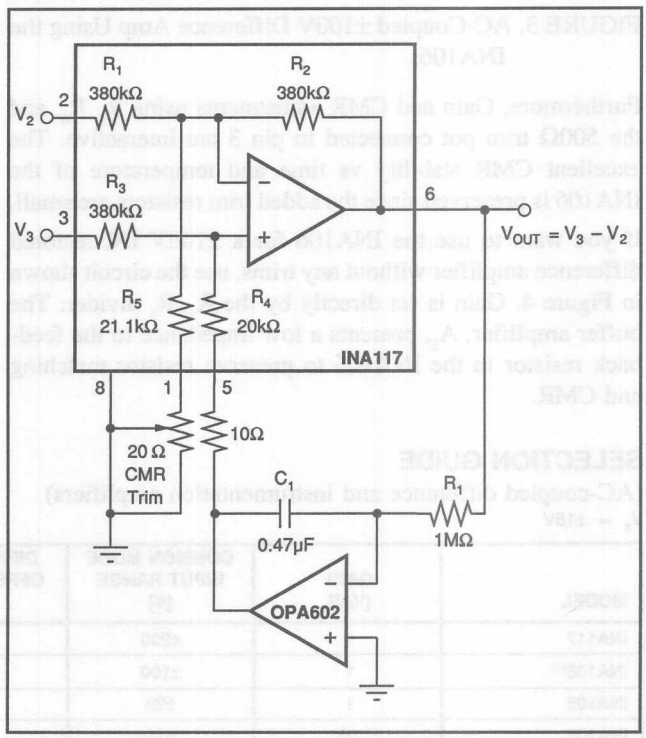

FIGURE 2. AC-Coupled INA117 with CMR Trim.

The simplest circuit for the DC-restored INA106 is shown in Figure 3. The INA106 is reversed from its normal Gain-of-10 configuration. The 100kΩ, 10kΩ resistors form a 11/1 voltage divider on the input so that ±100V at pins 1 and 5 are divided down to less than ±10V at the op amp inputs. The R_5, R_6 network provides the proper feedback Gain for an overall unity-gain transfer function. Since the precise resistor matching of the INA106 is disturbed by the R_5, R_6 network this circuit requires trims for both CMR and Gain.

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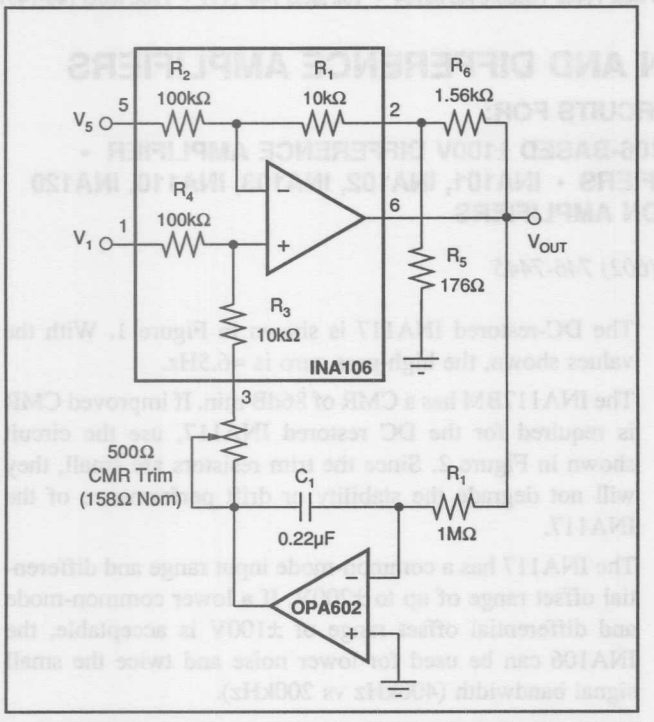

FIGURE 3. AC-Coupled ±100V Difference Amp Using the INA106.

Furthermore, Gain and CMR adjustments using R_5, R_6, and the 500Ω trim pot connected to pin 3 are interactive. The excellent CMR stability vs time and temperature of the INA106 is preserved since the added trim resistors are small.

If you want to use the INA106 for a ±100V DC-restored difference amplifier without any trims, use the circuit shown in Figure 4. Gain is set directly by the R_5, R_6 divider. The buffer amplifier, A_2, presents a low impedance to the feedback resistor in the INA106 to preserve resistor matching and CMR.

When using the DC restored ±100V difference amplifier shown in Figure 4, no trims are required for good CMR. However, the circuit shown in Figure 5 may be used to fine trim CMR if desired. Since the added trim resistors are small, they will not degrade the stability or drift of the INA106.

DC restoration can be used with any of the standard IAs shown in the table using the same technique as shown in Figure 6. Since all of these IAs use unity-Gain difference amplifiers, the high-pass multiplier is unity.

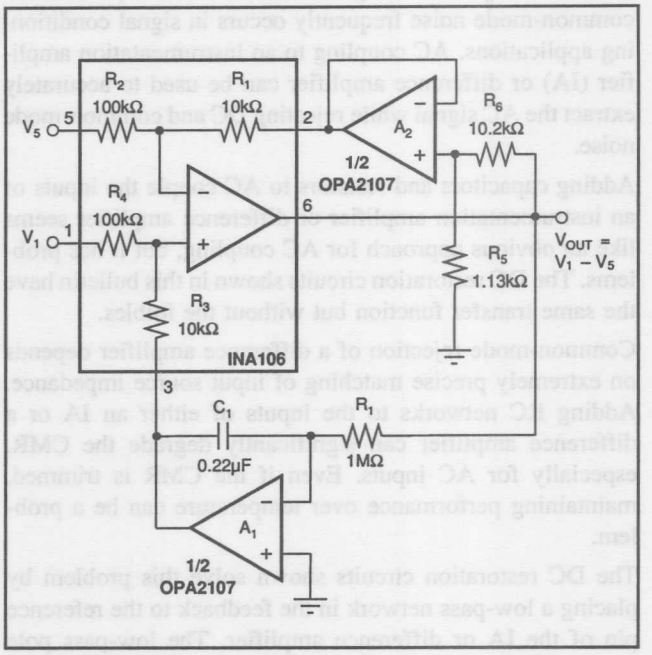

FIGURE 4. AC-Coupled ±100V Difference Amp Using the INA106 Requires No Trims.

SELECTION GUIDE

(AC-coupled difference and instrumentation amplifiers)

V_S = ±15V

MODEL	GAIN [V/V]	COMMON MODE INPUT RANGE [V]	DIFFERENTIAL OFFSET RANGE [V]	NOISE (RTI) [nV/√Hz]	BANDWIDTH (–3dB) [Hz]	HIGH PASS MULTIPLIER (See Text)
INA117	1	±200	±200	550	200k	19
INA106[1]	1	±100	±100	300	400k	10
INA105	1	±20	±10	60	1M	1
INA106	10	±11	±1	30	500k	1
INA101 INA102 INA103 INA110 INA120	[2]	±7 [3]	±10	1 [2]	6M [2]	1

NOTES (1) Reverse-connected, see figures 3,4, and 5. (2) Gain is adjustable from 1 to 1000+. Noise and bandwidth depend on Gain setting. INA103 has the lowest noise: 1nV/√Hz, Gain = 1000. INA103 has the highest bandwidth: 6MHz, Gain = 1. INA102 is low power (750µA max). INA110 has FET inputs (I_B = 50pA max). INA101 has lowest drift (.25µV/°C max). INA120 is a lower IQ INA101 with internal resistors for Gains of 1, 10, 100, and 1000. (3) Yes!, the common-mode input range of standard IAs is only about ±7V with ±10V V_{OUT}; see "Extended Common-Mode Instrument Amps", *Electronic Design*, December 22, 1988, pp 67, 68.

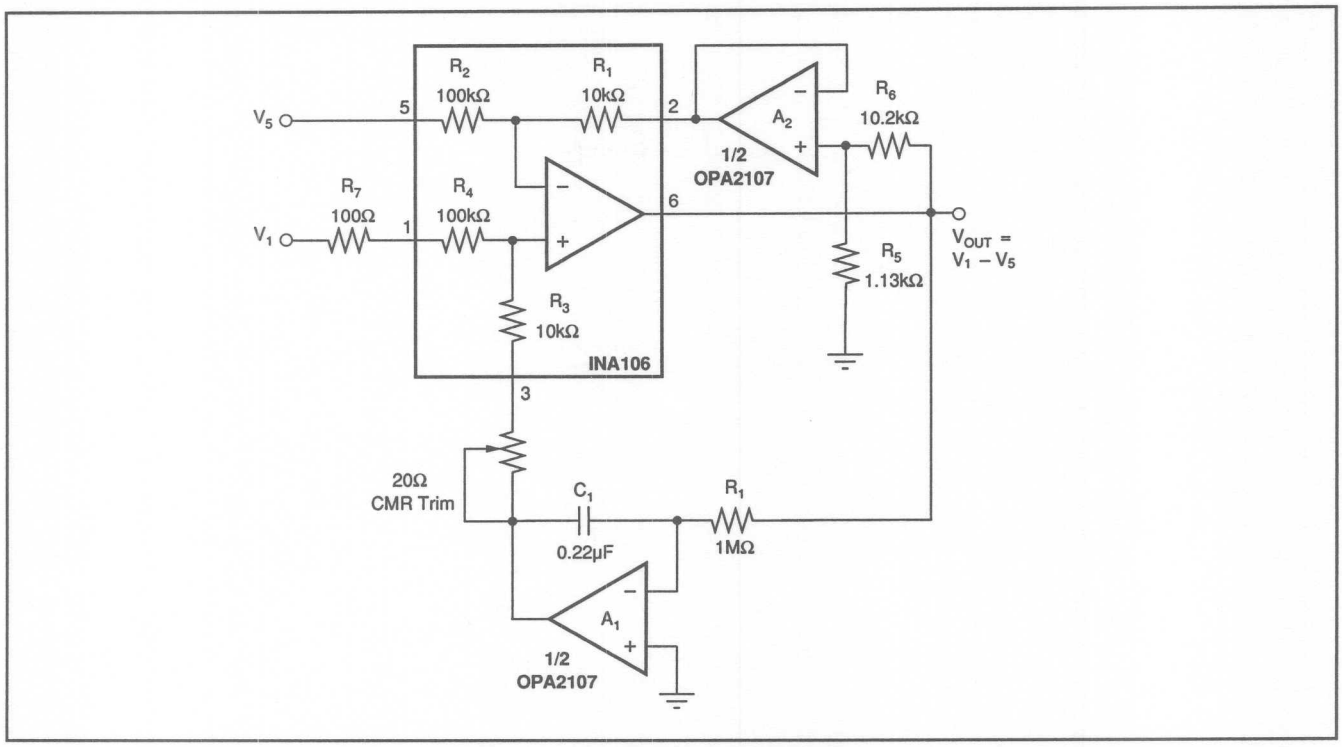

FIGURE 5. AC-Coupled ±100V Difference Amp Uses the INA106. Has CMR Trim.

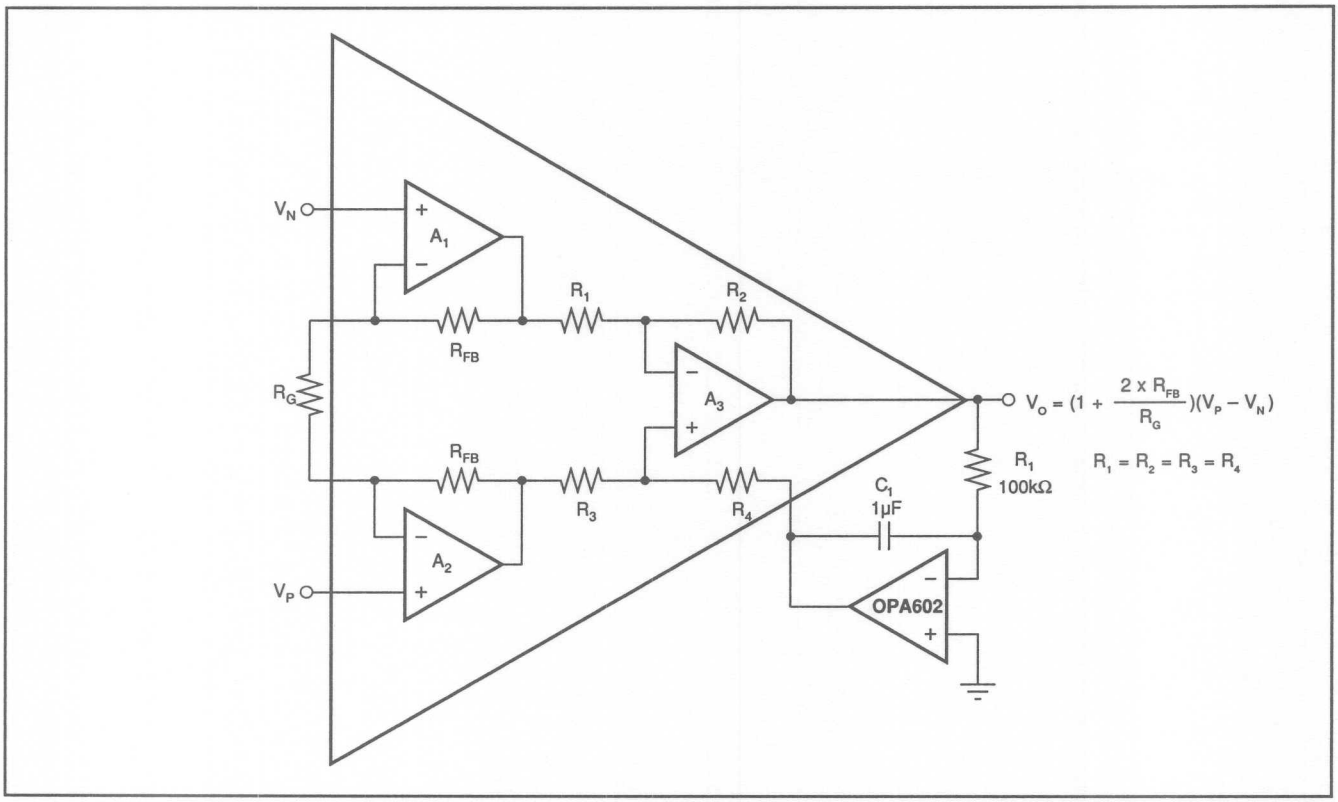

FIGURE 6. General AC-Coupled IA Circuit

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±200V DIFFERENCE AMPLIFIER WITH COMMON-MODE VOLTAGE MONITOR

By Art Gass and R. Mark Stitt (602) 746-7445

The INA117 is a monolithic difference amplifier with the unique ability to accept up to ±200V common-mode input signals while operating on standard ±15V power supplies. Using on-chip high-voltage resistor dividers, the INA117 rejects common-mode signals up to ±200V and translates a 0V to ±10V differential input signal to a 0V to ±10V ground-referenced output signal.

In some applications it is also necessary to monitor the common-mode level of the input signal. A common-mode level monitor can be implemented with the addition of an external op amp or two. Even though standard signal level op amps are used, the circuit remains protected for momentary common-mode or differential overloads up to ±500V.

If precision is not required, the circuit shown in Figure 1 can be used to monitor the common-mode voltage with a maximum error of about ±5V. This implementation actually monitors the common-mode level of the INA117 noninverting input (pin 3). The circuit works by measuring the current in reference pins 1 and 5, which are normally connected to ground. Amplifier A_1 forces the reference pins to a virtual ground through feedback resistors $R_6 + R_7$. The normal operation of the INA117 is unaffected since its reference pins are connected to virtual ground. Resistors R_3 and R_4 in the INA117 form a voltage divider so that the top of R_4 is at $V_3/20$. Feedback of the op amp in the INA117 forces the voltage of its inverting input to be equal to its noninverting input so that the top of resistor R_5 is also at $V_3/20$. The common mode level of V_3 is therefore related to the current flowing out of pins 1 and 5.

$$I_{1+5} = (V_3/20)/(R_4 \parallel R_5)$$

If

$$R_6 + R_7 = R_4 \parallel R_5$$

then

$$A_{1\,OUT} = -V_3/20.$$

Where

I_{1+5} = total current flowing out of INA117 pins 1 and 5 [A]

$R_4 \parallel R_5$ = parallel combination of R_4 and R_5 [Ω]

$R_4 \parallel R_5 = (R_4 \cdot R_5)/(R_4+R_5)$, nominally 10.27kΩ

$A_{1\,OUT}$ = A_1 output voltage [V]

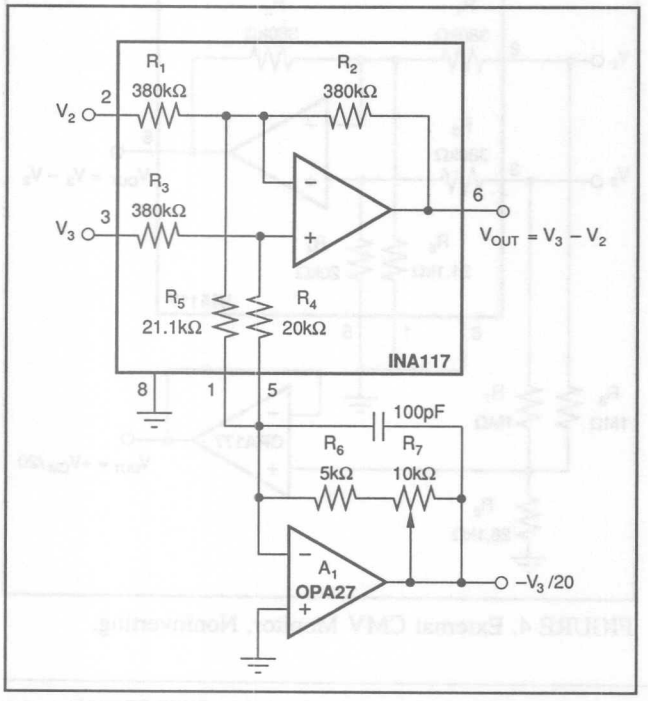

FIGURE 1. INA117 with V_3 Common-Mode Voltage Monitor.

The signal is scaled by 1/20 so the output of A_1 does not exceed its maximum of ±10V with common-mode inputs of ±200V. If smaller maximum common-mode voltages are to be monitored, the value of $R_6 + R_7$ can be increased for more gain.

Although the resistor ratios in the INA117 are accurately laser trimmed, the absolute resistor values can vary by as much as ±25%. For better accuracy, the circuit must be calibrated. To calibrate the gain, short pins 2 and 3 of the INA117 to ground, offset adjust A_1 for 0V at its output, connect pins 2 and 3 to a known V_{REF} (such as +10V or +100V), and adjust R_7 for an A_1 output of $-V_{REF}/20$.

By definition, the true common-mode input voltage of the INA117 is $(V_2 + V_3)/2$. The actual common-mode voltage can be monitored with the addition of a second op amp as shown in Figure 2. The second op amp is connected to sum the $-V_3/20$ output of A_1 at a gain of –1V/V with the $V_3 - V_2$ output of the INA117 at a gain of –1/40V/V to produce an output of $V_{CM}/20$.

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Calibrate the Figure 2 circuit as before, adjusting R_7 for an A_2 output of $V_{REF}/20$. Then, ground pin 3 of the INA117, connect pin 2 to +10V and trim R_9 for 0.025V at the output of A_2. If resistors R_8, R_9, and R_{10} accurately ratio match, adjustment of R_9 is unnecessary.

Of course, if connection of additional components to the INA117 inputs is acceptable, the circuits shown in Figures 3 and 4 can be used to monitor the common-mode input voltage. With these circuits, calibration is not required if accuracy commensurate with the tolerance of R_6, R_7, and R_8 is acceptable. As before, either R_7 or R_8 can be omitted to monitor the common-mode voltage of just one input. If R_7 or R_8 is omitted, double the value of R_6.

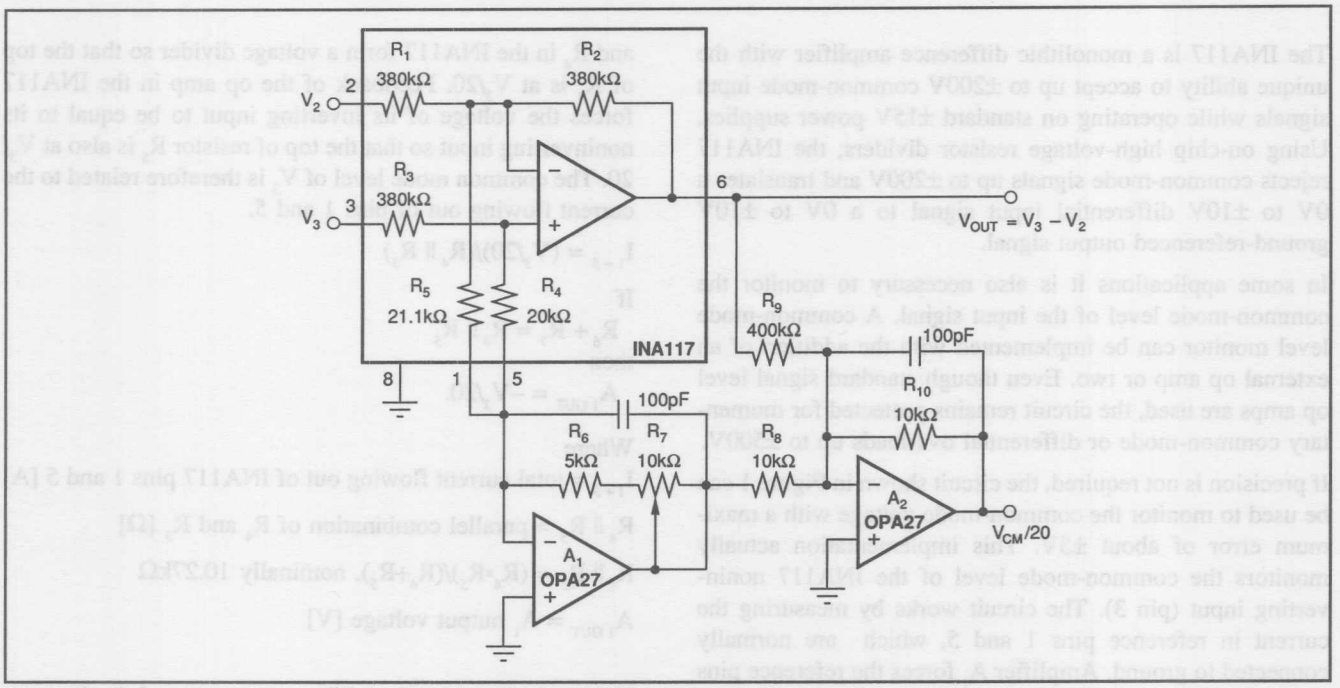

FIGURE 2. INA117 with True Common-Mode Voltage Monitor.

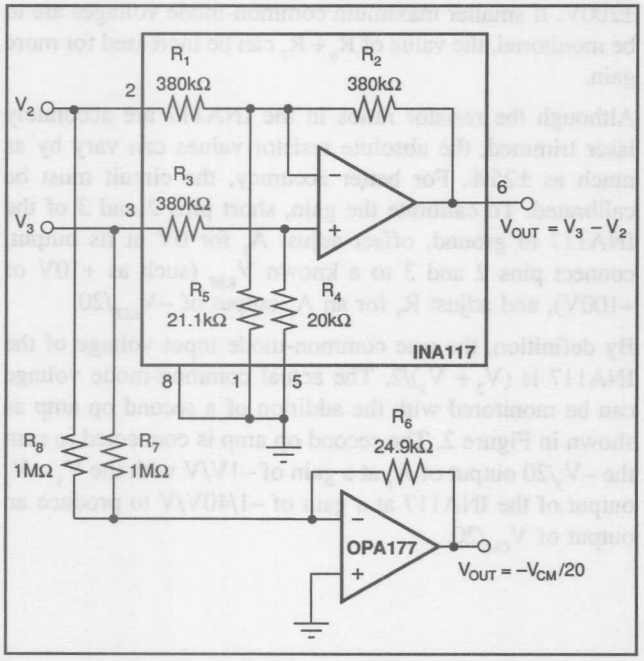

FIGURE 3. External CMV Monitor, Inverting.

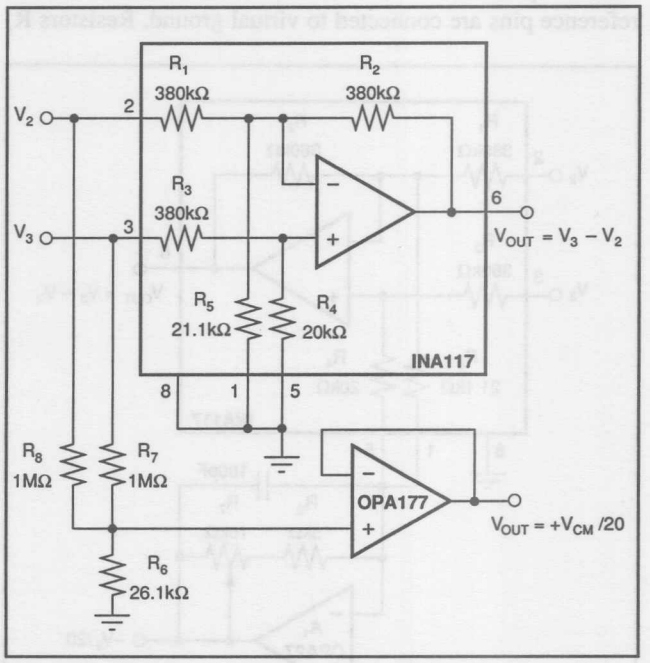

FIGURE 4. External CMV Monitor, Noninverting.

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INPUT OVERLOAD PROTECTION FOR THE RCV420 4–20MA CURRENT-LOOP RECEIVER

By R. Mark Stitt and David Kunst (602) 746-7445

Because of its immunity to noise, voltage drops, and line resistance, the 4–20mA current loop has become the standard for analog signal transmission in the process control industry. The RCV420 is the first one-chip solution for converting a 4–20mA signal into a precision 0–5V output. Although the on-chip current sensing resistor is designed to tolerate moderate overloads, it can be damaged by large overloads which can result from short circuits in the current loop. Complete input protection from short circuits to voltages of 50V or more can be afforded with the addition of the relatively simple circuitry shown in this bulletin.

The complete protected 4–20mA current loop receiver circuit is shown in Figure 1. The RCV420 is connected for a 0–5V output with a 4–20mA current sink input. For a 4–20mA current source input, connect the input to pin 3 instead of pin 1. An on-board precision +10.0V buried zener voltage reference in the RCV420 is used to offset the span (for 0V out with 4mA in) via pin 12. It can also be used for powering external circuitry such as the voltage dividers used to set the underrange/overrange comparator thresholds.

An LM193 dual voltage comparator is used to detect underrange and overrange conditions at the output of the RCV420. The LM193 is designed to operate from a single power supply with an input common-mode range to ground. In this application the LM193 is operated from a single +15V power supply for input common-mode range compatibility with the RCV420 output. The open-collector LM193 comparator outputs are connected through 10kΩ pull-up resistors to a +5V supply for compatibility with TTL and similar logic families.

The RCV420 has a gain of 0.3125V/mA and a 4mA span offset (a 4mA–20mA input produces a 0V–5V output). Under input open circuit conditions (0mA input), the output of the RCV420 goes to –1.25V. To level-shift the output up, for a minimum of 0V at the comparator inputs, it is summed with the 10.0V voltage reference through the 10kΩ, 1.27kΩ resistor network. The table below shows selected operating points for the RCV420 input/output and the comparator input.

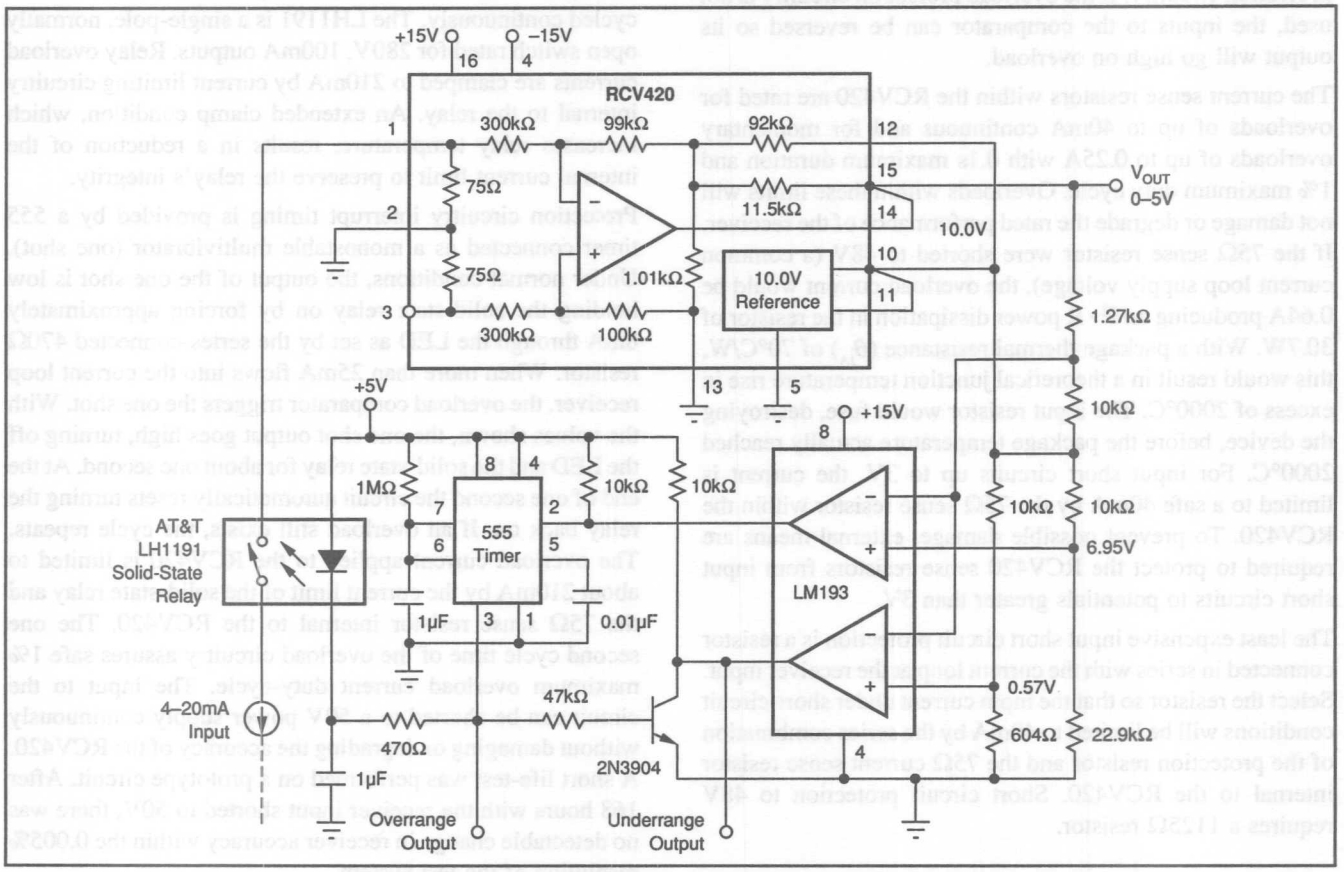

FIGURE 1. Input Protected RCV420.

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SELECTED OPERATING POINTS FOR RCV420 AND COMPARATORS

RCV420 INPUT (mA)	RCV420 OUTPUT (V)	COMPARATOR INPUT [1] (V)
0	–1.250	+0.017
2	–0.625	+0.572
4	0.000	1.269
20	5.000	5.563
25	6.563	6.950
36	10.000	10.000

NOTE: (1) From the 10kΩ, 1.27kΩ summing network.

The underrange comparator threshold is set at 0.57V by the 10kΩ, 604Ω resistor divider connected to the 10.0V reference. The comparator output goes high when the input to the current loop receiver goes below 2mA. The underrange output is TTL compatible.

The overrange comparator threshold is set at 6.95V by the 10kΩ, 22.9kΩ resistor divider connected to the 10.0V reference. The output of the overrange comparator goes low when the input to the current loop receiver exceeds 25mA.
With a 36mA current loop input, the overrange comparator input is 10V. For a 36mA overload set-point, the overrange resistor divider can be eliminated by connecting the overload comparator input directly to the 10.0V reference output of the RCV420.

The overrange comparator is connected so its output will go low on overrange to trigger the ensuing active overload protection circuitry. If the overload protection circuitry is not used, the inputs to the comparator can be reversed so its output will go high on overload.

The current sense resistors within the RCV420 are rated for overloads of up to 40mA continuous and for momentary overloads of up to 0.25A with 0.1s maximum duration and 1% maximum duty cycle. Overloads within these limits will not damage or degrade the rated performance of the receiver. If the 75Ω sense resistor were shorted to 48V (a common current loop supply voltage), the overload current would be 0.64A producing an $I^2 \cdot R$ power dissipation in the resistor of 30.7W. With a package thermal resistance (θ_{JA}) of 70°C/W, this would result in a theoretical junction temperature rise in excess of 2000°C. The input resistor would fuse, destroying the device, before the package temperature actually reached 2000°C. For input short circuits up to 3V, the current is limited to a safe 40mA by the 75Ω sense resistor within the RCV420. To prevent possible damage, external means are required to protect the RCV420 sense resistors from input short circuits to potentials greater than 3V.

The least expensive input short circuit protection is a resistor connected in series with the current loop at the receiver input. Select the resistor so that the input current under short-circuit conditions will be limited to 40mA by the series combination of the protection resistor and the 75Ω current sense resistor internal to the RCV420. Short circuit protection to 48V requires a 1125Ω resistor.

$$R_{PROTECTION} = (V_S/0.040) - 75\ (\Omega)$$

The problem with using a series resistor for input overload protection is the added voltage drop in the input current loop. A 1125Ω protection resistor in series with the 75Ω internal current sense resistor would result in a 24V drop at 20mA full scale input. In most applications the additional 24V burden can not be tolerated.

Another input protection scheme which can be used when only a small series voltage drop can be tolerated is to use a 0.032A fast-acting fuse (such as Littlefuse 217000 series, type F) in series with the current loop. This fuse adds negligible voltage drop to the current loop, and blows in less than 0.1s with an overload of 128mA or more. The problem with a fuse is that it must be replaced when it blows, and the cost of maintenance can be very high.

The active protection scheme shown in this application overcomes the disadvantages of resistor and fuse protection. It uses a solid-state relay for current loop interruption. After an interrupt time delay designed to provide a safe 1% maximum overload duty-cycle, the circuit resets automatically. The LH1191 solid-state relay used has a maximum on resistance of 33Ω which adds less than 0.1V of burden to the current loop at 20mA full scale input. Low receiver burden allows longer field wiring (with higher resistance) for remote sensors, and extra compliance for "intrinsically safe" barriers or other series connected receivers.

The solid-state relay is ideal for the resetable protection task. It is inexpensive as compared to a mechanical relay (less than $1.00), and because it is solid-state, it will not "wear out" if cycled continuously. The LH1191 is a single-pole, normally open switch rated for 280V, 100mA outputs. Relay overload currents are clamped to 210mA by current limiting circuitry internal to the relay. An extended clamp condition, which increases relay temperature, results in a reduction of the internal current limit to preserve the relay's integrity.

Protection circuitry interrupt timing is provided by a 555 timer connected as a monostable multivibrator (one shot). Under normal conditions, the output of the one shot is low holding the solid-state relay on by forcing approximately 8mA through the LED as set by the series-connected 470Ω resistor. When more than 25mA flows into the current loop receiver, the overload comparator triggers the one shot. With the values shown, the one shot output goes high, turning off the LED and the solid-state relay for about one second. At the end of one second the circuit automatically resets turning the relay back on. If an overload still exists, the cycle repeats. The overload current applied to the RCV420 is limited to about 210mA by the current limit of the solid-state relay and the 75Ω sense resistor internal to the RCV420. The one second cycle time of the overload circuitry assures safe 1% maximum overload current duty-cycle. The input to the circuit can be shorted to a 50V power supply continuously without damaging or degrading the accuracy of the RCV420. A short life-test was performed on a prototype circuit. After 168 hours with the receiver input shorted to 50V, there was no detectable change in receiver accuracy within the 0.005% resolution of the test system.

Since the overload protection circuitry interrupts the current loop, a logic gate is needed to prevent a false indication of open circuit. The 2N3904 transistor is wire-ORed to the underrange comparator output, assuring it will go high only during actual underload conditions. The 1μF capacitor connected to the 470Ω relay drive resistor delays relay turn-on to prevent possible logic race conditions which could produce a false underrange output logic "sliver". The capacitor can be omitted if this is not a concern.

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EXTENDING THE COMMON-MODE RANGE OF DIFFERENCE AMPLIFIERS

By R. Mark Stitt (602) 746-7445

Extending the common-mode range of difference amplifiers allows their use in a wider variety of reduced power-supply applications.

The INA117 has a specified common-mode input range of ±200V when operating on standard ±15V power supplies. At power-supply voltages above ±13V, the INA117 input range is limited to ±200V by the power capabilities of its internal input resistors. On reduced power supplies, the input range is limited by the common mode input range of the internal op amp.

The linear common-mode input range of the internal op amp extends to within 3V of its power supply voltage. For example, with a ±15V power supply, the common-mode input range of the internal op amp is ±12V. Because the INA117 internal resistor network divides the input by 20, the actual input range of the INA117 would be 20 • (±12V), or 240V, for ±15V power supplies. Similarly, reducing the power supply voltage to ±6V will limit the input common-mode voltage to ±60V.

There are two approaches to boosting the common-mode input range for reduced power supply applications: Offsetting the common-mode range by a fixed amount, and dynamically adjusting the common-mode range to follow the input common-mode signal.

OFFSETTING THE INPUT COMMON-MODE RANGE WITH A CONSTANT VOLTAGE

In many applications, the common-mode signal range is known and the common-mode input range of the difference amplifier can be adjusted to coincide with the required range. For example, the ±60V common-mode range of the INA117 operating on ±6V supplies could be shifted to range from +0V to +120V, or +50V to +170V.

To offset the common-mode range, the reference connection of the difference amplifier is connected to an offsetting voltage, V_X, instead of ground. With the reference connected to an offsetting potential, a second difference amplifier must be used to refer the output back to ground.

One way to offset the input voltage is to connect the reference pins 1 and 5 to the negative supply voltage as shown in Figure 1. Another possibility is to derive the offset voltage from a zener diode connected to the negative power supply as shown in Figure 2. In either case, the total common-mode range of the INA117 is unchanged and shifted by –19 • (V_X).

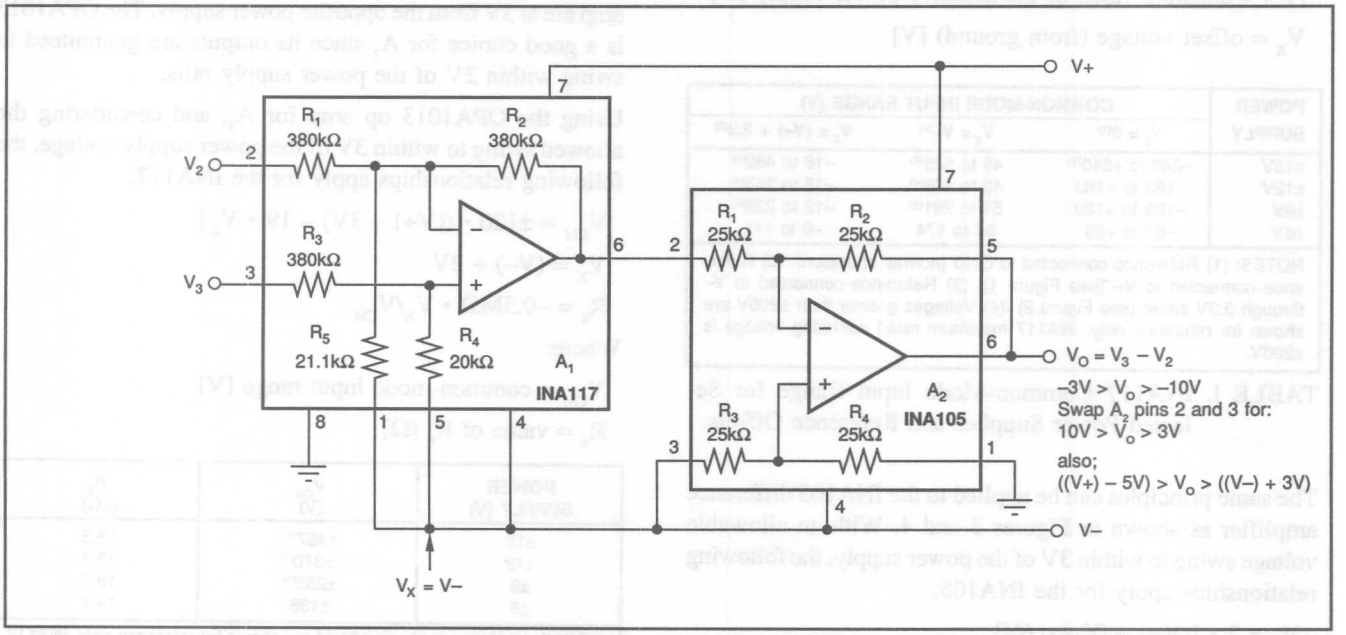

FIGURE 1. Offsetting the INA117 Common-Mode Input Range Using the Negative Power Supply as a Reference.

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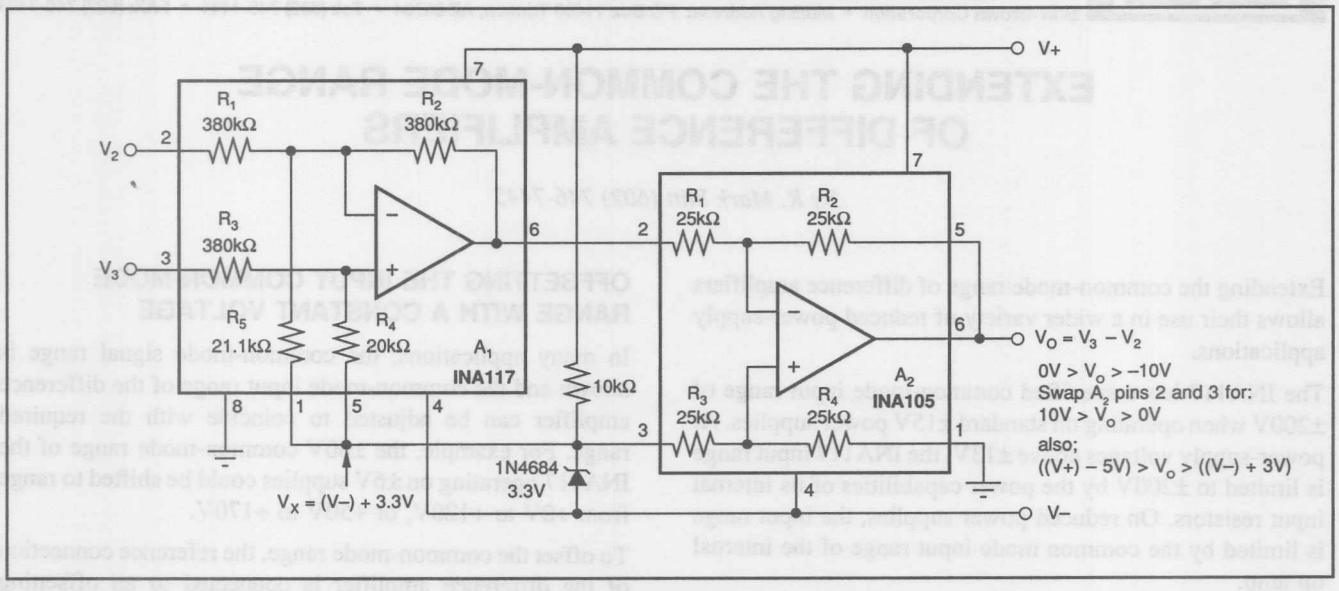

FIGURE 2. Offsetting the INA117 Common-Mode Input Range with a Zener Reference.

Since the input voltage can swing to within 3V of the power supply, the following relationships apply for the INA117:

$$V_R = 20 \cdot [(V+) + |V-| - 6V]$$

$$V_L = 20 \cdot [(V-) + 3V] - 19 \cdot V_X$$

$$V_H = V_R - V_L$$

Where

V_R = total common-mode range [V]

V_L = minimum common-mode signal [V]

V_H = maximum common-mode signal [V]

V+, V– = positive, negative power supply [V]

|V–| = absolute value of the negative power supply [V]

V_X = offset voltage (from ground) [V]

POWER SUPPLY	COMMON-MODE INPUT RANGE (V)		
	V_X = 0[1]	V_X = V–[2]	V_X = (V–) + 3.3[3]
±15V	–240 to +240[4]	45 to 525[4]	–18 to 462[4]
±12V	–180 to +180	48 to 408[4]	–15 to 345[4]
±9V	–120 to +120	51 to 291[4]	–12 to 228[4]
±6V	–60 to +60	54 to 174	–9 to 111

NOTES: (1) Reference connected to GND (normal operation). (2) Reference connected to V– (see Figure 1). (3) Reference connected to V– through 3.3V zener (see Figure 2). (4) Voltages greater than ±200V are shown for reference only. INA117 maximum rated operating voltage is ±200V.

TABLE I. INA117 Common-Mode Input Range for Selected Power Supplies and Reference Offsets.

The same principles can be applied to the INA105 difference amplifier as shown in Figures 3 and 4. With an allowable voltage swing to within 3V of the power supply, the following relationships apply for the INA105:

$$V_R = 2 \cdot [(V+) + |V-| - 6V]$$

$$V_L = 2 \cdot [(V-) + 3V] - V_X$$

ADJUSTING THE COMMON MODE RANGE DYNAMICALLY

Another way to boost the common-mode range of a difference amplifier is to drive the reference connection dynamically in response to changes in the input. A circuit to boost the input range of the INA117 is shown in Figure 5. A third amplifier, A_3, along with resistors R_7, R_8, and R_6 is used to derive, invert, and scale the input level presented to the reference connection.

The value for R_6 depends on the power supply voltages and op amp used for A_3. To maximize the common-mode range, R_6 should be selected so the output of A_3 is at its maximum swing limit when the inputs to the difference amplifier op amp are at 3V from the opposite power supply. The OPA1013 is a good choice for A_3 since its outputs are guaranteed to swing within 2V of the power supply rails.

Using the OPA1013 op amp for A_3, and considering the allowed swing to within 3V of the power supply voltage, the following relationships apply for the INA117.

$$V_{CM} = \pm\{20 \cdot ((V+) - 3V) - 19 \cdot V_X\}$$

$$V_X = (V-) + 2V$$

$$R_6 = -0.5M\Omega \cdot V_X/V_{CM}$$

Where:

V_{CM} = common-mode input range [V]

R_6 = value of R_6 [Ω]

POWER SUPPLY (V)	V_{CM} (V)	R_6 (kΩ)
±15	±487[1]	13.3
±12	±370[1]	13.7
±9	±253[1]	13.7
±6	±136	14.7

NOTES: (1) Voltages above ±200V are shown for reference only. INA117 maximum rated operating voltage is ±200V.

TABLE II. INA117 Common-Mode Input Range for Selected Power Supplies Using Figure 5 Circuit.

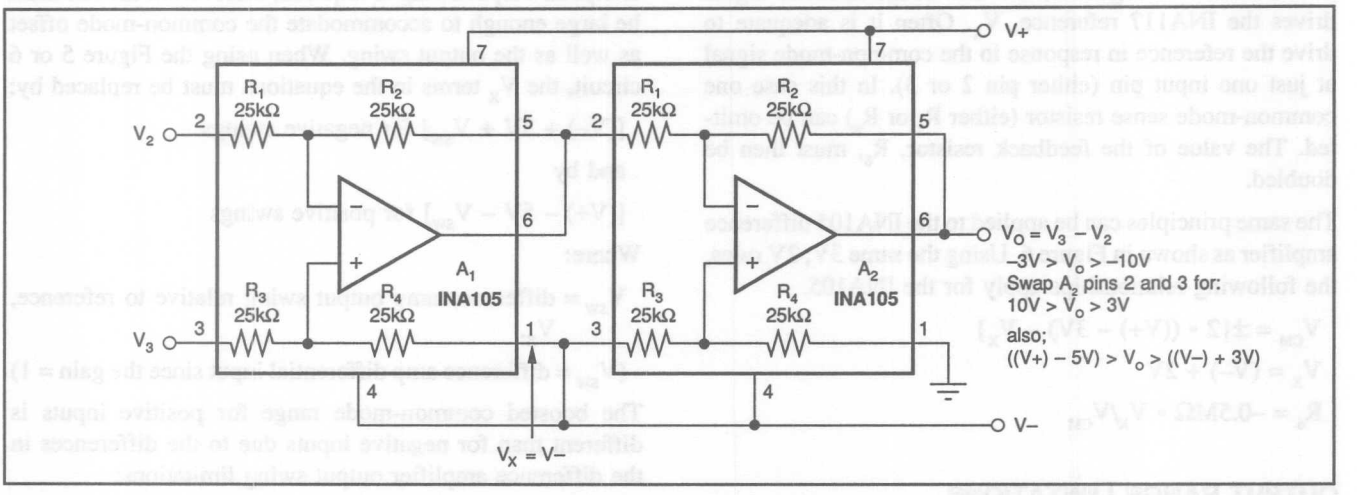

FIGURE 3. Offsetting the INA105 Common-Mode Input Range Using the Negative Power Supply as a Reference.

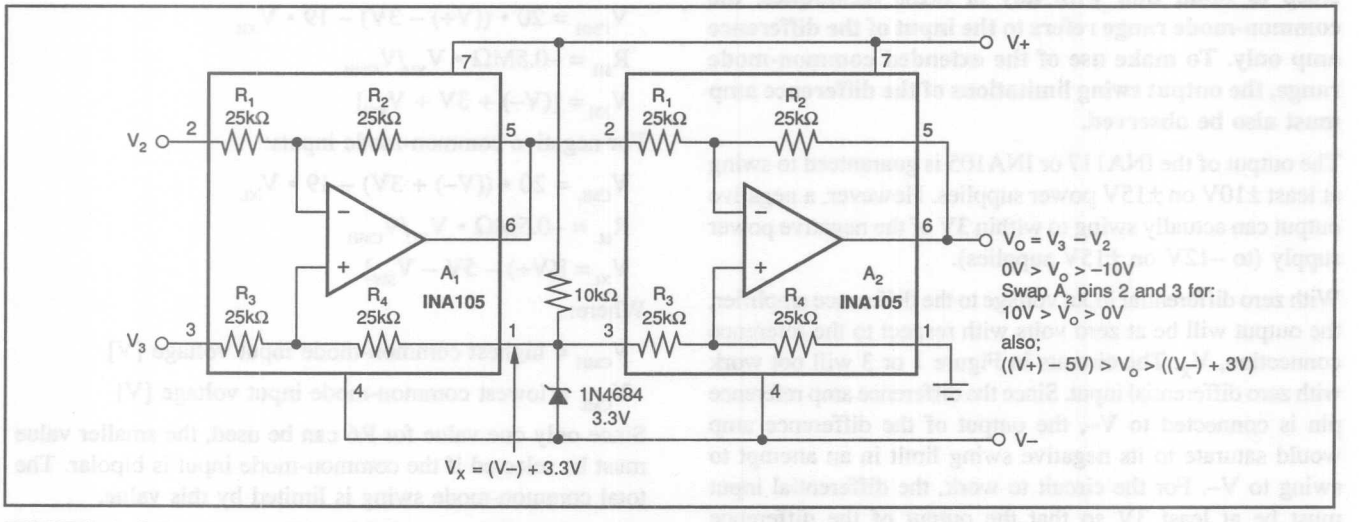

FIGURE 4. Offsetting the INA105 Common-Mode Input Range with a Zener Reference.

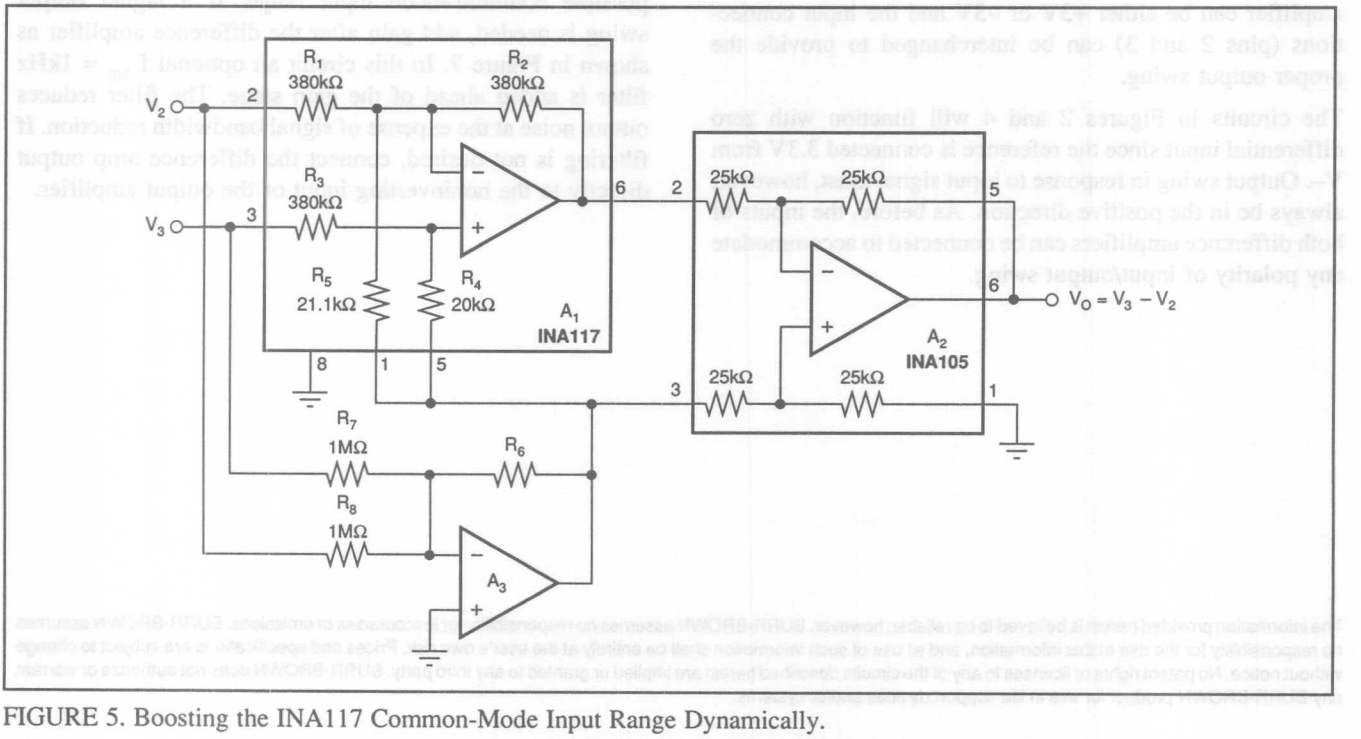

FIGURE 5. Boosting the INA117 Common-Mode Input Range Dynamically.

at just one input pin (either pin 2 or 3). In this case one common-mode sense resistor (either R_7 or R_8) can be omitted. The value of the feedback resistor, R_6, must then be doubled.

The same principles can be applied to the INA105 difference amplifier as shown in Figure 6. Using the same 3V, 2V rules, the following relationships apply for the INA105.

$$V_{CM} = \pm\{2 \bullet ((V+) - 3V) - V_X\}$$

$$V_X = (V-) + 2V$$

$$R_6 = -0.5M\Omega \bullet V_X/V_{CM}$$

OUTPUT RANGE LIMITATIONS

Keep in mind that with any of these techniques, the common-mode range refers to the input of the difference amp only. To make use of the extended common-mode range, the output swing limitations of the difference amp must also be observed.

The output of the INA117 or INA105 is guaranteed to swing at least ±10V on ±15V power supplies. However, a negative output can actually swing to within 3V of the negative power supply (to –12V on ±15V supplies).

With zero differential input voltage to the difference amplifier, the output will be at zero volts with respect to the reference connection, V_X. The circuits in Figure 1 or 3 will not work with zero differential input. Since the difference amp reference pin is connected to V–, the output of the difference amp would saturate to its negative swing limit in an attempt to swing to V–. For the circuit to work, the differential input must be at least 3V so that the output of the difference amplifier is at 3V from V–. The input to the difference amplifier can be either +3V or –3V and the input connections (pins 2 and 3) can be interchanged to provide the proper output swing.

The circuits in Figures 2 and 4 will function with zero differential input since the reference is connected 3.3V from V–. Output swing in response to input signal must, however, always be in the positive direction. As before, the inputs of both difference amplifiers can be connected to accommodate any polarity of input/output swing.

as well as the output swing. When using the Figure 5 or 6 circuit, the V_X terms in the equations must be replaced by:

$[(V-) + 3V + V_{SW}]$ for negative swings

and by

$[(V+) - 5V - V_{SW}]$ for positive swings

Where:

V_{SW} = difference amp output swing relative to reference, V_X.

(V_{SW} = difference amp differential input since the gain = 1)

The boosted common-mode range for positive inputs is different than for negative inputs due to the differences in the difference amplifier output swing limitations:

For positive common-mode inputs:

$$V_{CMH} = 20 \bullet ((V+) - 3V) - 19 \bullet V_{XH}$$

$$R_{6H} = -0.5M\Omega \bullet V_{XH}/V_{CMH}$$

$$V_{XH} = [(V-) + 3V + V_{SW}]$$

For negative common-mode inputs:

$$V_{CML} = 20 \bullet ((V-) + 3V) - 19 \bullet V_{XL}$$

$$R_{6L} = -0.5M\Omega \bullet V_{XL}/V_{CMH}$$

$$V_{XL} = [(V+) - 5V - V_{SW}]$$

Where:

V_{CMH} = highest common-mode input voltage [V]

V_{CML} = lowest common-mode input voltage [V]

Since only one value for R6 can be used, the smaller value must be selected if the common-mode input is bipolar. The total common-mode swing is limited by this value.

Reducing the difference amplifier output swing increases the possible common-mode input range. If a higher output swing is needed, add gain after the difference amplifier as shown in Figure 7. In this circuit an optional f_{-3dB} = 1kHz filter is added ahead of the gain stage. The filter reduces output noise at the expense of signal bandwidth reduction. If filtering is not desired, connect the difference amp output directly to the noninverting input of the output amplifier.

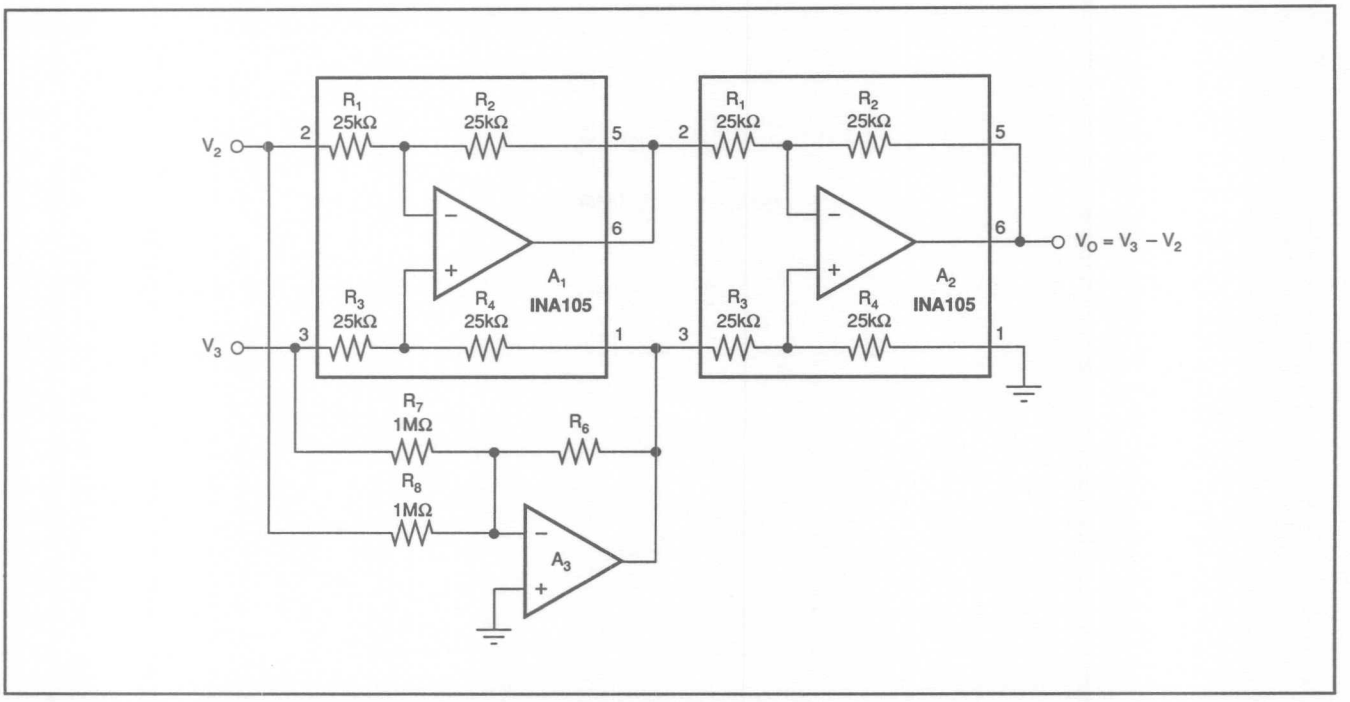

FIGURE 6. Boosting the INA105 Common-Mode Input Range Dynamically.

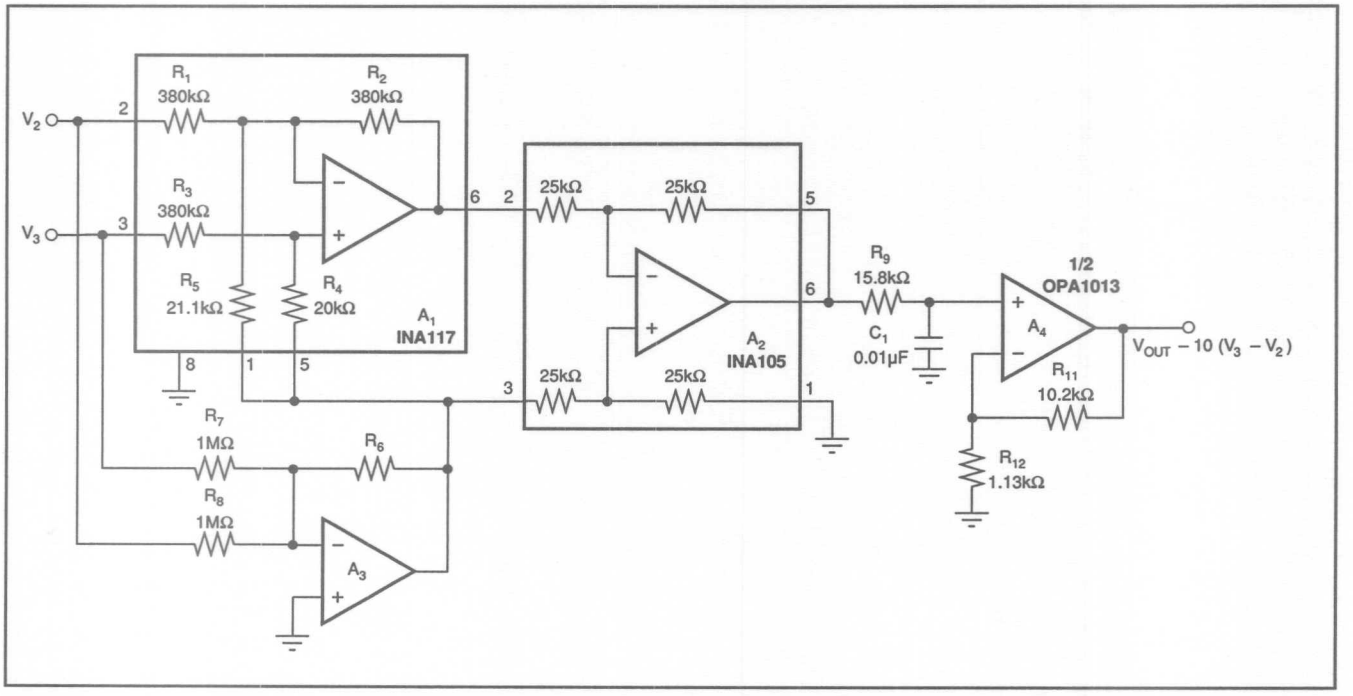

FIGURE 7. Boosted Common-Mode Input Range INA117 with Noise Filtering and Added Gain after the 2nd Difference Amplifier to Further Extend INA117 Common-Mode Input Range.

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BOOST AMPLIFIER OUTPUT SWING WITH SIMPLE MODIFICATION

By R. Mark Stitt and Rod Burt (602) 746-7445

In many applications it is desirable for the output of an amplifier to swing close to its power supply rails. Most amplifiers only guarantee an output swing of ±10V to ±12V when operating on standard ±15V power supplies. With the addition of four resistors and a pair of garden-variety transistors, the INA105 or INA106 difference amplifiers can be modified to provide nearly a full ±15V output swing on ±15V supplies.

Figure 1 shows the modified circuit for the INA105. The combined INA105 quiescent current and output current flowing from its power-supply pins drives external transistors Q_1 and Q_2 through base-emitter connected resistors R_3 and R_4. Q_1 and Q_2 are arranged as common-emitter amplifiers in a gain of approximately 1.7V/V (1 + 750Ω/1kΩ) so that the INA105's output only needs to swing about ±9V for a ±15V swing at the buffer output. Figure 4 shows the boosted INA105 driving a 1kΩ load to within a fraction of a volt of its ±15V power supplies. Figure 4 is a multiple exposure scope photo showing the composite amplifier output and the power-supply voltages.

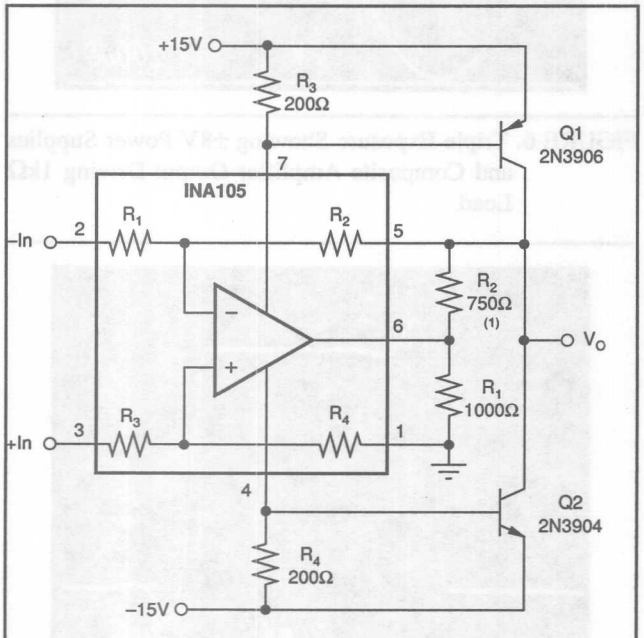

FIGURE 1. External Transistors Q_1 and Q_2 Add Output Boost so the Difference Amplifier Can Drive Loads Close to Its Power-Supply Rails.

Even though there is gain in the feedback of the INA105, the circuit is stable as shown by the small-signal response of the amplifier as seen in the scope photo, Figure 5. Since a unity-gain difference amplifier operates in a noise gain of two, gain can be added in its feedback loop without causing instability with the following restrictions: 1) the added gain is less than 2V/V, 2) the op amp in the difference amplifier is unity gain stable, and 3) the phase shift added by the gain buffer is low at the unity gain frequency of the op amp. All stability requirements are met when using the INA105.

To understand the details of the composite amplifier, consider the block diagram, Figure 2. Resistors R_1 and R_2 set the gain of the buffer amplifier A_2. The buffer amplifier is a current-feedback op amp formed from the output transistors in the INA105 and the external transistors, Q_1 and Q_2. The current feedback amplifier gives wide bandwidth and low phase shift. Figure 3 shows one of two complementary current-feedback amplifiers formed from the NPN output transistor in the INA105 and the external PNP transistor, Q_1. This current-feedback amplifier section is active for positive swings of the composite amplifier output. A complementary current-feedback amplifier, using external transistor Q_2, is active for negative output swings of the composite amp.

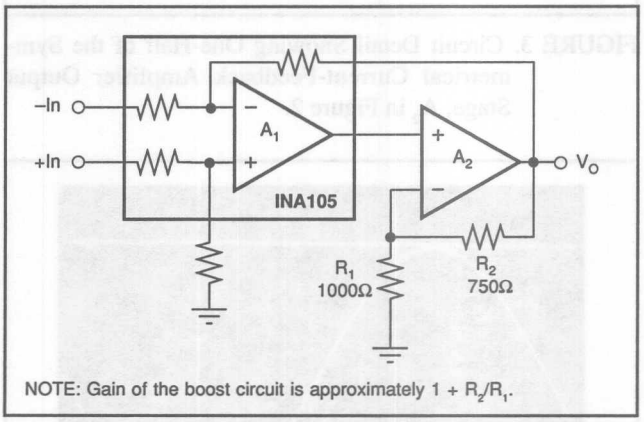

FIGURE 2. Block Diagram Showing Boost Circuit Feedback Arrangement.

Because the maximum gain in the feedback of an INA105 is limited to 2V/V, the boosted circuit works best with power supplies of ±12V or more. The INA105 doesn't have enough output swing on lower supplies to drive a gain-of-2 buffer to the power supply rails. For boosted output swing on lower supplies, consider the INA106 gain-of-10 difference amplifier. Although the op amp in the INA106 is not unity gain stable, the INA106 is stable with added gain in its feedback of up to 3V/V. This allows full output boost on lower voltage supplies. Scope photograph Figure 6 shows the boosted

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showing the composite amplifier output and the power-supply voltages. Scope photograph Figure 7, shows the small signal response of the INA106 with a gain-of-3 feedback buffer.

A word of caution: To obtain the boosted output swing, output protection circuitry was eliminated. There is no current limit in the output buffer. A short circuit at the output may destroy the external output transistors. Still, this simple modification is an effective means to obtain wide output swing.

So long as the stated stability requirements are observed, this technique can be applied to other op amp circuits.

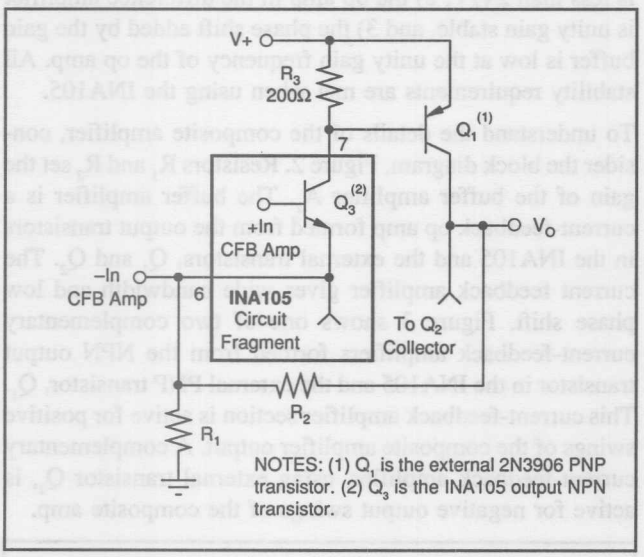

FIGURE 3. Circuit Detail Showing One-Half of the Symmetrical Current-Feedback Amplifier Output Stage, A_2 in Figure 2.

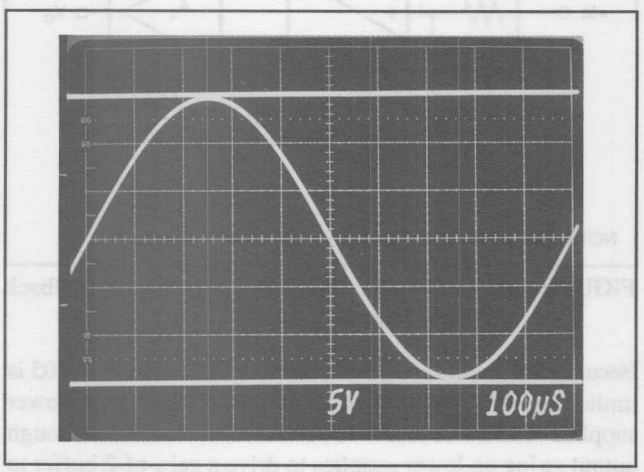

FIGURE 4. Triple Exposure Showing ±15V Power Supplies and Composite Amplifier Output Driving 1kΩ Load.

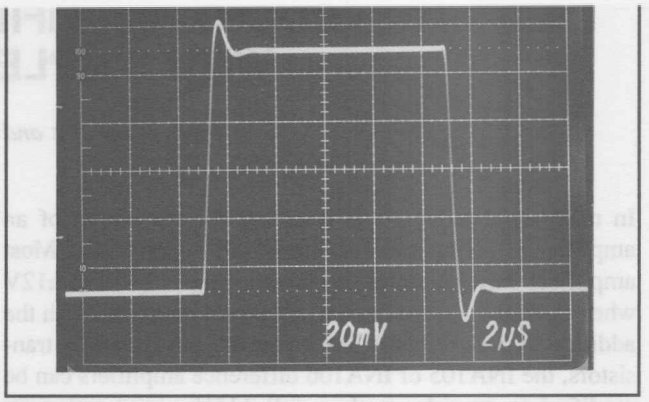

FIGURE 5. Small-Signal Response of Composite Amplifier Using INA105 and Buffer Amplifier with 750Ω, 1kΩ Feedback Resistors.

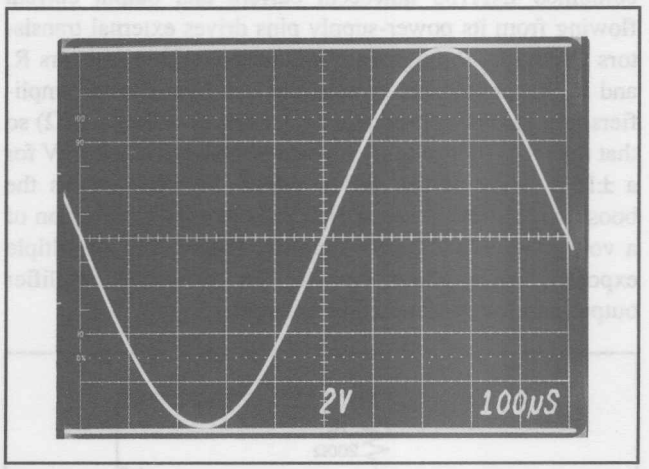

FIGURE 6. Triple Exposure Showing ±8V Power Supplies and Composite Amplifier Output Driving 1kΩ Load.

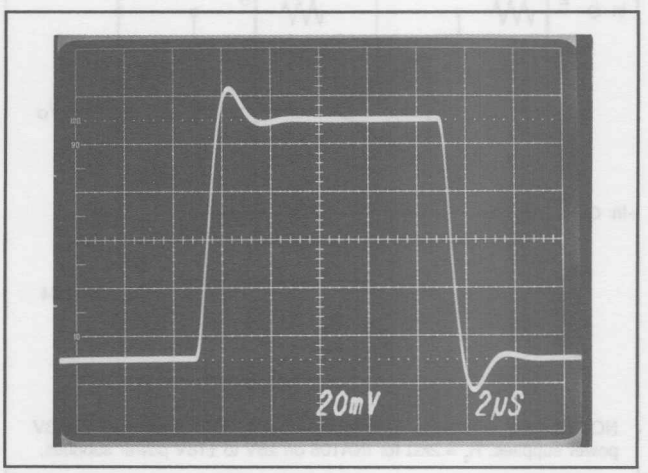

FIGURE 7. Small-Signal Response of Composite Amplifier Using INA106 and Buffer Amplifier with 3kΩ, 1kΩ Feedback Resistors.

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0 TO 20mA RECEIVER USING RCV420

By David Kunst and R. Mark Stitt (602) 746-7445

Many industrial current-loop applications call for conversion of a 0 to 20mA input current into 0 to 5V output. The RCV420 is intended primarily as a complete solution for precise 4 to 20mA to 0 to 5V conversion. But, with the addition of one or two external 1% resistors, the RCV420 can also accurately convert a 0 to 20mA input into a 0 to 5V output.

The recommended hook-up for 0-20mA/0-5V conversion is shown in Figure 1. To reduce the gain from 5V/16mA to 5V/20mA, the internal 75Ω sense resistor is paralleled with a 301Ω, 1% external resistor connected between pins 1 and 2.

Even though the external paralleling resistor has a 1% tolerance, the worst-case gain error of the current-to-voltage conversion will be only 0.5%. This is because the parallel combination of an external 301Ω resistor and the internal 75Ω resistor is dominated by the internal resistor.

A tighter tolerance on the external paralleling resistor would not significantly improve the gain accuracy. This is because the internal 75Ω sense resistor also has a tolerance of 1%. The high gain accuracy of the RCV420 transfer function comes from a fine laser trim of the internal amplifier's gain which compensates for any error in the 75Ω internal sense resistor. So even if the sense resistor were replaced by a resistor of exact value, the gain error could be as much as 1%.

For best common-mode rejection performance, a second 301Ω external resistor should be connected between pins 2 and 3 in parallel with the other internal 75Ω sense resistor. Without it, 86dB CMR would be degraded to about 80dB. If high CMR is not needed, the second resistor shown can be omitted.

To eliminate the offset, used for 4-20mA/0-5V conversion, the "Ref In" (pin 12) must be connected to ground instead of to the 10V reference. The "Ref Out" and "Ref Feedback" (pins 10 and 11) should still be connected together to prevent the reference circuitry from locking-up. Even though the 10.0V reference is not used for span offsetting, it is a precision reference which may be useful for other circuitry.

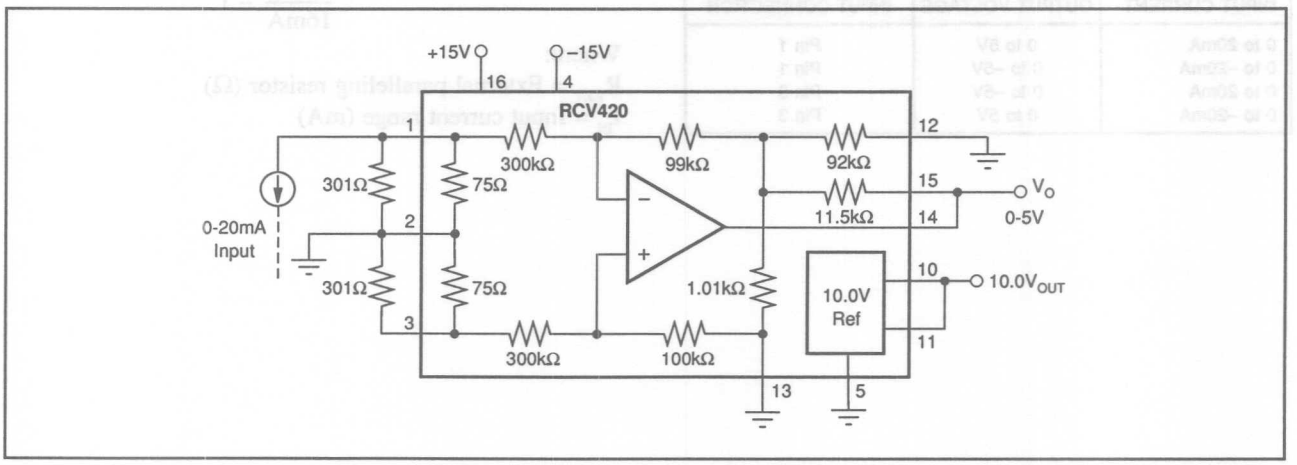

FIGURE 1. 0-20mA/0-5V Receiver Using RCV420.

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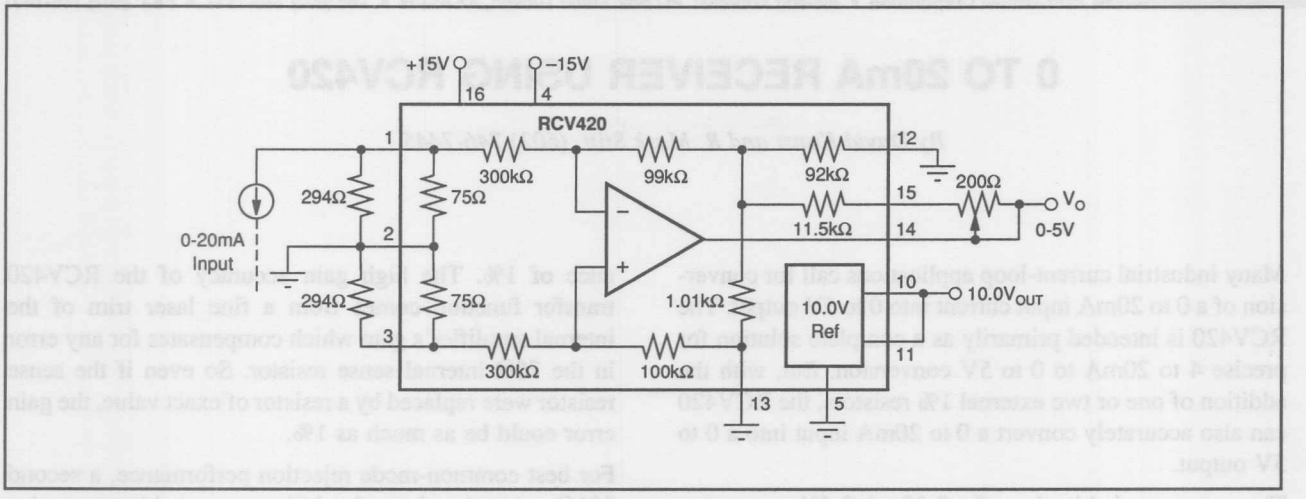

FIGURE 2. Gain Trimmable 0-20mA/0-5V Receiver Using RCV420.

If better gain accuracy is required, use the gain trim circuit shown in Figure 2. This circuit uses a slightly lower value external resistor in parallel with the internal 75Ω sense resistor and a potentiomenter in the feedback for fine trim of gain. Because of its small value, and the action of the "T" network feedback arrangement, the effect of the gain adjust pot on CMR is negligible.

Of course, any mix of input/output polarity can be obtained by connecting the current source input to either pin 1 or 3.

INPUT CURRENT	OUTPUT VOLTAGE	INPUT CONNECTION
0 to 20mA	0 to 5V	Pin 1
0 to –20mA	0 to –5V	Pin 1
0 to 20mA	0 to –5V	Pin 3
0 to –20mA	0 to 5V	Pin 3

Gain-reduction paralleling-resistors for selected gains are shown in the table below.

INPUT RANGE	OUTPUT RANGE	PARALLELING-RESISTOR
0 to 20mA	0 to 5V	301Ω
0 to 50mA	0 to 5V	35.7Ω

In general, to determine the value of the external paralleling resistor:

$$R_{EXT} = \frac{75\Omega}{\frac{I_{IN}}{16mA} - 1}$$

Where:

R_{EXT} = External paralleling resistor (Ω)

I_{IN} = Input current range (mA)

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BOOST INSTRUMENT AMP CMR WITH COMMON-MODE DRIVEN SUPPLIES

By R. Mark Stitt (602) 746-7445

Ever-increasing demands are being placed on instrumentation amplifier (IA) performance. When standard IAs can not deliver the required performance, consider this enhanced version. Dramatic performance improvements can be achieved by operating the input amplifiers of a classical three-op-amp IA from common-mode driven sub-regulated power supplies.

Instrumentation amplifiers are designed to amplify low-level differential signals while rejecting unwanted common-mode signals. One of the most important specifications is common-mode rejection (CMR)—the ability to reject common mode signals. AC CMR is especially important since the common-mode signals are inevitably dynamic—commonly ranging from 60Hz power-line interference to switching-power-supply noise at tens to hundreds of kHz. With common-mode driven sub-regulated supplies, both the AC and DC CMR of the IA can be dramatically improved. Improved AC and DC power supply noise rejection is an added bonus.

At the high gains often required, input offset voltage drift can also be a critical specification. In some applications, the low input offset voltage drift of chopper stabilized op amps might provide the best solution. But, since many of these chopper stabilized op amps are built using low voltage CMOS processes, they can not be operated on standard ±15V power supplies. Operating the chopper stabilized op amps from common-mode-driven, sub-regulated ±5V supplies allows them to be used without restriction in ±15V systems.

THE THREE OP AMP IA

To understand how the technique works, first consider the operation of the three op amp IA shown in Figure 1A. The design consists of an input gain stage driving a difference amplifier.

The difference amplifier consists of op amp A_3 and ratio matched resistors R_1 through R_4. If the resistor ratios R_2/R_1 exactly match R_4/R_3 the difference amplifier will amplify differential signals by a gain of R_2/R_1 while rejecting common-mode signals. The CMR of the difference amplifier will almost certainly be limited by resistor mismatch when a high-performance op amp is used for A_3. A unity-gain difference amplifier requires a difficult 0.01% resistor match for CMR of 86dB.

Since the slightest input source impedance mismatch would degrade the resistor matching of the difference amplifier, a differential input, differential output gain-stage (A_1, A_2, R_{FB1}, R_{FB2}, and R_G) is used ahead of the difference amplifier. The low output-impedance of the of the gain stage preserves difference amplifier resistor matching and maintains the CMR of the difference amplifier. The input amplifiers also provide high input impedance and additional gain.

When designing a high CMR instrumentation amplifier, it is important to use a differential input, differential output amplifier using a single gain-set resistor (see Figure 1A). In the Figure 1A circuit, CMR is independent of resistor matching. Resistor mismatches degrade CMR in the two gain-set-resistor differential in/out amplifier (see Figure 1B).

To understand why CMR is independent of resistor matching in the single gain-set resistor amplifier, consider the Figure 1A circuit. With a common-mode input signal, and no differential input signal, the voltage between V_N and V_P does not change. Therefore the voltage across R_G remains constant and, since no current flows in the op amp inputs, there is no current change in R_{FB1} or R_{FB2}, and the differential output voltage, V_1-V_2, does not change. Ideally then, with a perfect difference amplifier, the common-mode gain is zero and the CMRR is ∞.

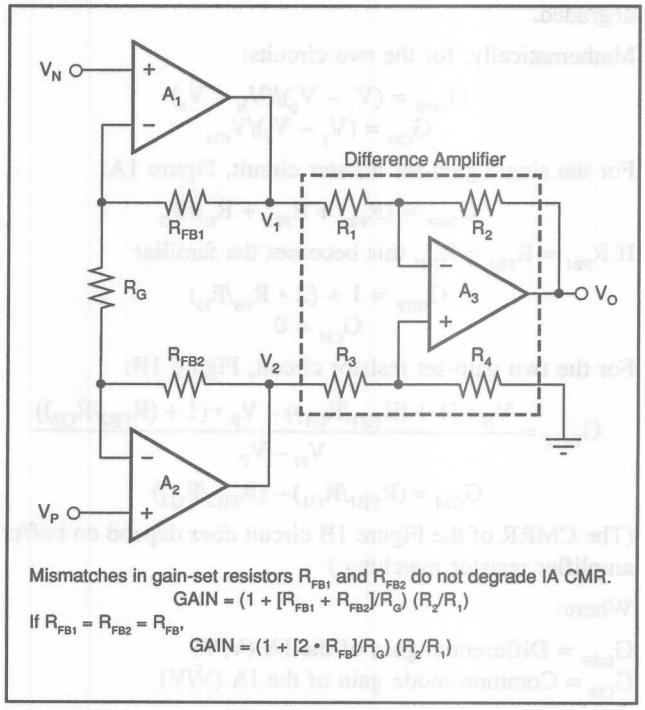

FIGURE 1A. The Three Op-Amp Instrumentation Amplifier.

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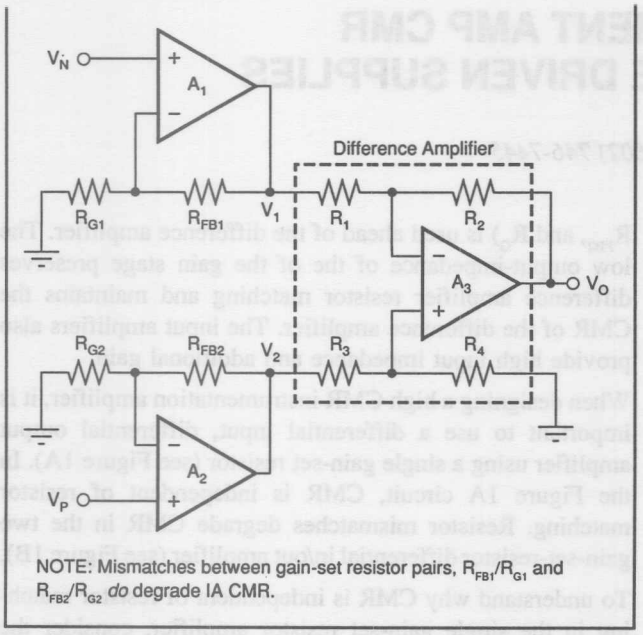


FIGURE 1B. The *Wrong* Way to Make a Three Op-Amp Instrumentation Amplifier.

In the Figure 1B circuit, CMR *does* depend on resistor matching. Common-mode signals will cause different common-mode currents to flow through R_{G1} and R_{G2} if their values are not matched. Then, if the ratio of R_{FB1}/R_{G1} is not exactly equal to the ratio of R_{FB2}/R_{G2}, there *will* be common-mode gain and the CMRR of the instrumentation amplifier *will* be degraded.

Mathematically, for the two circuits:

$$G_{DIFF} = (V_1 - V_2)/(V_N - V_P)$$
$$G_{CM} = (V_1 - V_2)/V_{CM}$$

For the single gain-set resistor circuit, Figure 1A:

$$G_{DIFF} = (R_{FB1} + R_{FB2} + R_G)/R_G$$

If $R_{FB1} = R_{FB2} = R_{FB}$, this becomes the familiar

$$G_{DIFF} = 1 + (2 \bullet R_{FB}/R_G)$$
$$G_{CM} = 0$$

For the two gain-set resistor circuit, Figure 1B:

$$G_{DIFF} = \frac{V_N \bullet (1 + (R_{FB1}/R_{G1})) - V_P \bullet (1 + (R_{FB2}/R_{G2}))}{V_N - V_P}$$

$$G_{CM} = (R_{FB1}/R_{G1}) - (R_{FB2}/R_{G2})$$

(The CMRR of the Figure 1B circuit *does* depend on buffer amplifier resistor matching.)

Where:

G_{DIFF} = Differential gain of the IA (V/V)
G_{CM} = Common-mode gain of the IA (V/V)

See Figures 1A and 1B for V_S and R_S.

Common-mode rejection ratio is the ratio of differential gain to common-mode gain. Adding gain ahead of the difference amplifier increases the CMR of the IA so long as the op amps in the gain stage have better CMR than the difference CMR (e.g. 80dB) at gain = 1 and a much higher CMR at higher gains (e.g. 100dB at gain = 1000).

Most high-performance op amps have better CMR than is available from difference amplifiers. Be careful when selecting an input op amp though; the venerable "741" op amp has a minimum high-grade CMR of 80dB, and the world's most popular op amp[1], the LM324, has a min high-grade CMR of only 70dB. High performance bipolar input op amps have the best CMR. The OPA177 has a min CMR of 130dB. FET input op amps usually don't offer quite as much performance. The Burr-Brown OPA627 comes the closest with a min CMR of 106dB.

LIMITING FACTORS IN IA PERFORMANCE

The DC CMR of a standard IA can be improved by driving the power supply connections of the input op amps from sub-regulated power supplies referenced to the IA common-mode input voltage. Op amp CMR is limited by device mismatch and thermal feedback that occurs as the op amp inputs change relative to its power supplies. If the power supply rails are varied to track the common mode input signal, there is no variation of the inputs relative to the power-supply rails, errors which degrade CMR are largely eliminated, and CMR can be substantially improved.

The AC CMR of the IA is limited by the AC response of the input amplifiers. The outputs of the input amplifiers in the IA follow the common mode input signal. As the frequency of the common-mode signal increases, the loop gain of the input op amps diminishes, and CMR falls off.

For large common-mode signals, the slew rate of the input op amps can limit the ability of the IA to function altogether. This will happen when the maximum rate of change of the common-mode signal exceeds the slew rate limit of the op amp. For a sine wave, the maximum rate of change occurs at the zero crossing and can be derived as follows:

$$V = V_P \bullet \sin(2 \bullet \pi \bullet f \bullet t)$$
$$dV/dt = 2 \bullet \pi \bullet f \bullet V_P \bullet \cos(2 \bullet \pi \bullet f \bullet t)$$

At t = 0,

$$dV/dt = 2 \bullet \pi \bullet f \bullet V_P$$
$$\text{Slew rate limit} = 2 \bullet \pi \bullet f_{MAX} \bullet V_P$$

Where:

V = common-mode voltage vs time (t)
V_P = peak common-mode voltage
Slew rate limit = maximum dV/dt
f_{MAX} = maximum common-mode frequency at amplitude V_P beyond which standard IA fails to function due to slew-rate limit of input op amp.

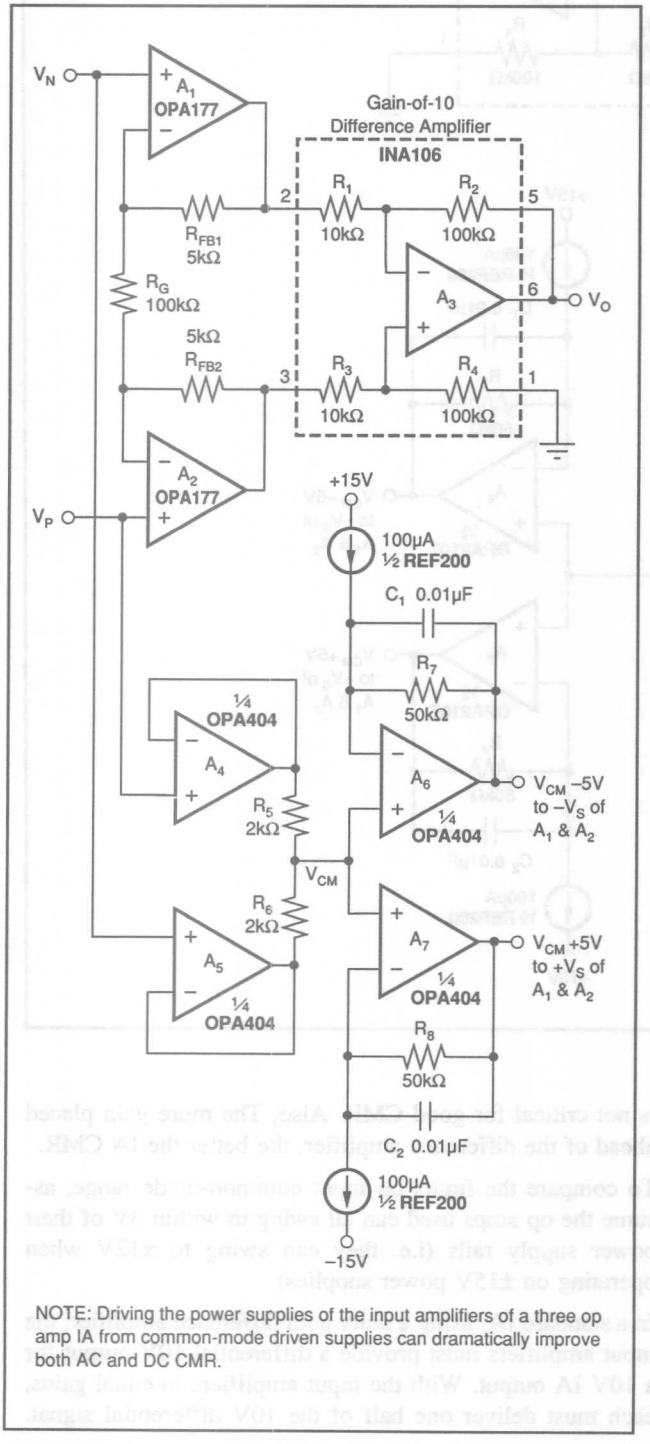
As with DC CMR, AC CMR can be improved by driving the power supply connections of the input op amps from common-mode referenced sub-regulated supplies. Since neither the inputs nor the output of the amplifier change relative to

(1) According to its designer: Frederiksen, Thomas M., *Intuitive IC Op Amps*, National Semiconductor's Technology Series, 1984, back cover.

the power supply rails, nothing within the amplifier moves in response to the common-mode signal. No current flows in the phase compensation capacitors and the phase compensation is therefore defeated for common-mode response.

THE BOOSTED IA

The complete circuit for the enhanced IA is shown in Figure 2. In addition to the three op amp IA, it contains a buffered common-mode voltage generator, and ±5V subregulated power supplies.



NOTE: Driving the power supplies of the input amplifiers of a three op amp IA from common-mode driven supplies can dramatically improve both AC and DC CMR.

FIGURE 2. Boosted Instrumentation Amplifier.

An INA106 gain-of-10 difference amplifier is used for the difference amplifier. The INA106 contains a precision op amp and ratio matched resistors R_1 through R_4 pretrimmed for 100dB min CMR. No critical resistor matching by the user is required to build a precision IA using this approach.

The common-mode signal driving the subregulated supplies is derived from resistor divider network, R_5, R_6. The network is driven from the IA inputs through unity-gain connected op amps A_4 and A_5. These buffer amplifiers persevere the IA's high input impedance. In some applications the impedance of the R_5, R_6 network connected directly to the IA inputs is acceptable and buffer amplifiers A_4 and A_5 can be deleted as shown in Figure 3. The signal at the R_5, R_6 connection of the resistor divider is the average or common-mode voltage of the two IA inputs.

The negative subregulator consists of A_6, R_7, C_1, and a 100µA current source (1/2 of Burr-Brown REF200). Since no current flows in the op amp input, 100µA flows through the 50kΩ resistor, R_7 forcing a –5V drop from the op amp input to its output. The op amp forces the negative input to be at the same potential as its positive input. The result is a a –5V floating voltage reference relative to the op amp noninverting input terminal.

The positive subregulator is the same as the negative subregulation except for the polarity of the current source connection.

The outputs of the positive and negative subregulators are connected to the power supplies of the input op amps A_1 and A_2 only. All other op amps are connected to ±15V power supplies.

COMMON MODE RANGE OF BOOSTED IA

The common-mode input range of the boosted IA is limited by the subregulated supply voltage. The outputs of the subregulator amplifiers, A_6 and A_7 must swing the common-mode voltage plus the subregulator voltage. The smaller the subregulator voltage, the better the common-mode input range. A subregulator voltage of ±5V was chosen because it is low enough to give good input common-mode range while it is high enough to allow full performance from almost any op amp.

COMMON MODE RANGE OF BOOSTED IA IS AS GOOD AS STANDARD IA

The common-mode input range of the boosted instrumentation amplifier is as good as that of most integrated circuit IAs. It might seem that the subregulated supplies would reduce the IA's common-mode range. But because the boosted IA uses a gain-of-10 difference amplifier rather than a unity gain difference amplifier its common mode range is not limited by the input amplifiers. The common-mode input range of both the boosted IA and the standard IA is about ±7V.

That's right. With a 10V output, the common mode input range of a standard IA is only about ±7V, not ±10V as many have been incorrectly led to believe.

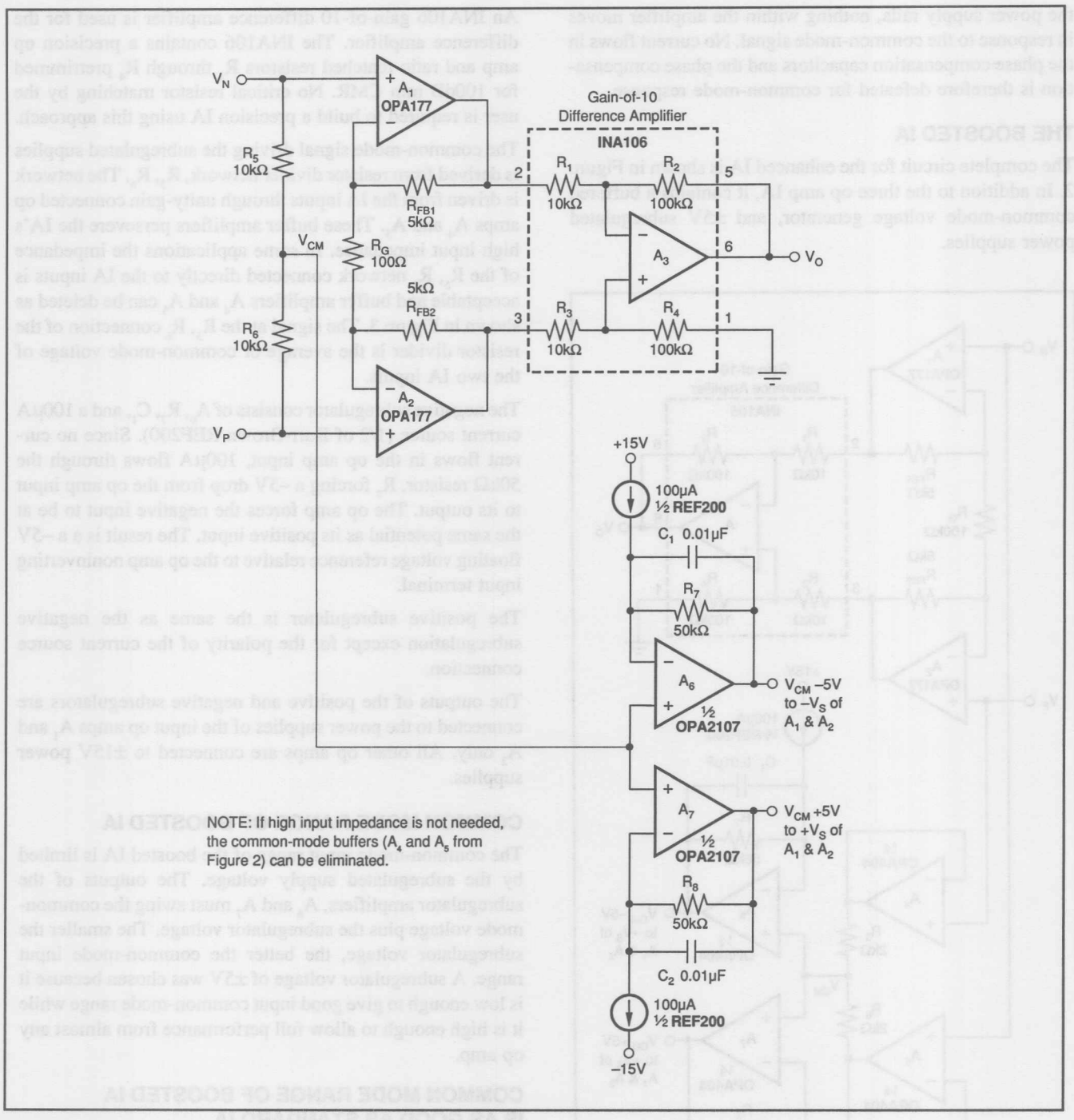


FIGURE 3. Simplified Boosted Instrumentation Amplifier.

The common-mode swing of a standard IA is limited by the output swing of the input amplifiers. The common mode range of the boosted IA is limited by the output swing of the subregulator amplifiers.

Standard IAs use unity gain difference amplifiers for practical reasons. Since standard IAs are designed for general applications, they must be adjustable to unity gain. Because it would be difficult for the user to maintain the resistor ratio matching necessary for good difference amplifier CMR, a fixed unity gain difference amplifier is provided. Gain adjustment is made with the input amplifiers, where matching is not critical for good CMR. Also, The more gain placed ahead of the difference amplifier, the better the IA CMR.

To compare the limits on input common-mode range, assume the op amps used can all swing to within 3V of their power supply rails (i.e. they can swing to ±12V when operating on ±15V power supplies).

In a standard IA, using a unity gain difference amplifier, the input amplifiers must provide a differential 10V output for a 10V IA output. With the input amplifiers in equal gains, each must deliver one half of the 10V differential signal.

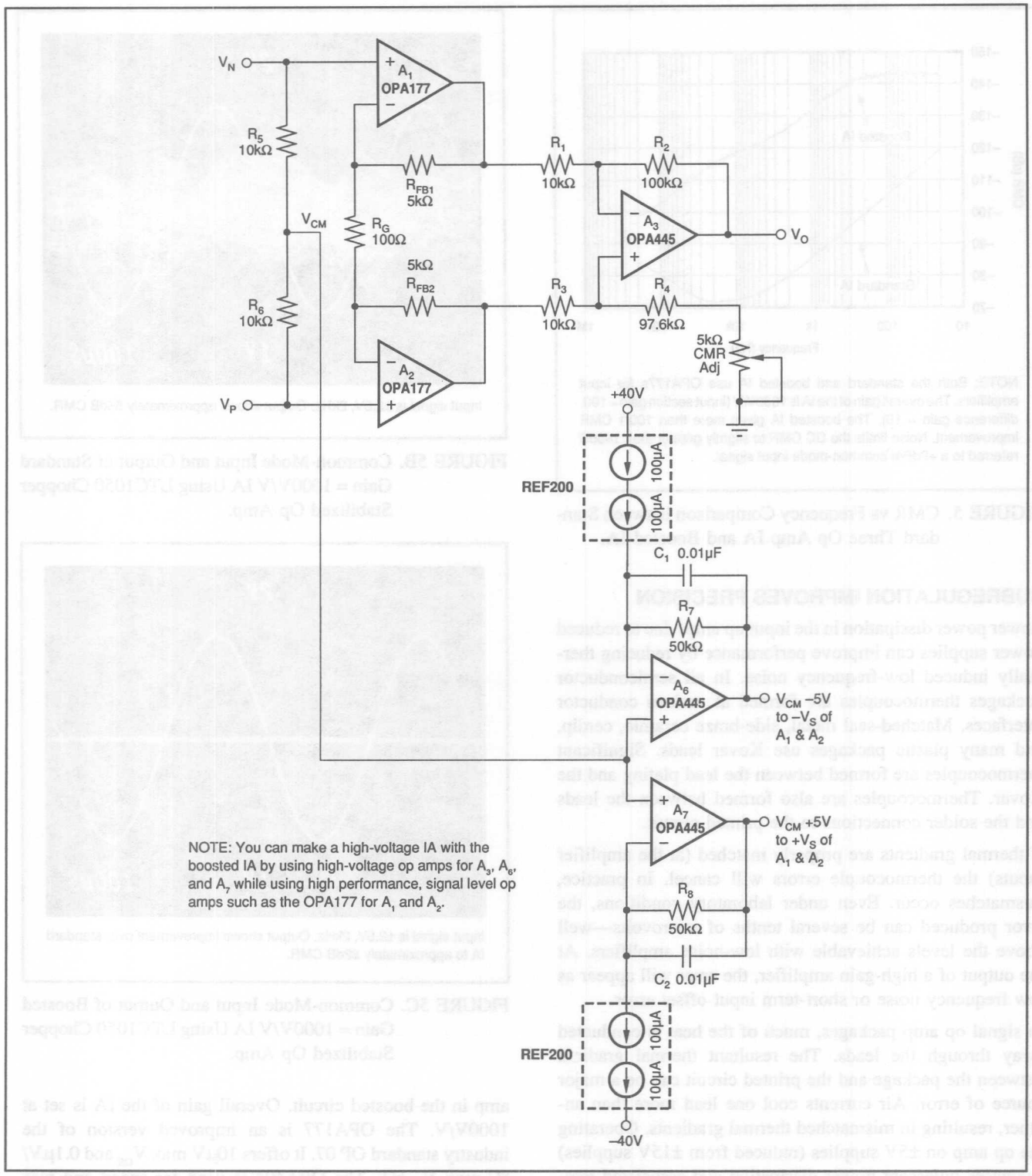
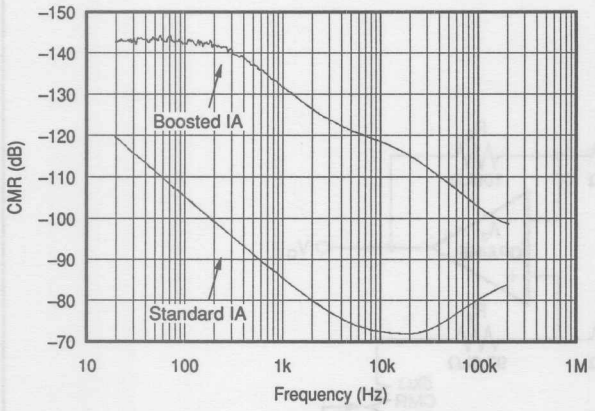


FIGURE 4. High Voltage Instrumentation Amplifier.

With a common-mode input of 7V one input amplifier must deliver 7V common-mode plus 5V differential—its 12V swing limit.

The boosted IA also has a ±7V common-mode input limit. The subregulators are set at ±5V from the input common-mode signal. With a 7V common mode input, one of the subregulator outputs is at its 12V swing limit.

In the boosted IA, using a gain-fo-10 difference amplifier, the buffer amplifiers must provide a differential output of only 1V for a 10V IA output. With the input amplifiers in equal gains, each must deliver one half of the 1V differential signal. With a common-mode input of 7V, one input amplifier must deliver 7V common-mode plus 0.5V differential for a total of 7.5V at its output which is no problem since the V_S is 12V (5V subregulated + 7V common-mode).



NOTE: Both the standard and boosted IA use OPA177s for input amplifiers. The overall gain of the IA is 1000V/V (input section gain = 100, difference gain = 10). The boosted IA gives more than 100/1 CMR improvement. Noise limits the DC CMR to slightly greater than 140dB referred to a +9dBm common-mode input signal.

FIGURE 5. CMR vs Frequency Comparison between Standard Three Op Amp IA and Boosted IA.

SUBREGULATION IMPROVES PRECISION

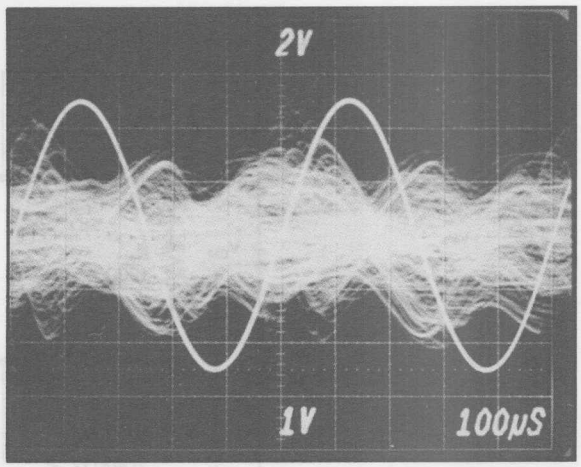
Lower power dissipation in the input op amps due to reduced power supplies can improve performance by reducing thermally induced low-frequency noise. In all semiconductor packages thermocouples are formed at various conductor interfaces. Matched-seal metal, side-braze ceramic, cerdip, and many plastic packages use Kovar leads. Significant thermocouples are formed between the lead plating and the Kovar. Thermocouples are also formed between the leads and the solder connections to the printed circuit.

If thermal gradients are properly matched (at the amplifier inputs) the thermocouple errors will cancel. In practice, mismatches occur. Even under laboratory conditions, the error produced can be several tenths of microvolts—well above the levels achievable with low-noise amplifiers. At the output of a high-gain amplifier, the error will appear as low frequency noise or short-term input offset error.

In signal op amp packages, much of the heat is conducted away through the leads. The resultant thermal gradient between the package and the printed circuit can be a major source of error. Air currents cool one lead more than another, resulting in mismatched thermal gradients. Operating the op amp on ±5V supplies (reduced from ±15V supplies) decreases quiescent power dissipation and associated temperature rise by three-to-one, providing a commensurate reduction in thermally induced errors.

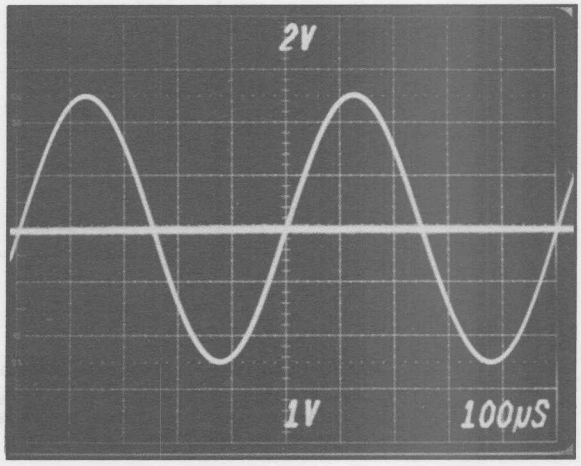
PERFORMANCE OF BOOSTED IA vs STANDARD IA

A performance comparison between the standard IA and the boosted IA in Figure 2 is shown in Figure 5. Amplifiers used for A_1 and A_2 are OPA177; A_3 is an INA106 gain-of-10 difference amplifier; and A_4 to A_7 are an OPA404 quad op



Input signal is ±2.5V, 2kHz. Output shows approximately 56dB CMR.

FIGURE 5B. Common-Mode Input and Output of Standard Gain = 1000V/V IA Using LTC1050 Chopper Stabilized Op Amp.



Input signal is ±2.5V, 2kHz. Output shows improvement over standard IA to approximately 82dB CMR.

FIGURE 5C. Common-Mode Input and Output of Boosted Gain = 1000V/V IA Using LTC1050 Chopper Stabilized Op Amp.

amp in the boosted circuit. Overall gain of the IA is set at 1000V/V. The OPA177 is an improved version of the industry standard OP 07. It offers 10µV max V_{OS} and 0.1µV/°C max V_{OS}/dT. The OPA404 is used for speed and bias current. The FET inputs of the OPA404 do not add loading at the input of the IA. The speed is high as compared to the OPA177 giving a good improvement of CMR vs Frequency. The CMR plots were made using an HP4194A gain-phase analyzer with an input signal to the IA of +9dBm. As you can see, CMR vs Frequency is boosted dramatically. At 2kHz, for example, the CMR of the standard IA is ≈ 80dB while the CMR of the boosted IA is more than 120dB—more than a 100-to-1 improvement!

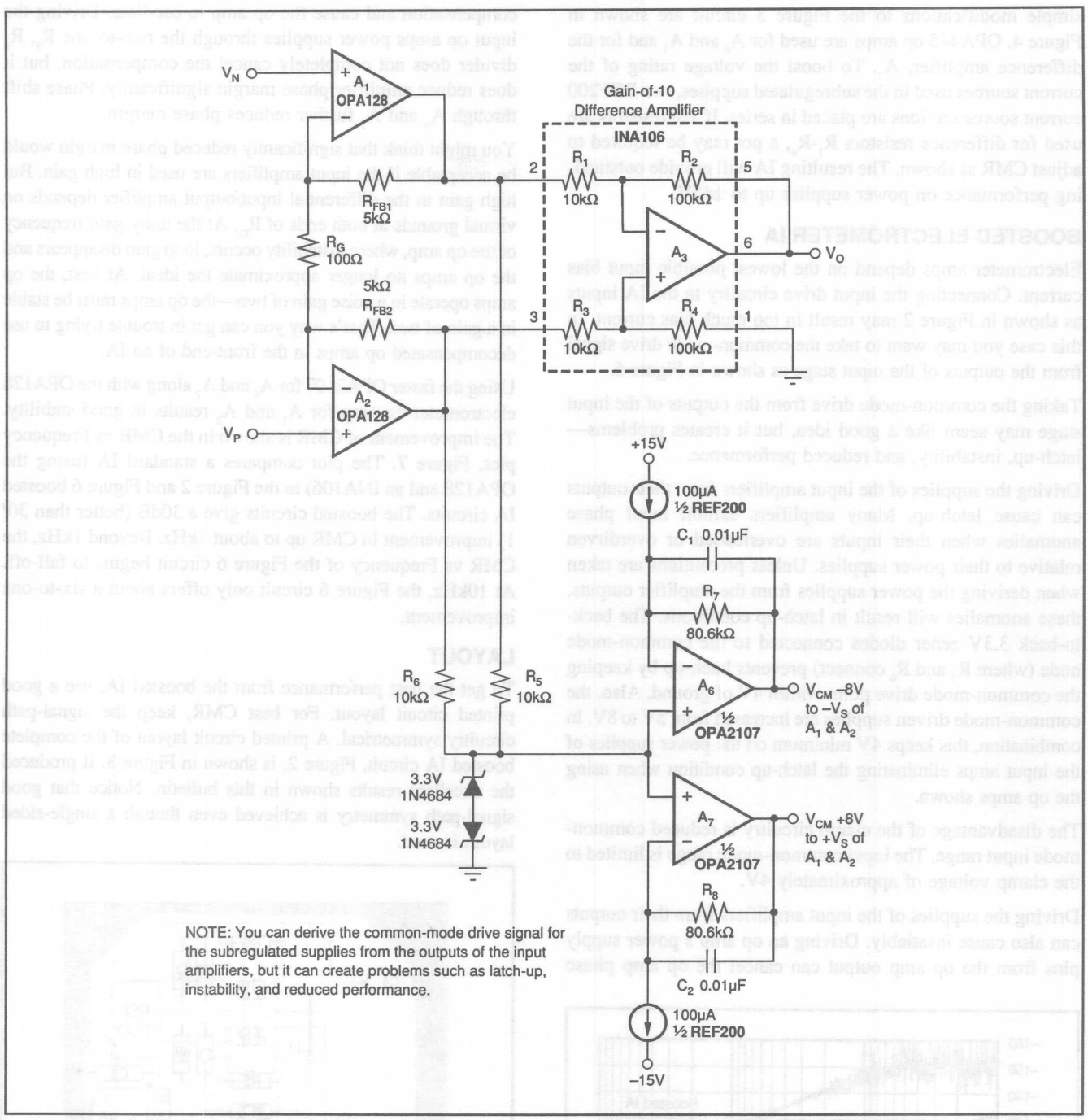


FIGURE 6. Boosted Electrometer Instrumentation Amplifier.

Another dramatic comparison is shown in the scope photos of the same IAs using LTC1050 chopper stabilized op amps for A_1 and A_2. When V_{OS}/dT is critical, chopper stabilized op amps may be the best choice—they offer 5µV max V_{OS} over temperature. As you can see, with a ±2.5V, 2kHz input signal, CMR is limited to ≈56dB by chopper noise. With the boosted circuit, CMR is a respectable ≈82dB.

The limit for CMR performance in the boosted IA is the difference amplifier. The more gain added ahead of the difference amplifier, the better the potential for improvement. For example, with a gain of 100V/V ahead of the difference amplifier an improvement in CMR of 40dB is possible. The actual performance boost will depend on matching and parasitics in the devices selected.

Of course, CMR vs Frequency depends on the dynamic performance of all amplifiers. Improvement in dynamic CMR will be most dramatic when the speed of the amplifiers used for A_4 to A_7 is much higher than the speed of A_1 and A_2.

HIGH-VOLTAGE IA

High voltage IAs can also be easily implemented using the boosted IA configuration. Standard precision signal level op amps can be used for the input amplifiers while the HV chores are taken care of by the other (less critical) op amps. The

simple modifications to the Figure 3 circuit are shown in Figure 4. OPA445 op amps are used for A_6 and A_7 and for the difference amplifier, A_3. To boost the voltage rating of the current sources used in the subregulated supplies, two REF200 current source sections are placed in series. If 1% resistors are used for difference resistors R_1-R_4, a pot may be required to adjust CMR as shown. The resulting IA will provide outstanding performance on power supplies up to ±45V.

BOOSTED ELECTROMETER IA

Electrometer amps depend on the lowest possible input bias current. Connecting the input drive circuitry to the IA inputs as shown in Figure 2 may result in too much bias current. In this case you may want to take the common-mode drive signal from the outputs of the input stage as shown in Figure 6.

Taking the common-mode drive from the outputs of the input stage may seem like a good idea, but it creates problems—latch-up, instability, and reduced performance.

Driving the supplies of the input amplifiers from their outputs can cause latch-up. Many amplifiers exhibit input phase anomalies when their inputs are overloaded or overdirven relative to their power supplies. Unless precautions are taken when deriving the power supplies from the amplifier outputs, these anomalies will result in latch-up conditions. The back-to-back 3.3V zener diodes connected to the common-mode node (where R_5 and R_6 connect) prevents latch-up by keeping the common-mode drive point within 4V of ground. Also, the common-mode driven supplies are increased from 5V to 8V. In combination, this keeps 4V minimum on the power supplies of the input amps eliminating the latch-up condition when using the op amps shown.

The disadvantage of the clamp circuitry is reduced common-mode input range. The input common-mode range is limited to the clamp voltage of approximately 4V.

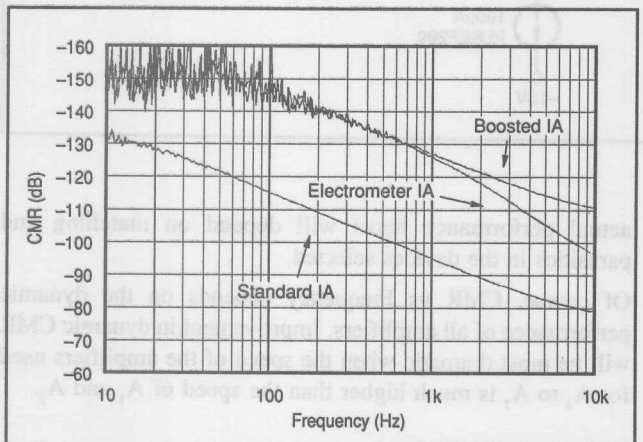
Driving the supplies of the input amplifiers from their outputs can also cause insatiably. Driving an op amp's power supply pins from the op amp output can cancel the op amp phase compensation and cause the op amp to oscillate. Driving the input op amps power supplies through the two-to-one R_5, R_6 divider does not completely cancel the compensation, but it does reduce amplifier phase margin significantly. Phase shift through A_6 and A_7 further reduces phase margin.

You might think that significantly reduced phase margin would be acceptable if the input amplifiers are used in high gain. But high gain in the differential input/output amplifier depends on virtual grounds at both ends of R_G. At the unity gain frequency of the op amp, where instability occurs, loop gain disappears and the op amps no longer approximate the ideal. At best, the op amps operate in a noise gain of two—the op amps must be stable in a gain of two. That's why you can get in trouble trying to use decompensated op amps in the front-end of an IA.

Using the faster OPA2107 for A_6 and A_7 along with the OPA128 electrometer op amp for A_1 and A_2 results in good stability. The improvement of CMR is shown in the CMR vs Frequency plot, Figure 7. The plot compares a standard IA (using the OPA128 and an INA106) to the Figure 2 and Figure 6 boosted IA circuits. The boosted circuits give a 30dB (better than 30/1) improvement in CMR up to about 1kHz. Beyond 1kHz, the CMR vs Frequency of the Figure 6 circuit begins to fall-off. At 10kHz, the Figure 6 circuit only offers about a six-to-one improvement.

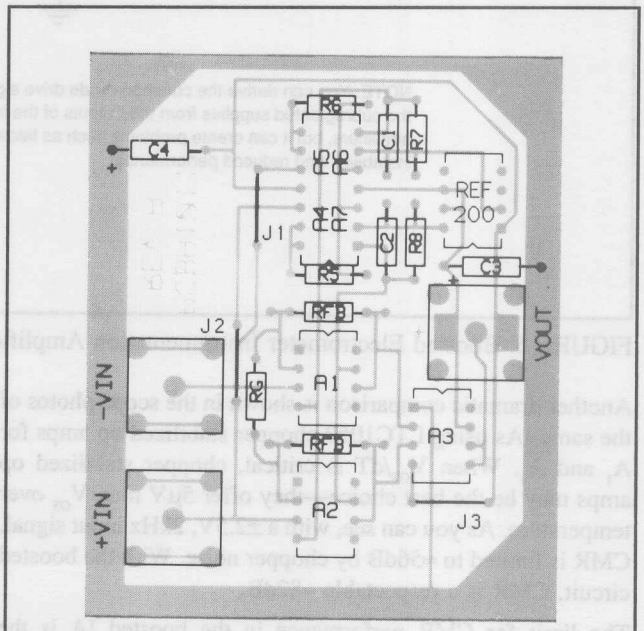
LAYOUT

To get the best performance from the boosted IA, use a good printed circuit layout. For best CMR, keep the signal-path circuitry symmetrical. A printed circuit layout of the complete boosted IA circuit, Figure 2, is shown in Figure 8. It produced the excellent results shown in this bulletin. Notice that good signal-path symmetry is achieved even though a single-sided layout is used.



NOTE: The boosted electrometer IA circuit adds CMR boost, but the boost starts to fall off beyond about 1kHz.

FIGURE 7. CMR vs Frequency Comparison between Standard Three Op Amp IA, Boosted IA, and Boosted Electrometer IA.



Best performance depends on signal-path symmetry. Notice that excellent symmetry can be maintained even with single-sided board layout. Extra pads at RFB allow *stacking* of feedback capacitors.

FIGURE 8. Printed Circuit Layout of Figure 2 Boosted IA.

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INPUT FILTERING THE INA117 ±200V DIFFERENCE AMPLIFIER

By R. Mark Stitt (602) 746-7445

Many customers have asked how to add input filtering to the INA117. Since the INA117 is rated for ±200V input voltage (±500V without damage), it is commonly used in environments with very high input noise or with high-voltage input transients. This bulletin shows how to connect input filters, discusses the errors they can add, and shows how to eliminate the errors.

Figure 1 shows the connection of a differential input filter. A pole is formed by C_1 and the two external input resistors. $f_{-3dB} = 1/(4 \cdot \pi \cdot R_I \cdot C_1)$. Differential input filtering is preferred because mismatches in filter components do not degrade CMR.

DON'T USE COMMON-MODE INPUT FILTERS ALONE

Don't be tempted to use common-mode input filtering alone (Figure 2) unless you are prepared to carefully match components. Mismatches between the $R_I \cdot C_2$ time constants reduce AC CMR. The mismatches result in a differential input signal in response to AC common-mode inputs. Even if you successfully match the components for good AC CMR at room temperature, maintaining the match over temperature can be a problem.

A COMBINATION COMMON-MODE AND DIFFERENTIAL INPUT FILTER IS OK

If you want common-mode input filtering, use it in conjunction with differential input filtering as shown in Figure 3. If

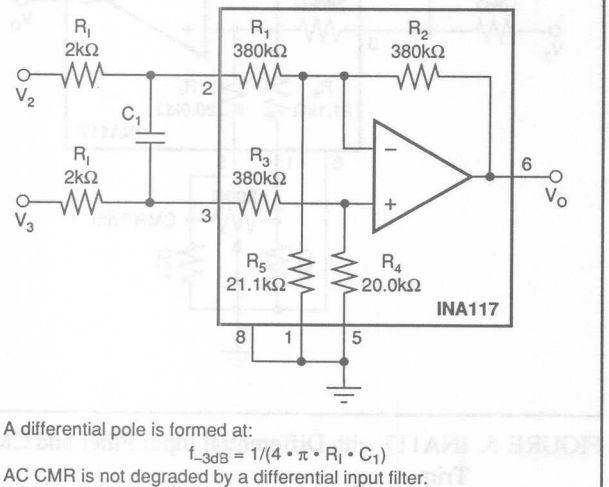

FIGURE 1. INA117 with Differential Input Filter.

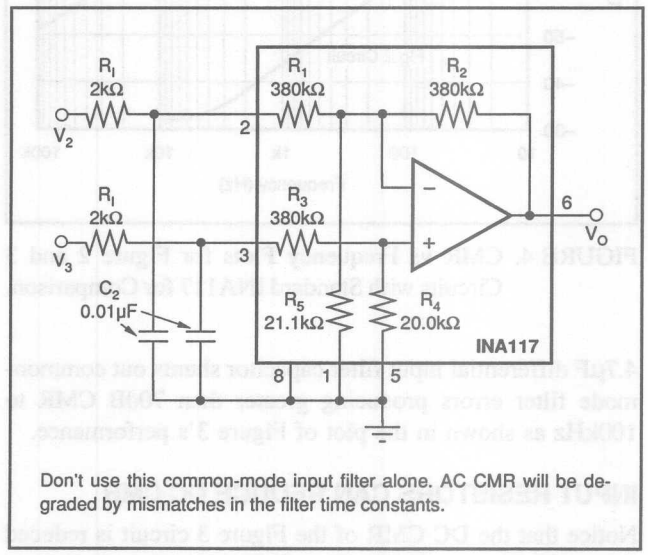

FIGURE 2. INA117 with Common-Mode Input Filter.

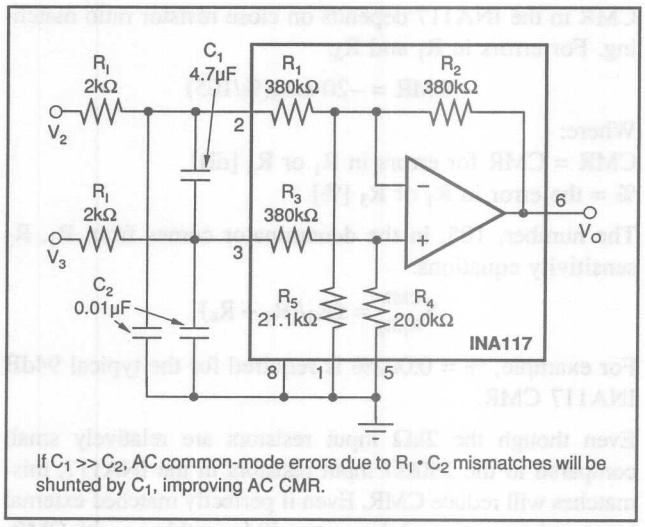

FIGURE 3. INA117 with a Combination Differential and Common-Mode Input Filter.

$C_1 >> C_2$, AC common-mode errors will be shunted by C_1 so AC CMR can be successfully boosted. A value of $C_1 = 500 \cdot C_2$ is suggested.

Figure 4 shows actual CMR vs Frequency performance plots for the Figure 2 and Figure 3 circuits. Standard INA117 performance is shown for comparison. The standard INA117 has about 60dB CMR at 30kHz. Mismatches of 5% in R • C time constants (5% C_2 mismatch) cause the Figure 2 circuit CMR to drop below 60dB at less than 200Hz. Adding a

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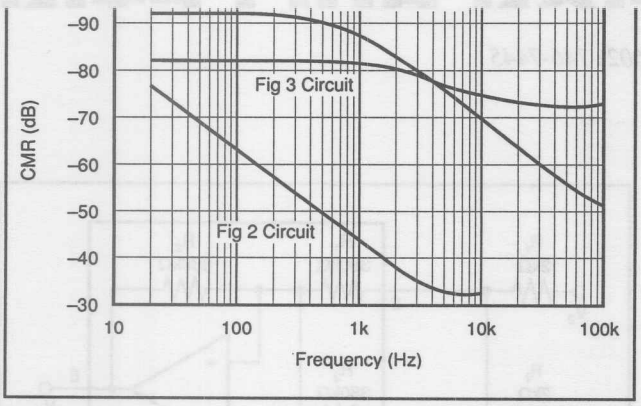

FIGURE 4. CMR vs Frequency Plots for Figure 2 and 3 Circuits with Standard INA117 for Comparison.

4.7µF differential input filter capacitor shunts out common-mode filter errors producing greater than 70dB CMR to 100kHz as shown in the plot of Figure 3's performance.

INPUT RESISTORS CAN REDUCE DC CMR

Notice that the DC CMR of the Figure 3 circuit is reduced from ≈92dB to ≈82dB. The CMR reduction is due to mismatches from input filter resistors, R_I.

CMR in the INA117 depends on close resistor ratio matching. For errors in R_1 and R_3:

$$CMR = -20\ Log(\%/105)$$

Where:
CMR = CMR for errors in R_1 or R_3 [dB]
% = the error in R_1 or R_3 [%]

The number, 105, in the denominator comes from R_1, R_3 sensitivity equations.

$$S^{CMR}_{R_1,R_3} = \pm R_1/(R_1 + R_4)$$

For example, % = 0.002% is required for the typical 94dB INA117 CMR.

Even though the 2kΩ input resistors are relatively small compared to the 380kΩ input resistors in the INA117, mismatches will reduce CMR. Even if perfectly matched external input resistors are used there can still be problems with CMR.

Although some resistor ratios in the INA117 are carefully matched to achieve good CMR, the R_1/R_3 ratio is not. A typical mismatch of 1% can be expected. The effect is to add an effective 1% mismatch to external resistors. The following worst-case CMR can be expected:

$$CMR = -20\ Log((ERROR_1 + ERROR_2)/105)$$

Where:
$ERROR_1$ = Error due R_I, R_1, and R_3 mismatches [%]
$ERROR_1 = R_I \cdot (T_{OL} + 1)/(R_I + 3.8 \cdot 10^5)$
R_I = DC resistance of external filter resistor, R_I, [Ω]
T_{OL} = Tolerance of R_I [%], i.e. 1.0 for 1%
$ERROR_2$ = Initial INA117 error [%]—See Table I

INA117BM typ	94	0.002
INA117BM min	86	0.005
INA117KP min	70	0.033

TABLE I. Initial INA117 CMR Values.

R_I (Ω)	$ERROR_1$ (%)	$ERROR_2$ (%)	CMR (dB)
1k	0.005	0.005	80
2k	0.010	0.005	76
5k	0.026	0.005	71
10k	0.051	0.005	65

TABLE II. Examples of Worst-Case CMR to be Expected (INA117BM and selected 1% R_Is).

Also,

$$ERROR_2 = \frac{105}{10(CMR_{117}/20)}$$

CMR_{117} = Initial INA117 CMR [dB]

See Tables I and II for examples.

CMR TRIM

If you want to use 10kΩ input resistors and must be assured of good DC CMR, you can use the trim circuit shown in Figure 5. Resistor TCR mismatches can limit difference amplifier performance over temperature. Use high quality film resistors and keep $R_I \leq 10k\Omega$ for good performance over temperature.

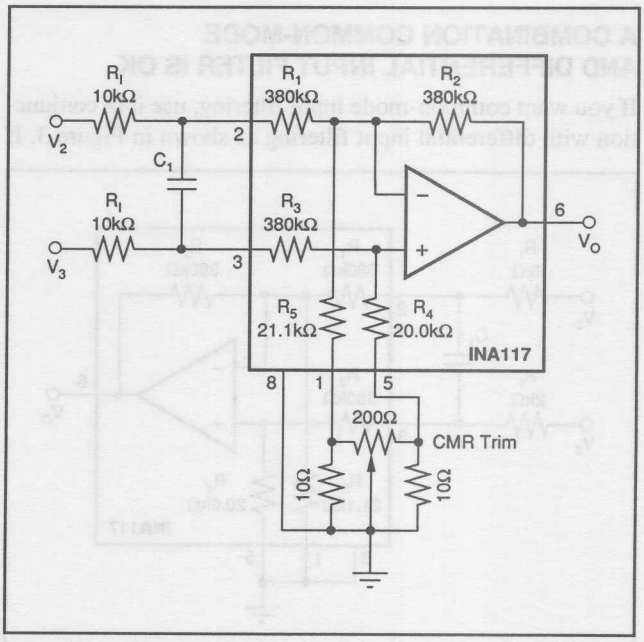

FIGURE 5. INA117 with Differential Input Filter and CMR Trim.

ADDED INPUT RESISTORS CAUSE GAIN ERROR

Adding input resistors to the INA117 causes gain error. When all resistor ratios are properly adjusted for good CMR, INA117 gain is R_2/R_1. When input filter resistors are added, gain is reduced to $R_2/(R_I + R_1)$. With $R_I = 10k\Omega$, gain is ≈0.974 V/V (approximately –2.6% gain error). Since gain does not depend on R_3, R_4, or R_5, the gain error can not be corrected by adding resistance in series with any pin.

CORRECTING GAIN ERROR

To correct for the gain error introduced by the input filter resistors, you can add a small amount of positive feedback as shown in Figure 6. Resistors R_{4A}, R_{4B}, and R_{5A} must be selected to maintain CMR and to give the proper positive feedback to correct for gain error.

The following procedure is suggested:

Set $\boxed{R_{4A} = 10\Omega}$

This is an arbitrary but adequate value for R_{4A}. It is the smallest standard 1% value. With this small value, even a 5% ratio matching error between R_{4A} and R_{5A} would only degrade INA117 CMR to 82.5dB. In practice, ratio errors will be lower than this when closest standard 1% resistors are used.

Calculate R_{4B} and R_{5A} and use closest standard 1% resistor value.

$$R_{4B} \approx 18 \bullet R_{4A} + \frac{19 \bullet R_2 \bullet R_{4A}}{R_I}$$

With $R_I < 10k\Omega$ and $R_{4A} = 10\Omega$ this is an adequate approximation for all practical purposes.

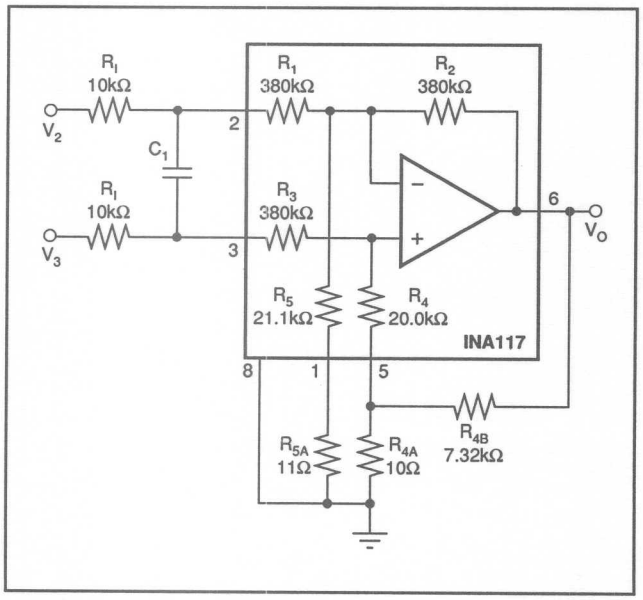

FIGURE 6. INA117 with Differential Input Filter and Positive Feedback Circuit to Compensate for Gain Error Due to R_I.

If $R_2 = 380k\Omega$, $R_I = 10k\Omega$, and $R_{4A} = 10\Omega$:

$$R_{4B} \approx 180 + \frac{72M\Omega}{R_I} \quad \boxed{\approx 7.4k\Omega}, \text{ use } 7.32k\Omega$$

$$R_{5A} \approx \frac{361 \bullet R_2 \bullet R_{4A} \bullet R_{4B}}{324(R_2 \bullet R_{4A}) + 324(R_2 \bullet R_{4B}) - 342(R_{4A} \bullet R_{4B})}$$

With $R_2 = 380k\Omega$ and $R_{4A} = 10\Omega$:

$$R_{5A} \approx \frac{3.61 \bullet R_{4B}}{3.24 + 0.323991 \bullet R_{4B}}$$

With $R_{4B} = 7.4k\Omega$, $\boxed{R_{5A} = 11.13\Omega}$, use 11Ω.

FINE-TRIM FOR ZERO GAIN ERROR

You must trim to get zero gain error. The resistors in the INA117 are accurately ratio trimmed to give excellent CMR and gain accuracy, but their absolute values are only accurate to within about ±20%. With the values calculated above, gain error will be reduced from approximately –2.6% to about ±0.5%.

For lower gain error use the gain-trim circuit shown in Figure 7. The circuit is the same as in Figure 6 except, R_{4B} is replaced with a 5kΩ fixed resistor and a 5kΩ pot.

To trim for zero gain error, ground the INA117 inputs (0V input) and measure the offset voltage, V_{OFF}, at the output. Apply a known input voltage, V_{REF}, (e.g. 10.0V) to the INA117 noninverting input. Measure V_{REF} so you know its precise value. Adjust the 5kΩ pot for the correct INA117 output voltage: $V_{OUT} = V_{REF} + V_{OFF}$.

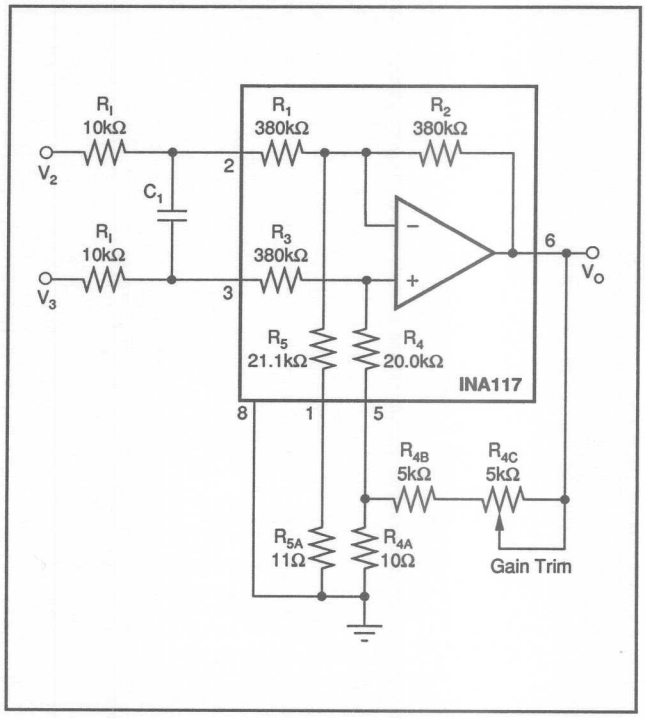

FIGURE 7. INA117 with Differential Input Filter and Gain Trim Circuit.

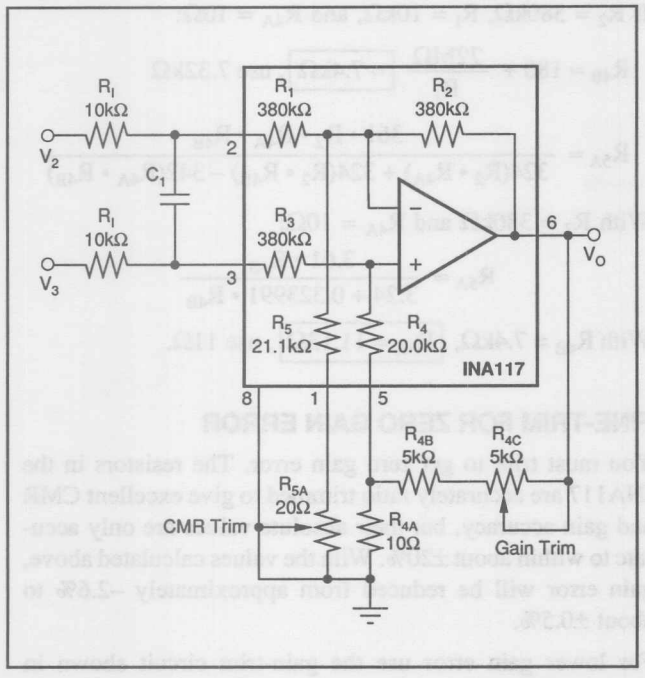

FIGURE 8. INA117 with Differential Input Filter and Both Gain Trim and CMR Trim Circuits.

You can automate the trim process by using an amplifier with a known gain of 1V/V. The Burr-Brown INA105BM difference amplifier with gain error = ±0.01% max is a good choice. Instead of using a voltage reference, drive the input of the INA117 with a ±5V, 10Hz sine or triangle wave (see AN-165, Fig. 46 for a suitable triangle generator circuit). Connect one input of the INA105 to the driven INA117 input. Connect the other input of the INA105 to the INA117 output. Adjust the 5kΩ gain trim pot for zero AC at the INA105 output. Using the AC technique allows you to distinguish between offset and gain error.

If you want to adjust both gain and CMR, use the circuit shown in Figure 8.

4-20mA TO 0-20mA CONVERTER AND CURRENT SUMMING CURRENT-TO-CURRENT CONVERTERS

By R. Mark Stitt and David Kunst (602) 746-7445

Current loops have become the standard for signal transmission in the process control industry. Current loops are insensitive to noise and are immune to errors from line impedance. Burr-Brown offers a complete line of monolithic 4mA to 20mA current loop transmitters and receivers.

XTR101

General purpose two-wire 4-20mA current-loop transmitter. This transmitter has an instrumentation amplifier input and two 1mA current sources for transducer excitation and offsetting.

XTR103

Two-wire RTD 4-20mA current-loop transmitter. Similar to XTR101, but with internal linearization circuitry for direct interface to RTDs (Resistance Temperature Detectors). The XTR103 along with an RTD forms a precision temperature to 4-20mA current loop transmitter.

XTR104

Two-wire bridge 4-20mA current-loop transmitter. Similar to XTR101, but with shunt regulator and linearization circuitry for direct interface to resistor transducer bridges.

XTR110

Three-wire 4-20mA transmitter. The XTR110 converts a 0-5V or 0-10V high-level input into a 0-20mA or 4-20mA current-soruce output.

RCV420

Self-contained 4-20mA receiver. Conditions and offsets 4-20mA input signals to give a precision 0-5V output. Contains precision voltage reference, 75Ω precision sense resistor and ±40V common-mode input range difference amplifier.

The 4mA to 20mA current loop is the most often used standard. Since the minimum signal current is 4mA, the transducer and transmitter can be powered by the same two wires used for the current loop connection. This feature eliminates the need for a remote power supply. Also, open circuits are easy to detect since the signal goes to 0mA. Some systems, however, use a 0 to 20mA current loop standard instead. To interface to these systems, the 4-20mA XTR output must be converted to 0-20mA. This bulletin shows the suggested circuit and also discusses summing current-to-current converters in general.

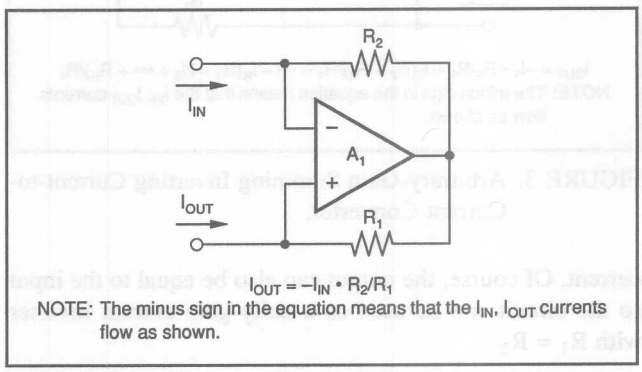

FIGURE 1. Basic Inverting Current-to-Current Converter.

INVERTING CURRENT-TO-CURRENT CONVERTERS

Figure 1 shows the basic inverting current-to-current converter. The input current all flows through R_2 resulting in an $I_{IN} \cdot R_2$ voltage drop across R_2. The op amp forces the same voltage across R_1 so that there is no voltage difference at the op amp inputs. The I_{OUT} current is therefore:

For Figure 1:

$$I_{OUT} = -I_{IN} \cdot R_2/R_1$$

Notice that, like its cousin the inverting voltage amplifier, the output current can be greater than or less than the input

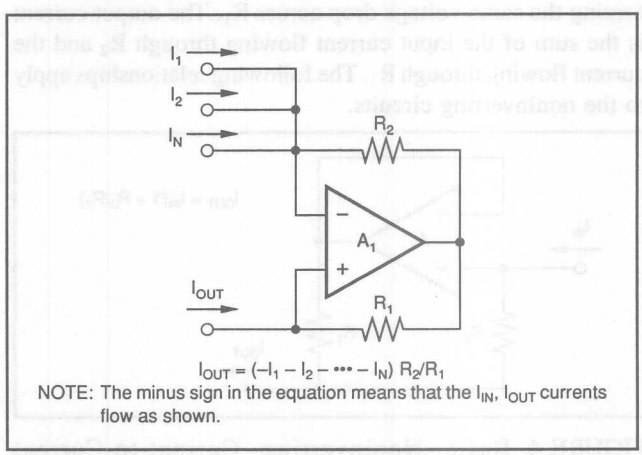

FIGURE 2. Equal-Gain Summing Inverting Current-to-Current Converter.

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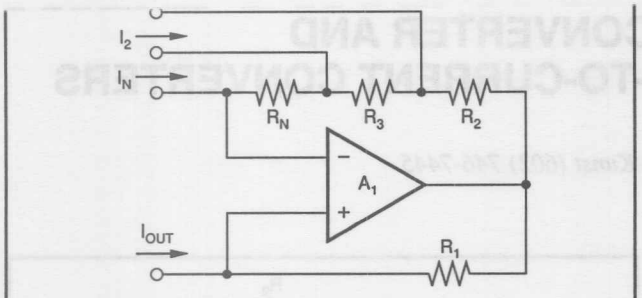


$I_{OUT} = -I_1 \cdot R_2/R_1 - I_2(R_2 + R_3)/R_1 - \cdots - I_N(R_2 + R_3 + \cdots + R_N)/R_1$

NOTE: The minus sign in the equation means that the I_{IN}, I_{OUT} currents flow as shown.

FIGURE 3. Arbitrary-Gain Summing Inverting Current-to-Current Converter.

current. Of course, the output can also be equal to the input so the circuit can be used as a unity-gain current inverter with $R_1 = R_2$.

So long as the gain is the same, any number of currents can be summed at the current-to-current converter input as shown in Figure 2.

For Figure 2:

$$I_{OUT} = (-I_1 - I_2 - \cdots - I_N)R_2/R_1$$

Any number of currents can be summed with arbitrary gain by using separate gain-setting resistors as shown in Figure 3.

For Figure 3:

$$I_{OUT} = -I_1 \cdot R_2/R_1 - I_2(R_2 + R_3)/R_1 - \cdots - I_N(R_2 + R_3 + \cdots + R_N)/R_1$$

NONINVERTING CURRENT-TO-CURRENT CONVERTERS

Figure 4 shows the circuit for the basic noninverting current-to-current converter. As before, all the input current flows through R_2 resulting in a $I_{IN} \cdot R_2$ voltage drop across R_2. In this circuit, the op amp is connected as a unity-gain buffer forcing the same voltage drop across R_1. The output current is the sum of the input current flowing through R_2 and the current flowing through R_1. The following relationships apply to the noninverting circuits.

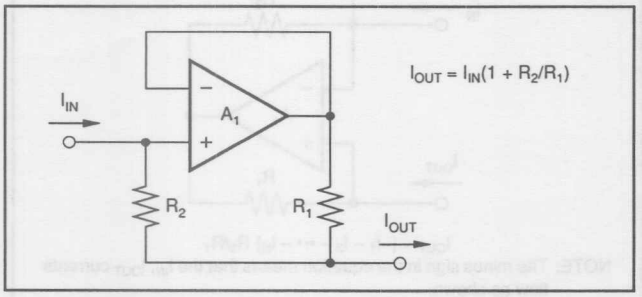


FIGURE 4. Basic Noninverting Current-to-Current Converter.

$I_{OUT} = I_{IN}(1 + R_2/R_1)$

Notice that, like its cousin the noninverting voltage amplifier, the gain is always greater than 1.0 so that the output current must always be greater than the input current.

As with the inverting summing current-to-current converter, so long as the gain is the same, any number of currents can be summed at the current-to-current converter input as shown in Figure 5.

For Figure 5:

$$I_{OUT} = (I_1 + I_2 + \cdots + I_N)(1 + R_2/R_1)$$

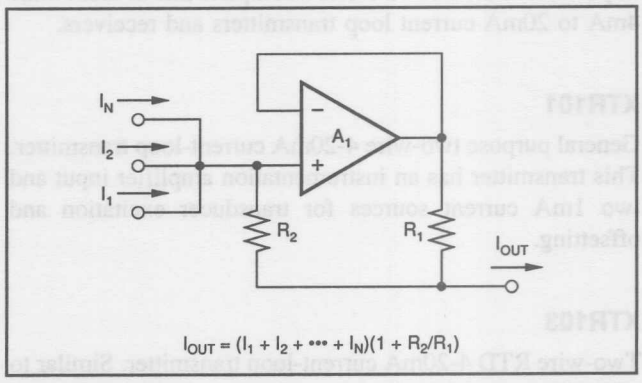


FIGURE 5. Equal-Gain Summing Noninverting Current-to-Current Converter.

Likewise, any number of currents can be summed with arbitrary gain by using separate gain-setting resistors as shown in Figure 6.

For Figure 6:

$$I_{OUT} = I_1(1 + R_2/R_1) + I_2(R_1 + R_2 + R_3)/R_1 + \cdots + I_N(R_1 + R_2 + R_3 + \cdots + R_N)/R_1$$

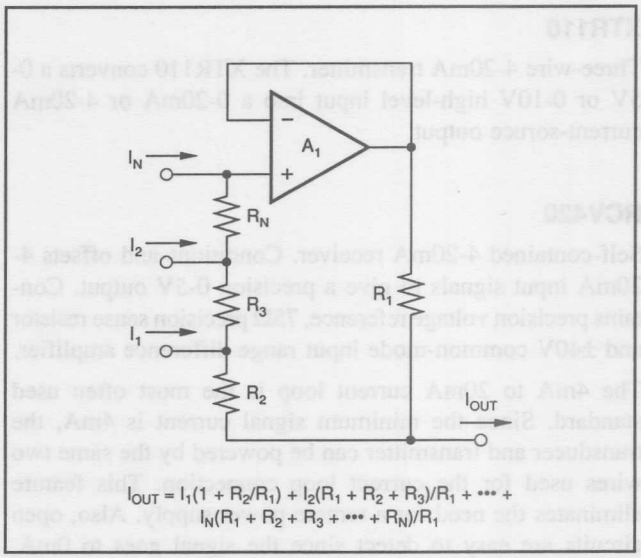


FIGURE 6. Arbitrary-Gain Summing Noninverting Current-to-Current Converter.

INVERTING AND NONINVERTING CURRENT-TO-CURRENT CONVERTERS

The inverting and noninverting circuits can be used simultaneously either with equal gains or arbitrary gains as shown in Figures 7 and 8:

For Figure 7:

$$I_{OUT} = \{(-I_{1A} - I_{2A} - \bullet\bullet\bullet - I_{NA})R_{2A}/R_{1B}\} + \{(I_{1B} + I_{2B} + \bullet\bullet\bullet + I_{NB})(1 + R_{2B}/R_{1B})\}$$

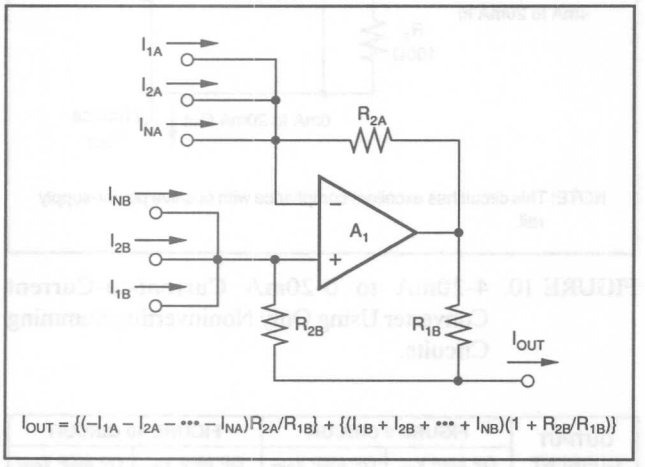


FIGURE 7. Equal-Gain Summing Inverting and Noninverting Current-to-Current Converter.

For Figure 8:

$$I_{OUT} = \{-I_{1A} \bullet R_{2A}/R_{1B} - I_{2A}(R_{2A} + R_{3A})/R_{1B} - \bullet\bullet\bullet - I_{NA}(R_{2A} + R_{3A} + \bullet\bullet\bullet + R_{NA})/R_{1B}\} + \{I_{1B}(1 + R_{2B}/R_{1B}) + I_{2B}(R_{1B} + R_{2B} + R_{3B})/R_{1B} + \bullet\bullet\bullet + I_{NB}(R_{1B} + R_{2B} + R_{3B} + \bullet\bullet\bullet + R_{NB})/R_{1B}\}$$

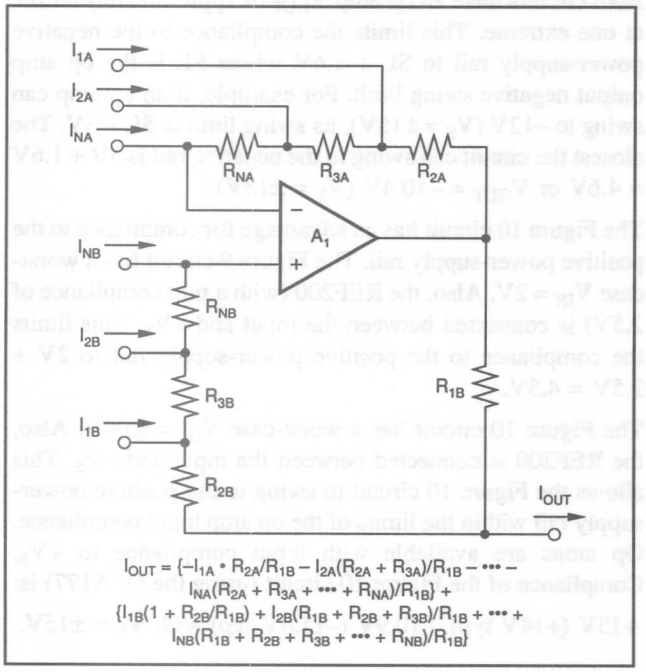


FIGURE 8. Arbitrary-Gain Summing Inverting and Noninverting Current-to-Current Converter.

4-20mA to 0-20mA CONVERTER

There are two ways to make a 4-20mA to 0-20mA converter using current summing circuits and a REF200 100µA current source for offsetting. Since the polarity of the 0-20mA output current must be the same as the 4-20mA input signal, the noninverting circuit is used in the main signal path. The REF200 100µA current source can be connected in either polarity so either inverting or noninverting summing can be used to offset the signal for 0mA out with 4mA in.

4-20mA to 0-20mA CONVERTER USING BOTH INVERTING AND NONINVERTING CURRENT-TO-CURRENT CONVERTER CIRCUITS

One implementation of the 4-20mA to 0-20mA converter is shown in Figure 9. From the Figure 4 and Figure 1 equations:

For Figure 9:

$$I_{OUT} = I_1(1 + R_2/R_1) - I_2 \bullet R_3/R_1$$

Where:

I_1 = 4-20mA input current

I_2 = 100µA REF200 offsetting current

Two equations can be written: one for I_{OUT} = 0mA with I_{IN} = 4mA and one for I_{OUT} = 20mA with I_{IN} = 20mA. Since there are three unknowns (R_1, R_2, and R_3) and only two equations, one resistor value must be selected first. A value of 100Ω was selected as an arbitrary but adequate value for R_2. With R_2 = 100Ω, the maximum voltage drop across it is 2V at 20mA. A smaller value for R_2 will reduce the voltage burden and power dissipation in the circuit, but since the signal-to-noise ratio is reduced, it will be more sensitive to op amp errors.

To solve for R_1:

Notice that the current gain is:

$$(20mA - 0mA)/(20mA - 4mA) = (20mA)/(16mA) = 1.25mA/mA$$

Rewriting the Figure 4 equation in terms of gain:

$$GAIN = I_{OUT}/I_{IN}$$
$$GAIN = 1 + R_2/R_1$$

Solving the gain equation for R_1:

$$R_1 = R_2/(GAIN - 1)$$

Substituting R_2 = 100Ω:

$$R_1 = 100\Omega/(1.25 - 1)$$
$$R_1 = 400\Omega$$

Then, solving the Figure 9 equation for R_3:

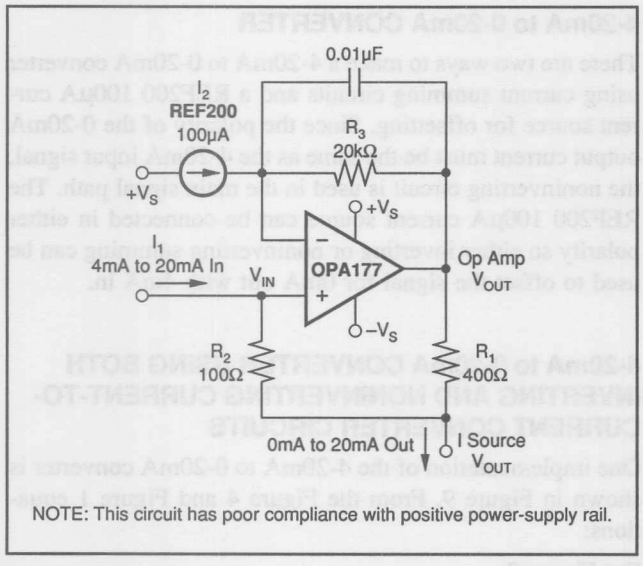
$$R_3 = I_1(R_1 + R_2)/I_2$$

Substituting I_1 = 4mA, I_2 = 100µA:

$$R_3 = 40(R_1 + R_2)$$

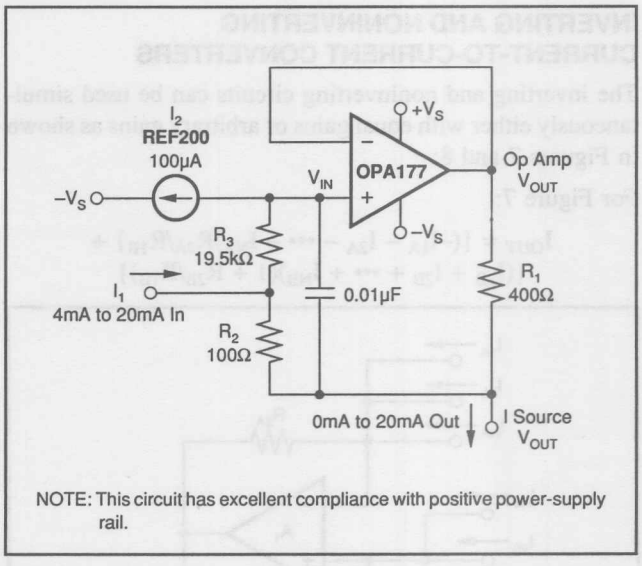
Substituting R_1 = 100Ω, R_2 = 400Ω:

$$R_3 = 20.0k\Omega$$



NOTE: This circuit has poor compliance with positive power-supply rail.

FIGURE 9. 4-20mA to 0-20mA Current-to-Current Converter Using Inverting and Noninverting Summing Circuits.



NOTE: This circuit has excellent compliance with positive power-supply rail.

FIGURE 10. 4-20mA to 0-20mA Current-to-Current Converter Using Only Noninverting Summing Circuits.

4-20mA TO 0-20mA CONVERTER USING ONLY NONINVERTING CURRENT-TO-CURRENT CONVERTER CIRCUIT

The other possible circuit is shown in Figure 10. From the Figure 6 equations:

For Figure 10:

$$I_{OUT} = I_1(1 + R_2/R_1) + I_2(R_1 + R_2 + R_3)/R_1$$

Where, as before:
I_1 = 4-20mA input current
I_2 = 100µA REF200 offsetting current

The relationships for R_1 and R_2 are the same as for the Figure 9 circuit: with $R_2 = 100\Omega$, $R_1 = 400\Omega$.

Solving the Figure 10 equation for R_3:

$$R_3 = (I_1 - I_2)(R_1 + R_2)/I_2$$

Substituting $I_1 = 4mA$, $I_2 = 100\mu A$:

$$R_3 = 39(R_1 + R_2)$$

Substituting $R_1 = 100\Omega$, $R_2 = 400\Omega$:

$$R_3 = 19.5k\Omega$$

WHICH 4-20mA TO 0-20mA CONVERTER IS BETTER?

The only significant functional difference between the Figure 9 and Figure 10 converter circuits is the output voltage compliance range. Output range of the current-to-current converter circuit is limited by the op amp input and output ranges and by the minimum compliance range of the REF200 current source. Voltages for the two circuits at the 0mA and 20mA output current extremes are shown in Table I.

OUTPUT CURRENT	FIGURE 9 CIRCUIT		FIGURE 10 CIRCUIT	
	OP AMP V_{IN}	OP AMP V_{OUT}	OP AMP V_{IN}	OP AMP V_{OUT}
0mA	0.4	–1.6	–1.56	–1.56
20mA	2.0	0.0	0.04	0.04
NOTE: With the 0-20mA output connection node held at 0V.				

TABLE I. Op Amp Input/Output Voltages for Figures 9 and 10 Circuits.

Both circuits have an op amp V_{OUT} of approximately –1.6V at one extreme. This limits the compliance to the negative power-supply rail to SL + 1.6V where SL is the op amp output negative swing limit. For example, if an op amp can swing to –12V ($V_S = \pm 15V$), its swing limit is SL = 3V. The closest the circuit can swing to the negative rail is 3V + 1.6V = 4.6V or $V_{OUT} = -10.4V$ ($V_S = \pm 15V$).

The Figure 10 circuit has an advantage for compliance to the positive power-supply rail. The Figure 9 circuit has a worst-case $V_{IN} = 2V$. Also, the REF200 (with a min compliance of 2.5V) is connected between the input and $+V_S$. This limits the compliance to the positive power-supply rail to 2V + 2.5V = 4.5V.

The Figure 10 circuit has a worst-case $V_{IN} = 0.04V$. Also, the REF200 is connected between the input and $-V_S$. This allows the Figure 10 circuit to swing to the positive power-supply rail within the limits of the op amp input compliance. Op amps are available with input compliance to $+V_S$. Compliance of the Figure 10 circuit (using the OPA177) is: +13V (+14V typ), –10.9V (–11.4V typ) with $V_S = \pm 15V$.

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IC BUILDING BLOCKS FORM COMPLETE ISOLATED 4-20mA CURRENT-LOOP SYSTEMS

By R. Mark Stitt and David Kunst (602) 746-7445

Current loops have become the standard for signal transmission in the process control industry. Current loops are insensitive to noise and are immune to errors from line impedance. Adding isolation to the 4-20mA current loop protects system electronics from electrical noise and transients. It also allows transducers to be electrically separated by hundreds of volts. Burr-Brown now offers all of the integrated circuit building blocks needed to assemble complete isolated 4-20mA current-loop systems. The product line includes two-wire transmitters, two-wire receivers, low cost isolation amplifiers, and low cost isolation power supplies. Three two-wire transmitters are available: one is general purpose, one designed for use with RTD temperature sensors, and one designed for use with bridge circuits.

THE BASIC ISOLATED 4-20mA TWO-WIRE SYSTEM

Figure 1 shows a typical isolated 4-20mA system. An XTR101 converts a position sensor output into a two-wire 4-20mA current-loop signal. An ISO122 low-cost isolation amplifier isolates the 0-5V signal. Power (±15V for the RCV420, 30V for the current loop) is supplied by the HPR117 low-cost DC/DC converter.

In this example, a Penny & Giles Model HLP 190 50mm linear potentiometer is used as the position transducer. One of the 1mA current sources in the XTR101 is used to bias the transducer. A 2kΩ fixed resistor in parallel with the 2kΩ potentiometer sets its output range to 0-1V. The 2.5kΩ resistor sets a 5V common-mode input level to bias the XTR101 instrumentation amplifier input into its linear region.

With the span-setting resistor connections open, the XTR101 current-loop output is:

$$I_O = 4mA + V_{IN}/62.5\Omega$$

Where:
I_O = current loop output (A)
V_{IN} = Differential IA input voltage between pins 3 and 4 (V)

The XTR101 directly converts the 0-1V position sensor output into a 4-20mA current loop output. The isolated voltage output from the ISO122 is 0-5V for 0-50mm displacement.

Other, more specialized two-wire transmitters are also available. See the brief summary at right of available building blocks.

HPR117 LOW-COST ISOLATED DC/DC CONVERTER

Provides ±15V, 30mA isolated output power with 15V input. Key specifications are:
$\pm V_{OUT} = V_{IN}$, ±5%
(V_{IN} = 13.5V to 16.5V, I_{OUT} = 25mA)
I_{OUT} = 30mA continuous at 70°C.
8mA quiescent current, no load; 80% efficiency, full load
750VDC isolation rating

ISO122 LOW-COST PRECISION ISOLATION AMPLIFIER

Precision analog isolation amplifier in a standard 16-pin plastic DIP. Key specifications are:
Unity gain (±10V in to ±10V out), ±0.05%
0.02% max nonlinearity
5mA quiescent current
140dB isolation mode rejection at 60Hz
1500Vrms continuous isolation rating (100% tested)

RCV420

Self-contained 4-20mA receiver. Conditions and offsets 4-20mA input signals to give a precision 0-5V output. Contains precision voltage reference, 75Ω precision sense resistor and ±40V common-mode input range difference amplifier. The RCV420 has a total combined span and zero error of less than 0.1%—adjustable to zero.

XTR101

General purpose two-wire 4-20mA current-loop transmitter. This transmitter has an instrumentation amplifier input and two 1mA current sources for transducer excitation and offsetting.

XTR103

Two-wire RTD 4-20mA current-loop transmitter with 9V compliance. Similar to XTR101, but with internal linearization circuitry for direct interface to RTDs (Resistance Temperature Detectors). The XTR103, along with an RTD, forms a precision temperature to 4-20mA current-loop transmitter. Along with an RTD, the XTR103 can achieve better than 0.1% span linearity over a –200°C to +850°C temperature span.

XTR104

Two-wire bridge 4-20mA current-loop transmitter with 9V compliance. Similar to XTR101, but with shunt regulator and linearization circuitry for direct interface to resistor transducer bridges. The XTR104 can provide better than 0.1% span linearity from bridges with uncorrected linearity in excess of 2%.

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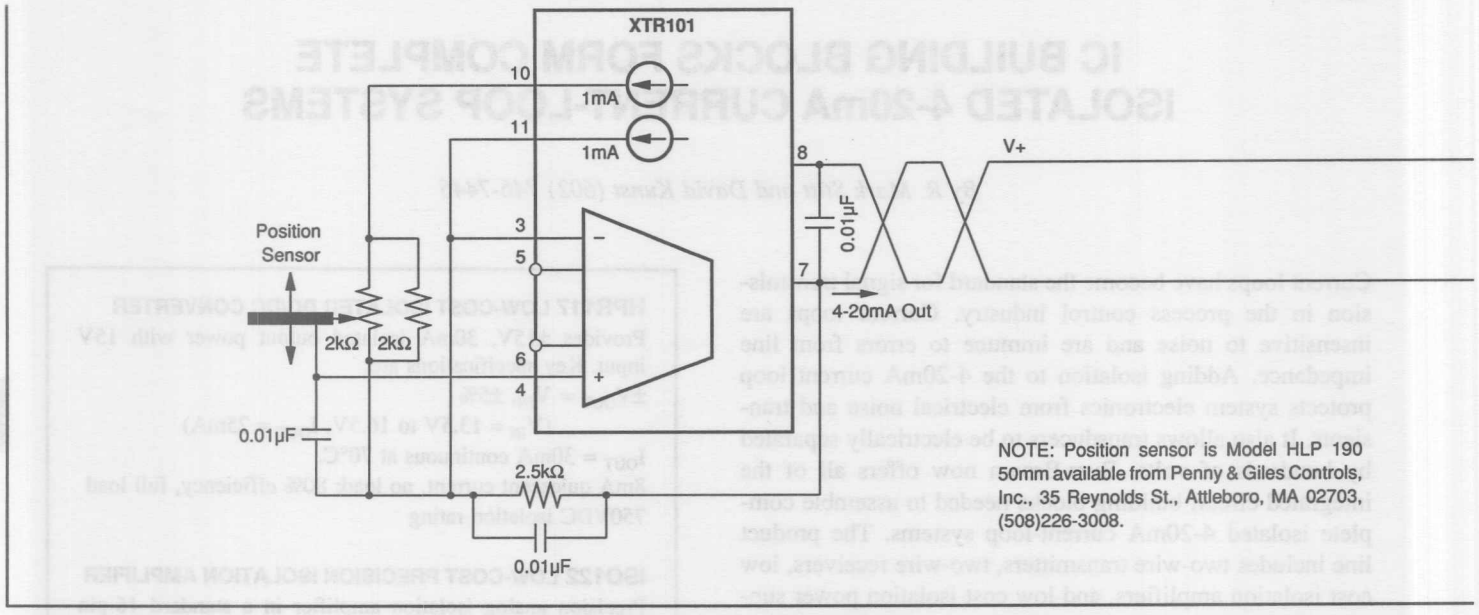


FIGURE 1. Four IC Packages and Transducer Form Complete Isolated 4-20mA Current-Loop System.

THERMISTOR-BASED TEMPERATURE MEASUREMENT

The most often measured physical parameter is temperature. Of the many commonly used temperature measurement transducers, the thermistor is the least expensive. Both positive and negative temperature coefficient types are available in all sorts of packages. Due to their high temperature coefficients, negative temperature coefficient types are the most common and widely used types. Thermistors are useful for temperature measurement from –55°C up to 300°C.

Figure 2 shows the circuit for a thermistor-based two-wire 4-20mA current-loop temperature measurement system. A bridge is formed with a thermistor, R_{T1}, and a 5kΩ variable resistor. The bridge is excited by the two 1mA current sources in the XTR101. The 5kΩ variable resistor is used to set the temperature-range zero for 4mA current loop output. The XTR101 span setting resistor, R_S, sets the span to get 20mA current-loop output at full-scale. XTR101 current-loop output is:

$$I_O = 4mA + V_{IN}(1 + 2500\Omega/R_S)/62.5\Omega$$

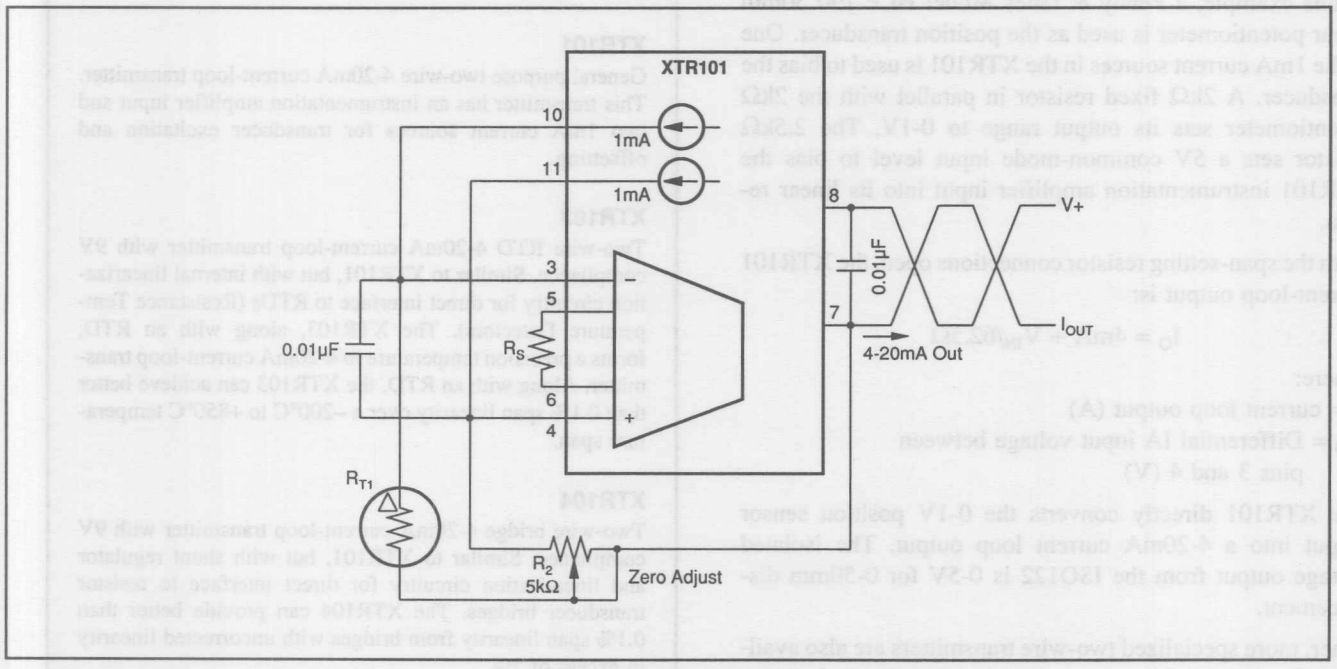
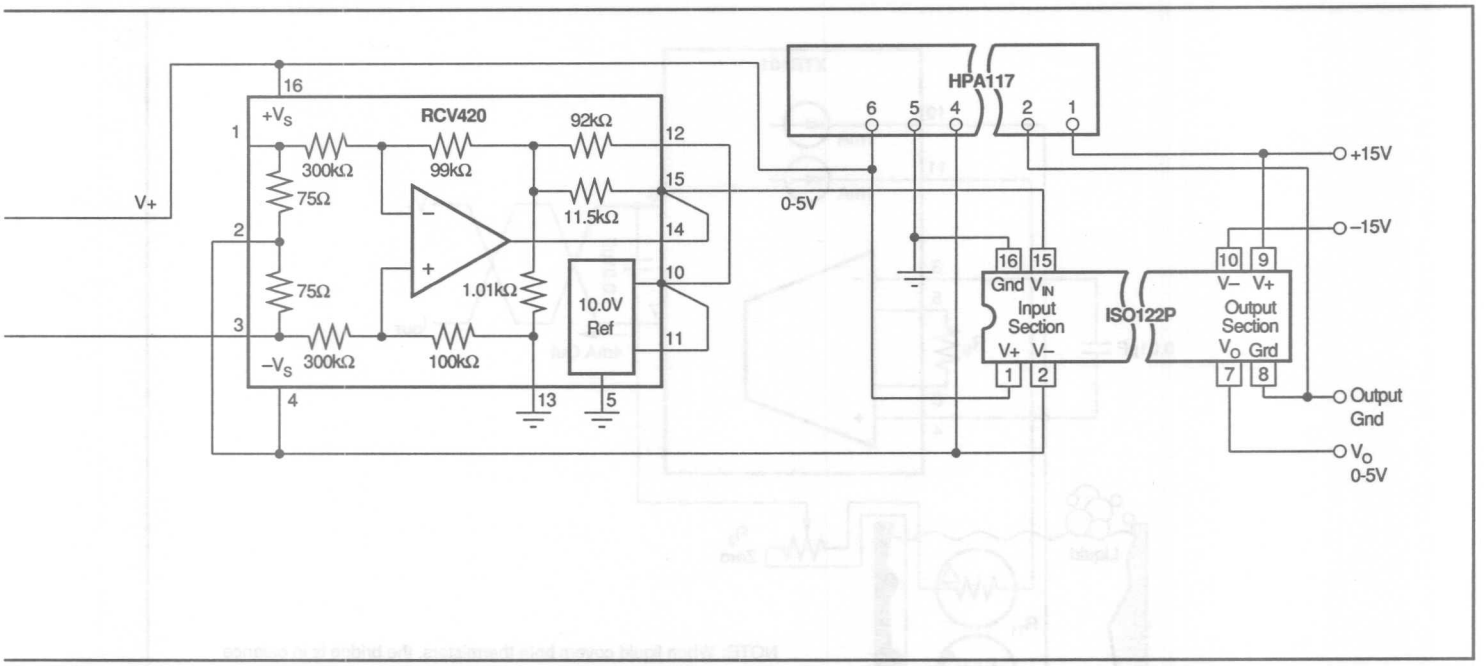


FIGURE 2. Basic Thermistor-Based Two-wire Temperature Measurement Using XTR101.



Where:

I_O = Current loop output (A)

V_{IN} = Differential IA input voltage between pins 3 and 4 (V)

R_S = Span-setting resistor (Ω)

Keep in mind that the maximum differential input range for the XTR101 is 1V.

Since the thermistor is a powered sensor, self heating can be a problem. For example, with a thermistor voltage of 5V, power dissipation is 5V • 1mA = 5mW. If a bead-in-glass type thermistor with a thermal resistance of 600°C/W is used, self-heating can increase the thermistor temperature by 3°C. To minimize this error, use a thermistor in a low thermal resistance package or lower the thermal resistance by heat sinking the thermistor to a thermal mass residing at the temperature to be measured. For example, if air temperature in an enclosure is to be measured, attach the thermistor to the package instead of mounting it in free air.

THERMISTOR-BASED LIQUID LEVEL INDICATOR

Due to high nonlinearities, thermistors can only be used for accurate temperature measurement over relatively small temperature spans. The high output of thermistors, however makes them attractive for other applications. In some applications thermistor self-heating can be used to advantage. Consider, for example, the liquid level indicator shown in Figures 3A and 3B. A bridge is formed by a pair of matched thermistors. The bridge is excited by the 1mA current sources in the XTR101. When both thermistors are submerged in liquid as shown in Figure 3A, the thermistors are at the same temperature—heat-sinked by the liquid. The potentiometer, R_3, is used to correct for component tolerances and zero the bridge for 4mA current-loop output.

When the liquid level falls below thermistor R_{T1} as shown in Figure 3B, the temperature of R_{T1} increases due to self-heating. The resulting bridge imbalance is measured by the XTR. Span-setting resistor, R_S, is selected to give 10mA output under low liquid level conditions. There is no simple rule for selecting R_S. Its value depends on thermistor selection and liquid properties and conditions.

When compared to level detectors using floats and moving parts, a thermistor-based liquid level indicator can have much better reliability.

GAS FLOW MEASUREMENT USING THERMISTORS

The liquid level indicator uses thermistor self-heating for a two-state high/low measurement. The gas flow measurement system shown in Figure 3C gives a quantitative flow rate measurement.

As in the previous example, a matched thermistor bridge is biased by the two 1mA current sources in the XTR101. One thermistor is positioned in the air flow stream. The other thermistor resides in still air—baffled from the air stream. The thermal resistance of the thermistor is proportional to the air flow rate. Potentiometer, R_3, is used to balance the bridge for 4mA out at zero flow rate. Span setting resistor, R_S, is selected to give a full-scale 20mA output at maximum flow rate. The value of R_S depends on thermistor characteristics and gas flow dynamics.

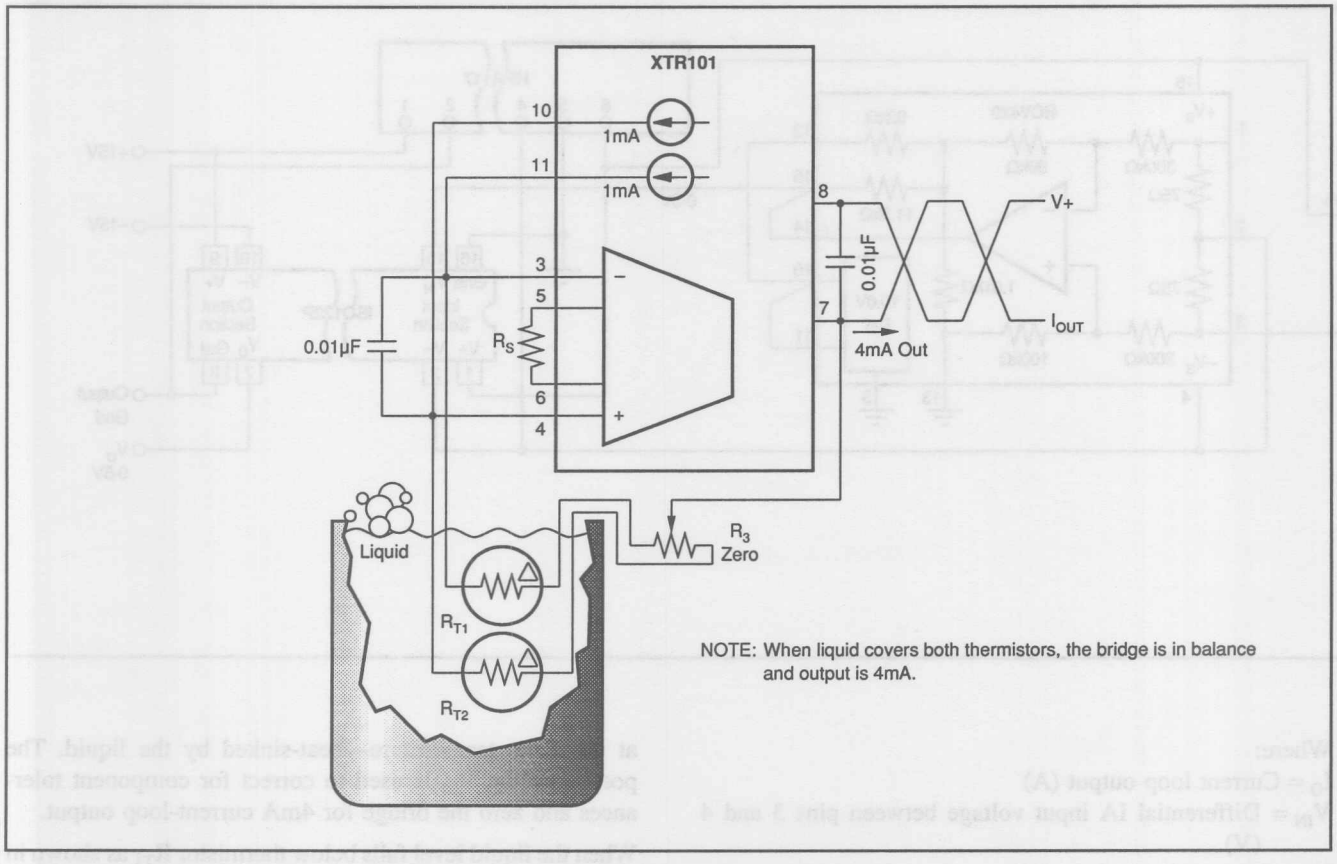


FIGURE 3A. Thermistor-Based Two-wire Liquid Level Detector Using XTR101.

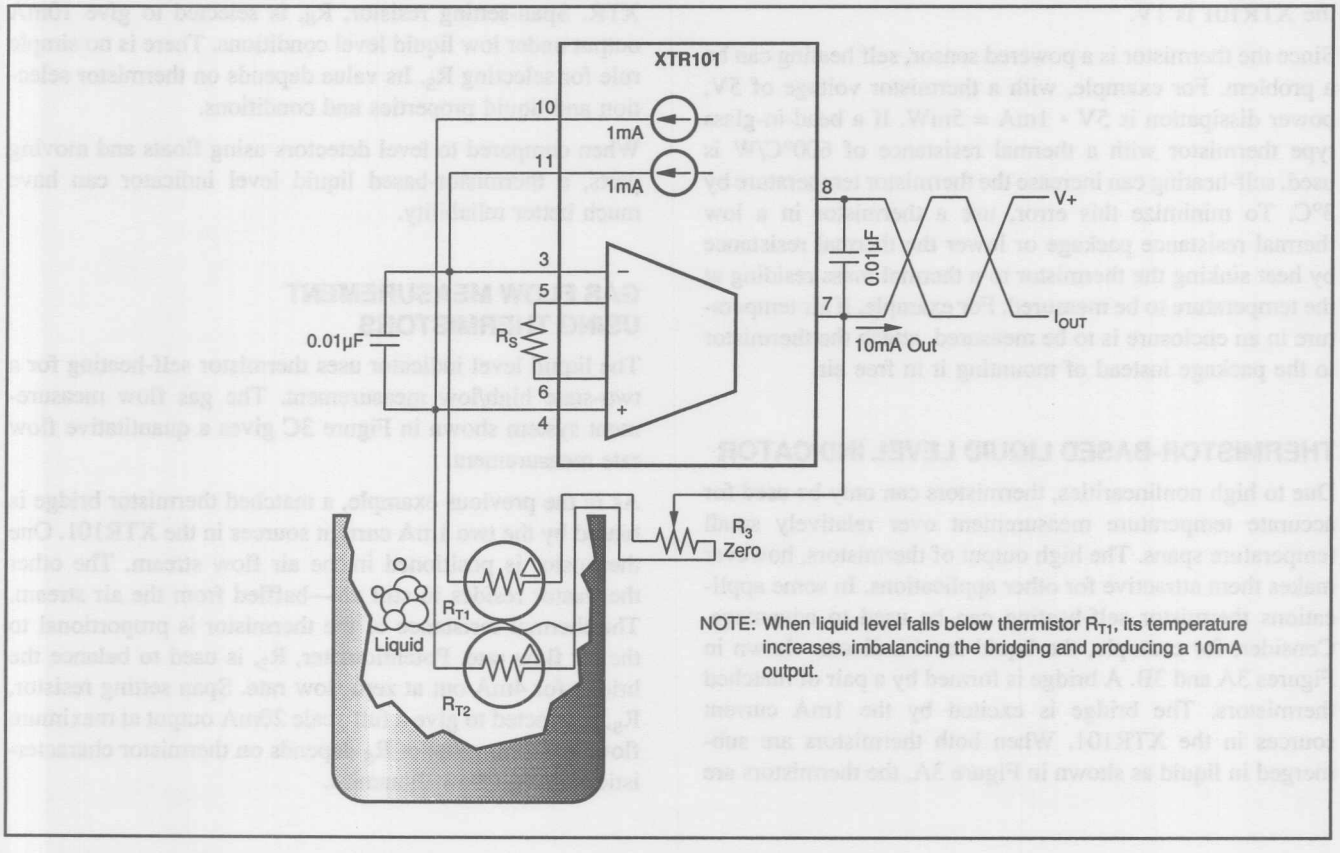


FIGURE 3B. Thermistor-Based Two-wire Liquid Level Detector Using XTR101.

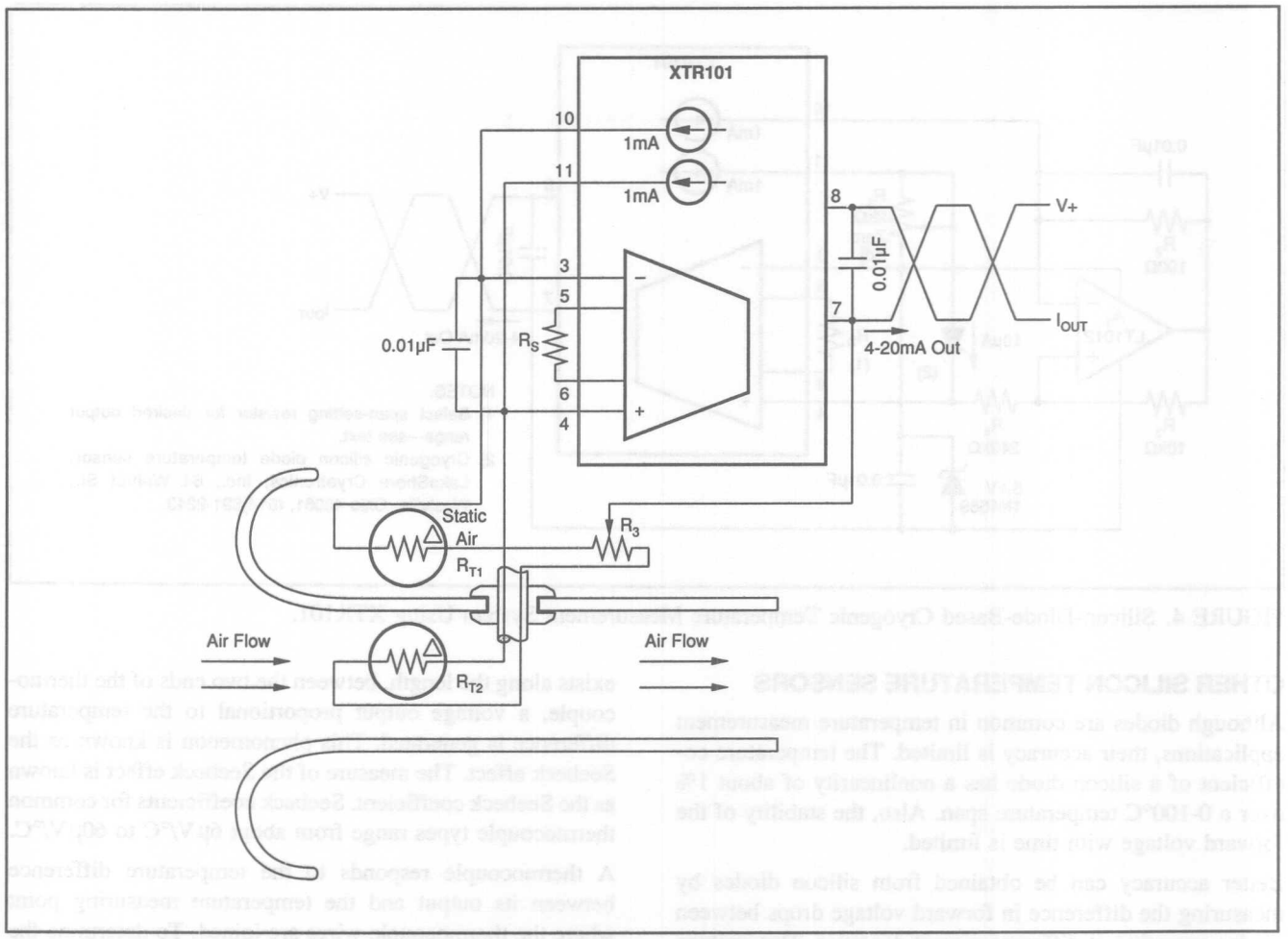


FIGURE 3C. Thermistor-Based Air Flow Rate Measurement Using XTR101.

Many systems today use resistance wire instead of thermistors for gas flow rate measurement. These are sometimes called hot-wire anemometers, and can have faster response due to lower (thermal mass)/(heat transfer) ratio.

DIODE-BASED TEMPERATURE MEASUREMENT

Cousin to the thermistor is the semiconductor diode temperature transducer. Regular silicon diodes, biased with constant current, have a forward voltage of about 0.6V with a temperature coefficient of about –2mV/°C. The usable upper temperature range for silicon semiconductors is about 125°C. Some high-temperature types are useful up to 200°C. In the future, novel semiconductor types such as silicon carbide and diamond promise to raise the upper usable temperature range of semiconductors into the 300°C to 600°C range. For now, thermocouples and RTDs can be used for higher temperature measurements.

Consider semiconductors for measurement of very low temperatures. Specialized silicon diodes can be used at very low temperatures. For example, the LakeShore Cryotronics, Inc., DT-470 series silicon diode cryogenic temperature sensor can be used to measure temperatures near absolute zero—from 1.4K to 475K.

Figure 4 shows a cryogenic temperature measurement circuit using a silicon diode temperature sensor. The sensor requires an accurate 10µA current source for excitation. One of the current sources from the XTR101 is scaled by a precision mirror to supply the 10µA excitation current.

To convert a 1mA current-source output into a precise 10µA for sensor excitation, a precision current mirror is formed with R_2, R_3, and A_1. The 1mA current source is connected to R_2 and the inverting input of the op amp. The op amp drives its inputs to the same voltage through R_3. The result is a precision 0.1V across both R_2 and R_3. The output current at the noninverting input is $1mA \cdot R_2/R_3 = 10\mu A$. With the amplifier specified, op amp bias currents add negligible error.

The other 1mA current source in the XTR101 supplies both a precision zero-set voltage and power for the op amp. The current source is connected to a 5.1V zener through R_1. The current through R_1 is precisely 1mA – 10µA. Zero-set voltage is $R_1 \cdot 990\mu A$. The 5.1V zener sets the supply voltage of the op amp. The 249kΩ resistor in series with the temperature sensor diode forces the op amp to operate in its linear common-mode and output ranges.

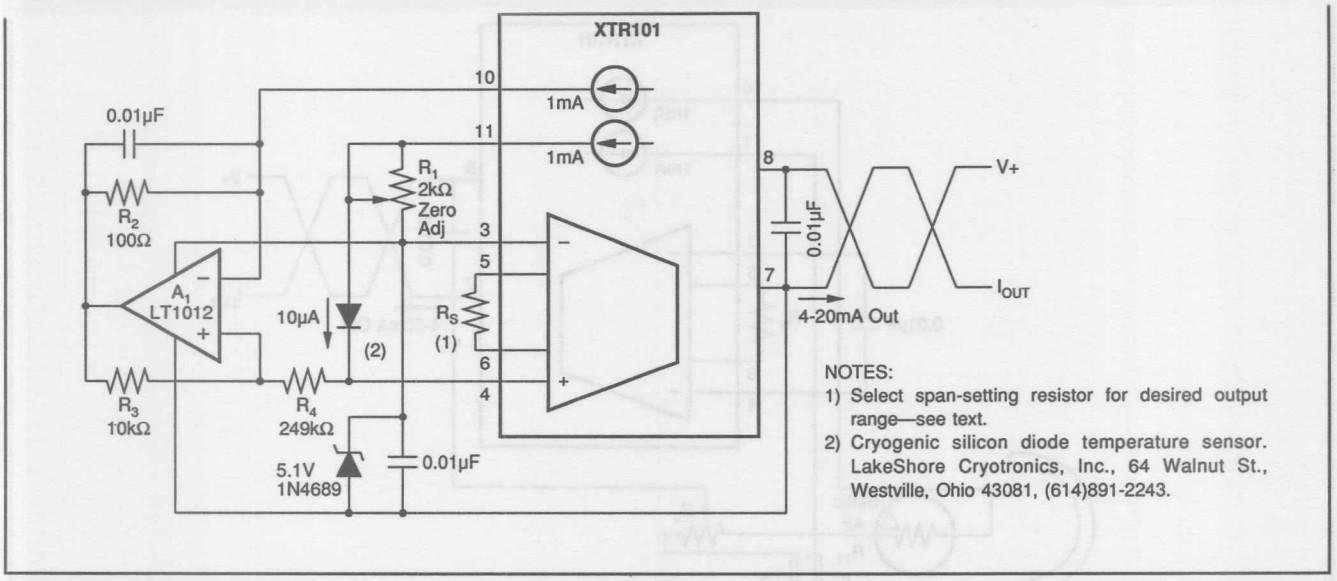


FIGURE 4. Silicon-Diode-Based Cryogenic Temperature Measurement System Using XTR101.

OTHER SILICON TEMPERATURE SENSORS

Although diodes are common in temperature measurement applications, their accuracy is limited. The temperature coefficient of a silicon diode has a nonlinearity of about 1% over a 0-100°C temperature span. Also, the stability of the forward voltage with time is limited.

Better accuracy can be obtained from silicon diodes by measuring the difference in forward voltage drops between diodes operating at different current densities. This voltage has a positive temperature coefficient proportional to absolute temperature. If the diodes have low bulk resistance and are well-matched, temperature coefficient linearity of better than 0.01% is possible.

THERMOCOUPLE-BASED TEMPERATURE MEASUREMENT

In the United States, the most commonly used precision temperature sensor is the thermocouple. Depending on the type, wire size, and construction, thermocouples can be used to measure temperatures from about –250°C up to 1700°C.

When designing thermocouple-based measurement systems, it is helpful to understand how thermocouples work. A common misconception is that temperature somehow creates an EMF in the thermocouple junction.

Thermocouples are based on the Thomson effect, which states that, in a single conductor, a voltage difference will exist between two points that are at different temperatures. The voltage difference is proportional to the temperature differential, and its magnitude and direction depends on the conductor material.

A thermocouple is formed when a pair of dissimilar conductors are connected at one end. If a temperature difference exists along the length, between the two ends of the thermocouple, a voltage output proportional to the temperature difference is generated. This phenomenon is known as the Seebeck effect. The measure of the Seebeck effect is known as the Seebeck coefficient. Seebeck coefficients for common thermocouple types range from about 6µV/°C to 60µV/°C.

A thermocouple responds to the temperature difference between its output and the temperature measuring point where the thermocouple wires are joined. To determine the temperature at the measuring point you must know the temperature at the thermocouple output. One way to do this is to keep the output in an ice bath at 0°C. Thermocouple calibration tables were derived this way, and, following tradition, the thermocouple output junctions have come to be known as *the cold junction.* In reality, the measurement junction may be colder.

In most modern thermocouple-based temperature measurement systems, the thermocouple output end simply resides at the ambient temperature. To compensate for variations in ambient temperature, a temperature-dependent voltage is summed with the thermocouple output. This method is known as cold-junction compensation.

A thermocouple-based 4-20mA temperature measurement system with cold-junction compensation is shown in Figure 5. In this application, a *type J* thermocouple is combined with an XTR101 to give a 4-20mA output for a 0-1000°C temperature change. One of the 1mA current sources in the XTR101 biases a silicon diode used as a temperature transducer for cold-junction compensation. For good accuracy, the thermocouple output junctions and the diode must be maintained at the same temperature. The diode has a forward-voltage temperature dependance of about –2mV/°C. The R_1, R_2 resistor divider attenuates the temperature depen-

dence to match the thermocouple Seebeck coefficient. The other 1mA current source is connected to R_3 for zero adjustment. The 2.5kΩ resistor establishes a 5V bias to keep the XTR101 IA in its linear range. Adjust R_3 for 4mA out with the thermocouple measurement end at 0°C. The span-setting resistor is chosen to give a 4-20mA output for the 58mV/1000°C thermocouple output. Nominal component values and Seebeck coefficients for recommended thermocouples are shown in the table in Figure 5 below.

RTD-BASED TEMPERATURE MEASUREMENT

The highest performance temperature measurement transducer in common use is the platinum resistance temperature detector (RTD). RTDs can be used to accurately measure temperatures from –200°C to 850°C. As with other temperature transducers, best performance requires correction for nonlinearities. The XTR103 is a special purpose 4-20mA current-loop transmitter with built-in circuitry for RTD linearization.

To understand how the linearization circuitry works, consider how an RTD works. In the range from 0°C to 850°C, the temperature/resistance relationship of a Pt-type RTD is:

$$RTD = R_0 \bullet (1 + A \bullet T + B \bullet T^2)$$

Where:
RTD = DC resistance value of RTD (Ω) at temperature T (°C)
R_0 = Value of RTD at 0°C (Ω)

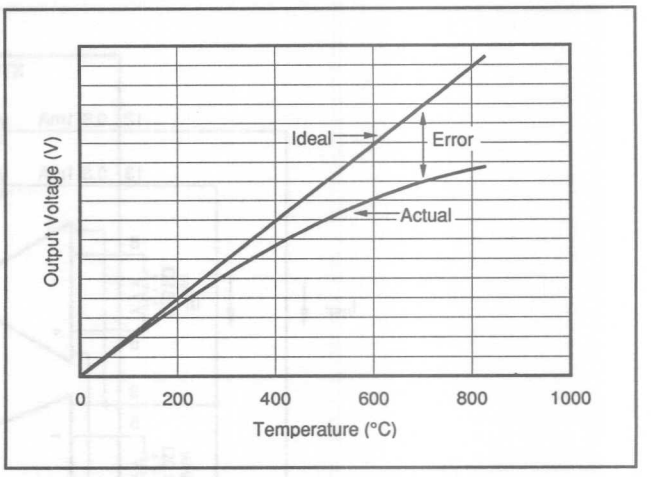
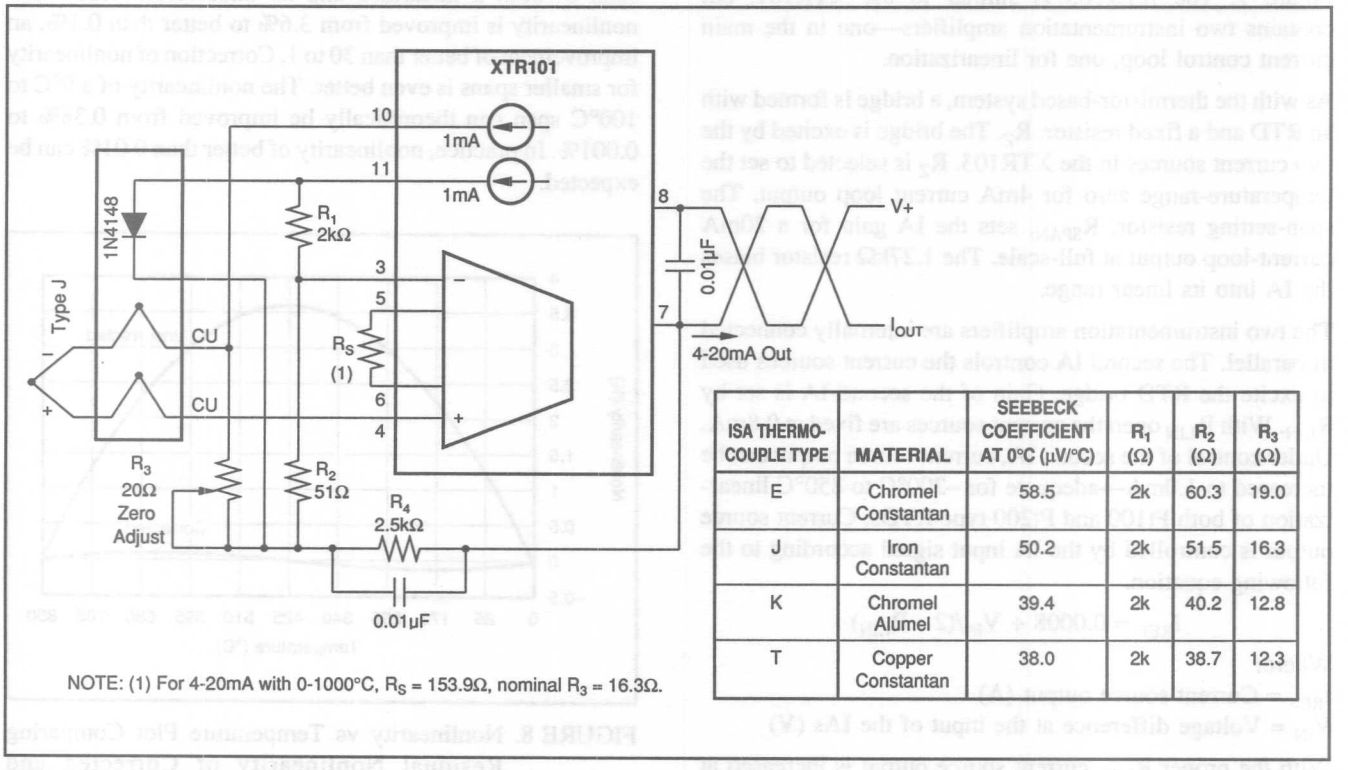


FIGURE 6. RTD Output Voltage vs Temperature.

R_0 = 100Ω for Pt100 = 200Ω for Pt200
A = Detector constant = 3.908×10^{-3} ($°C^{-1}$) (for Pt100)
B = Detector constant = -5.802×10^{-7} ($°C^{-2}$) (for Pt100)

The second-order term, $B \bullet T^2$, in the temperature/resistance relationship causes a nonlinearity in the response of ≈3.6% for a 0°C to 850°C temperature change. Figure 6 shows a plot of the voltage across an RTD with constant current excitation. The nonlinearity is exaggerated to show its characteristic shape. Increasing the current through the RTD by an appropriate amount as temperature increases will "straighten out" the curve and reduce the nonlinearity.



NOTE: (1) For 4-20mA with 0-1000°C, R_S = 153.9Ω, nominal R_3 = 16.3Ω.

ISA THERMOCOUPLE TYPE	MATERIAL	SEEBECK COEFFICIENT AT 0°C (µV/°C)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)
E	Chromel Constantan	58.5	2k	60.3	19.0
J	Iron Constantan	50.2	2k	51.5	16.3
K	Chromel Alumel	39.4	2k	40.2	12.8
T	Copper Constantan	38.0	2k	38.7	12.3

FIGURE 5. Thermocouple-Based Two-wire Temperature Measurement Using XTR101.

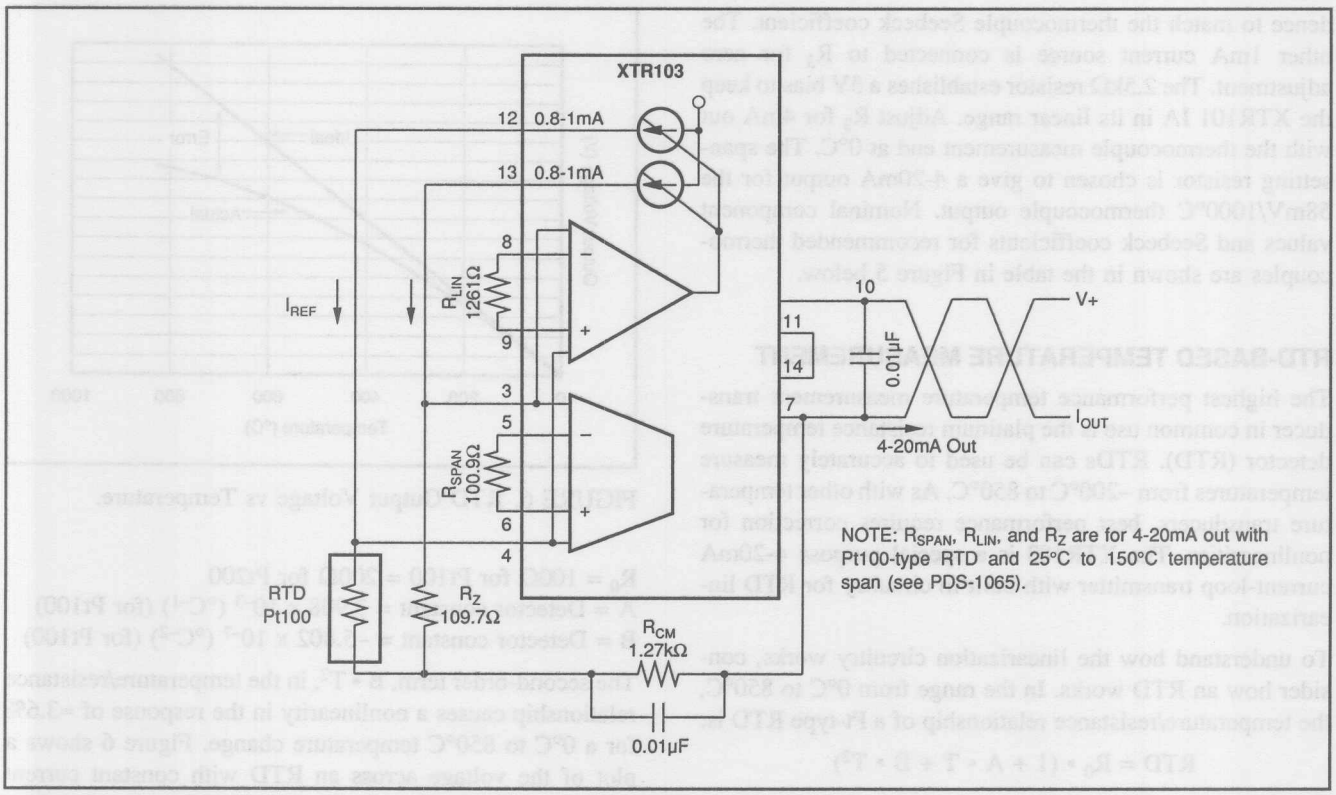


FIGURE 7. RTD-Based Two-wire Temperature Measurement Using XTR103.

An RTD measurement circuit using the XTR103 is shown in Figure 7. The XTR103 is similar to the XTR101, but contains two instrumentation amplifiers—one in the main current control loop, one for linearization.

As with the thermistor-based system, a bridge is formed with an RTD and a fixed resistor, R_Z. The bridge is excited by the two current sources in the XTR103. R_Z is selected to set the temperature-range zero for 4mA current loop output. The span-setting resistor, R_{SPAN}, sets the IA gain for a 20mA current-loop output at full-scale. The 1.27kΩ resistor biases the IA into its linear range.

The two instrumentation amplifiers are internally connected in parallel. The second IA controls the current sources used to excite the RTD bridge. Gain of the second IA is set by R_{LIN}. With R_{LIN} open the current sources are fixed at 0.8mA. Under control of the second IA, current source output can be increased to 1.0mA—adequate for –200°C to 850°C linearization of both Pt100 and Pt200 type RTDs. Current source output is controlled by the IA input signal according to the following equation.

$$I_{REF} = 0.0008 + V_{IN}/(2 \bullet R_{LIN})$$

Where:
I_{REF} = Current source output (A)
V_{IN} = Voltage difference at the input of the IAs (V)

With the proper R_{LIN}, current source output is increased at the correct rate to correct RTD nonlinearity. Simple selection procedures for R_{LIN} are outlined in the XTR product data sheet. Request PDS-1065.

Figure 8 shows the residual nonlinearity for a 0 to 850°C span of both a linearized and an uncorrected RTD. The nonlinearity is improved from 3.6% to better than 0.1%, an improvement of better than 30 to 1. Correction of nonlinearity for smaller spans is even better. The nonlinearity of a 0°C to 100°C span can theoretically be improved from 0.38% to 0.001%. In practice, nonlinearity of better than 0.01% can be expected.

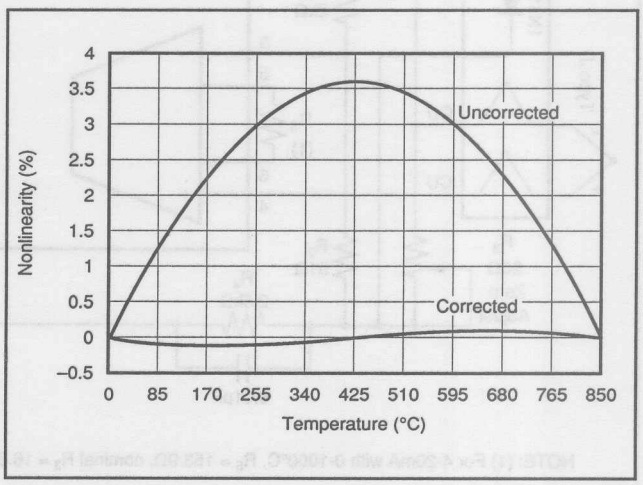


FIGURE 8. Nonlinearity vs Temperature Plot Comparing Residual Nonlinearity of Corrected and Uncorrected RTDs.

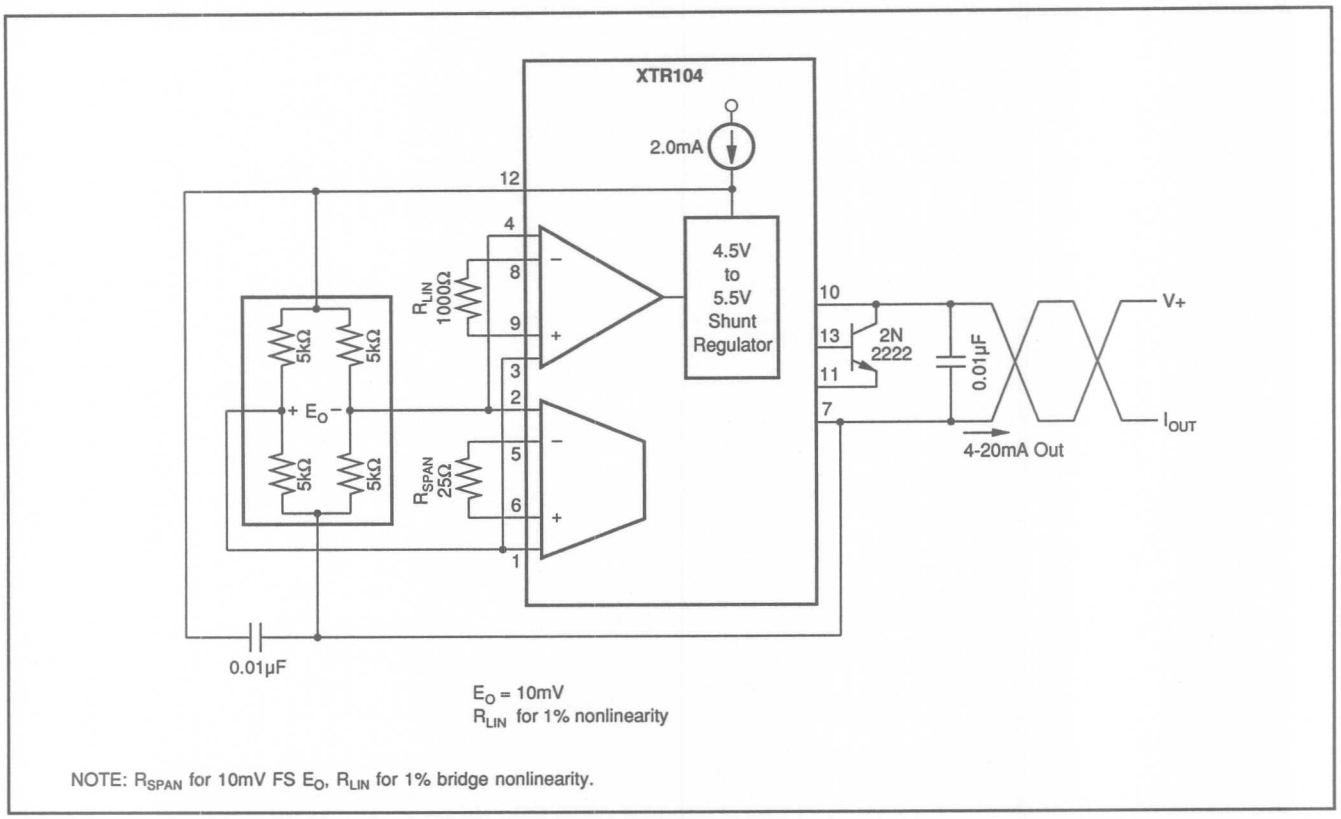


FIGURE 9. Bridge-Based Two-wire Measurement System Using XTR104.

BRIDGE MEASUREMENT 4-20mA CURRENT-LOOP SYSTEMS

Another common transducer is based on the four-resistor (Wheatstone) bridge. Wheatstone bridges are commonly used for pressure measurement. Bridges are usually intended to be biased with a voltage rather than a current source. By changing the voltage bias in response to the bridge output, bridge nonlinearities can be eliminated.

The XTR104 is a two-wire 4-20mA current loop transmitter designed specifically for use with bridges. It is similar to the XTR103 in that it contains two instrumentation amplifiers—one for signal, one for linearization. The difference is the addition of a 5V shunt regulator. The shunt regulator can be adjusted from 4.5V to 5.5V range under control of the second IA. The inputs to the second IA are brought out separately because, unlike RTD linearization, the correction signal may need to be either polarity for bridge linearizaton. Simple selection procedures for R_{LIN} are outlined in the XTR104 product data sheet. Request PDS-1066.

The complete bridge-based 4-20mA current loop transmitter circuit is shown in Figure 9. The XTR104 requires an external pass transistor as shown. Using an external pass device keeps power dissipation out of the XTR104 and improves accuracy. As an option, the XTR103 can use an external pass transistor. In either case, a garden variety bipolar transistor such as the 2N2222 shown is adequate.

Notice that, as with the other two-wire transmitters, only 2mA is available for bridge excitation. This means that, for accurate 5V regulation, bridge elements can be no less than 2.75kΩ unless additional resistance is added in series with the bridge.

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SINGLE-SUPPLY, LOW-POWER MEASUREMENTS OF BRIDGE NETWORKS

By Bonnie Baker (602) 741-3980

Bridge sensor measurements often need to be made in systems operating on a single 5V power supply. An OPA1013 dual op amp along with a REF200 current source, makes an excellent bridge measurement system which features low power single-supply 5V operation and immunity to power supply variations. One OPA1013 dual op amp is used as a two-op-amp instrumentation amplifier. A second OPA1013 is used with a REF200 to make two voltage references. One voltage reference is used to power the bridge, the other is used to offset the instrumentation amplifier.

In Figure 1, A_1 and A_2 (an OPA1013 dual operational amplifier) along with one of the current sources from the REF200 establishes a 3.4V voltage reference for excitation of a pressure transducer bridge. Although the REF200 contains two current sources, the second current source is not used, which keeps power consumption low.

A second OPA1013 (A_3, A_4), connected as a two op amp instrumentation amplifier, amplifies the differential voltage output from the bridge. Gain is easily adjusted with R_T. If 1% resistors are used for R_4-R_7, common-mode rejection will be better than 80dB for gains greater than 200V/V. A CMR of 80dB is quite acceptable in this application.

The instrumentation amplifier's reference connection is made to a 0.5V reference at the output of A_2. This voltage sets an instrumentation amplifier offset so that a zero bridge output will result in a 0.5V instrumentation amplifier output. The value of the offset can be changed by adjusting R_3.

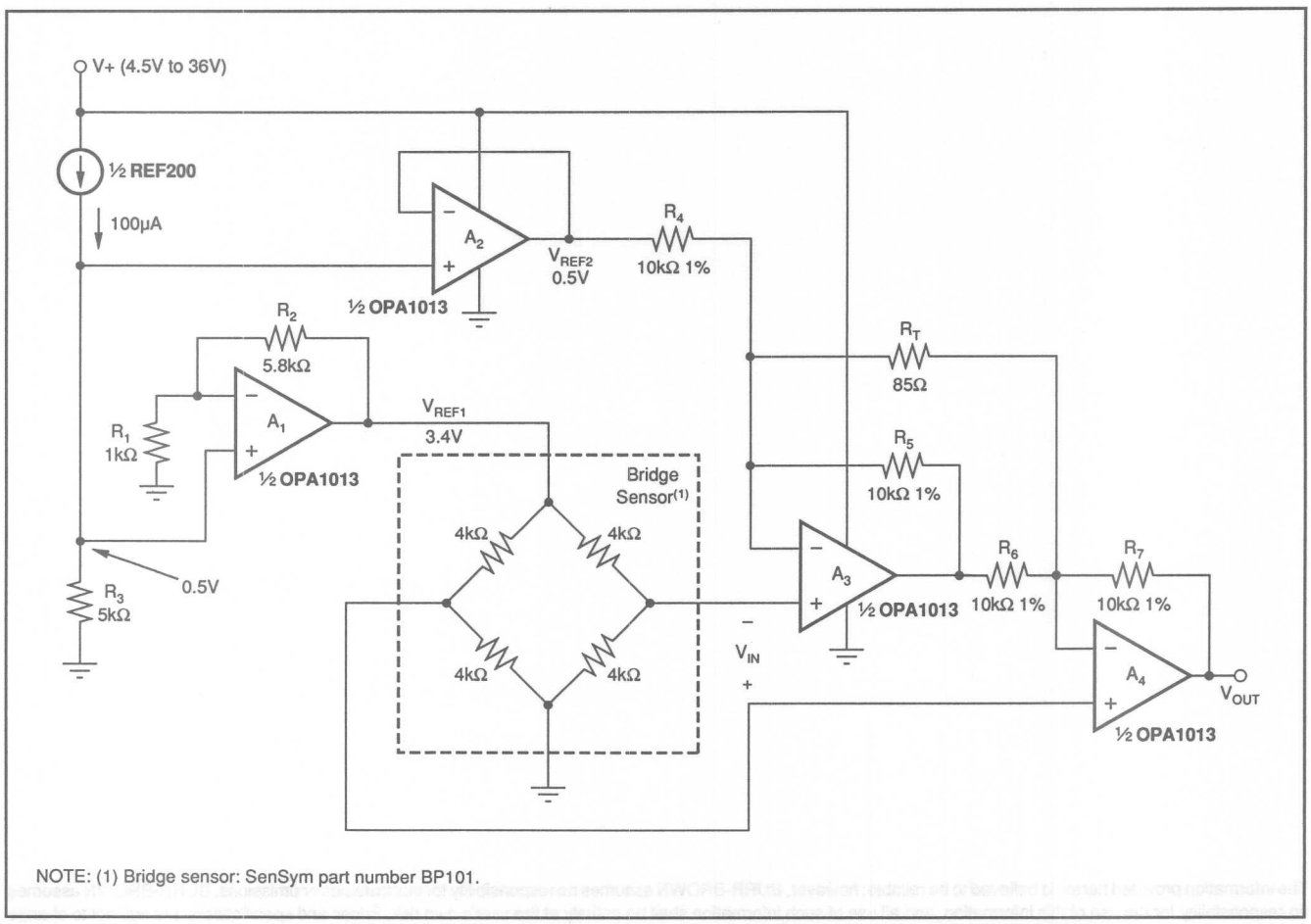

FIGURE 1. Single-Supply Bridge Measurement Circuit.

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For $V_{REF2} = 0.5V$, $R_3 = 5k\Omega$.

For $V_{REF1} = 3.4V$, $R_1 = 1k\Omega$, $R_2 = 5.8k\Omega$.

The required instrumentation amplifier gain can be calculated from its input voltage and the output span. The output voltage equation is:

$$V_{OUT} = V_{IN} [2(1 + R/R_T)] + V_{OUT1}$$

This equation can be rewritten as:

$$V_{OUT} = V_{IN} \cdot GAIN + V_{OUT1}$$

Where: $V_{OUT1} = V_{OUT}$ for zero instrumentation amplifier input or for zero pressure applied to the pressure transducer,

$$GAIN = -V_{OUT}/-V_{IN} = 2(1 + R/R_T)$$
$$R = R_4 = R_5 = R_6 = R_7$$

For example, a pressure sensor specified for 12.6mV full-scale output with 3.4V excitation voltage:

$$GAIN = 238V/V$$
$$\text{if } R = 10k\Omega, R_T = 85\Omega$$

If adjustment is required:

Adjustment Procedure

1. With zero-pressure applied, adjust R_3 for $V_{OUT} = 0.5V$.
2. Apply full-scale pressure to the sensor and adjust R_T for $V_{OUT} = 3.5V$.
3. Repeat procedure if necessary.

There is no true single-supply instrumentation amplifier on the market today. Although some come close, their applications are limited because they are fixed gain. The OPA1013 provides the best solution for this application because of its single supply operation and output swing range within 15mV from ground. The REF200 requires one power supply and is ideal for use in single supply systems. The REF200 provides a simple, economical way to make adjustable voltage references.

The supply voltage of the bridge conditioning circuit can range from 4.5V to 36V without affecting the operation of the circuit. Because of the low quiescent current of the OPA1013 (350μA) and the low current requirements of the REF200 (100μA), this is an excellent circuit for battery operated applications.

By R. Mark Stitt and David Kunst (602) 746-7445

Diodes are frequently used as temperature sensors in a wide variety of moderate-precision temperature measurement applications. The relatively high temperature coefficient of about –2mV/°C is fairly linear. To make a temperature measurement system with a diode requires excitation, offsetting, and amplification. The circuitry can be quite simple. This Bulletin contains a collection of circuits to address a variety of applications.

THE DIODE

Just about any silicon diode can be used as a temperature measurement transducer. But the Motorola MTS102 Silicon Temperature Sensor is a diode specifically designed and optimized for this function. It is intended for temperature sensing applications in automotive, consumer and industrial products where low cost and high accuracy are important. Packaged in a TO-92 package it features precise temperature accuracy of ±2°C from –40°C to +150°C.

EXCITATION

A current source is the best means for diode excitation. In some instances, resistor biasing can provide an adequate approximation, but power supply variations and ripple can cause significant errors with this approach. These problems are exacerbated in applications with low power supply voltages such as 5V single supply systems. Since the MTS102 is specified for 100µA operation, the Burr-Brown REF200 Dual 100µA Current Source/Sink makes the perfect match. One current source can be used for excitation and the other current source can be used for offsetting.

AMPLIFICATION

In most instances, any precision op amp can be used for diode signal conditioning. Speed is usually not a concern. When ±15V supplies are available, the low cost precision OPA177 is recommended. For 5V single-supply applications, the OPA1013 Dual Single-Supply op amp is recommended. Its inputs can common-mode to its negative power supply rail (ground in single-supply applications), and its output can swing to within about 15mV of the negative rail.

Figure 1 shows the simplest diode-based temperature measurement system. One of the 100µA current sources in the REF200 is used for diode excitation. The other current source is used for offsetting. One disadvantage of this circuit is that the span (GAIN) and zero (OFFSET) adjustments are interactive. You must either accept the initial errors or use an

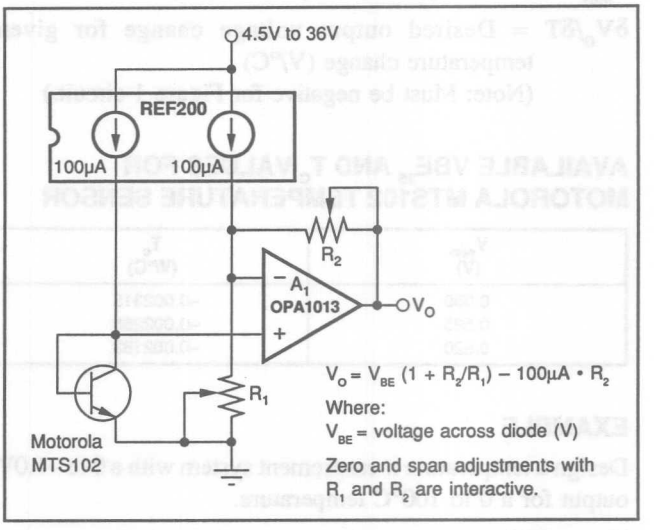

Figure 1. Simple Diode-based Temperature Measurement Circuit.

interactive adjustment technique. Another *possible* disadvantage is that the temperature to voltage conversion is inverting. In other words, a positive change in temperature results in a negative change in output voltage. If the output is to be processed in a digital system, neither of these limitations may be a disadvantage.

The following relationships can be used to calculate nominal resistor values for the Figure 1 circuit.

BASIC TRANSFER FUNCTION

$$V_O = V_{BE} (1 + R_2/R_1) - 100\mu A \bullet R_2$$

CALCULATING RESISTOR VALUES

$$R_1 = \frac{(\delta V_O/\delta T) \bullet (V_{BE25} + T_C \bullet (T_{MIN} - 25°C)) - (T_C \bullet V1)}{100\mu A \bullet ((\delta V_O/\delta T) - T_C)}$$

$$R_2 = R_1 \bullet \left(\frac{(\delta V_O/\delta T)}{T_C} - 1\right)$$

Where:

R_1, R_2 = Resistor values (Ω)

V_{BE} = Voltage across diode (V)

V_{BE25} = Diode voltage at 25°C (V)

Three choices are available for the MTS102—See table on page 2.

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V_1 = Output voltage of circuit at T_{MIN} (V)

V_O = Output voltage of circuit (V)

T_C = Diode temperature coefficient (V/°C)

T_C value depends on V_{BE25}—See table below.

T_{MIN} = Minimum process temperature (°C)

$\delta V_O/\delta T$ = Desired output voltage change for given temperature change (V/°C)
(Note: Must be negative for Figure 1 circuit.)

AVAILABLE VBE_{25} AND T_C VALUES FOR MOTOROLA MTS102 TEMPERATURE SENSOR

V_{BE25} (V)	T_C (V/°C)
0.580	–0.002315
0.595	–0.002265
0.620	–0.002183

EXAMPLE

Design a temperature measurement system with a 0 to –1.0V output for a 0 to 100°C temperature.

T_{MIN} = 0°C

$\delta V_O/\delta T$ = (–1V – 0V)/(100°C – 0°C) = –0.01V/°C

If V_{BE25} = 0.595V, T_C = –0.002265V/°C, and
R_1 = 8.424kΩ
R_2 = 28.77kΩ

For a 0 to –10V output with a 0 to 100°C temperature:
R_1 = 6.667kΩ
R_2 = 287.7kΩ

If independent adjustment of offset and span is required consider the circuit shown in Figure 2. In this circuit, a third resistor, R_{ZERO} is added in series with the temperature-sensing diode. System zero (offset) can be adjusted with R_{ZERO} without affecting span (gain). To trim the circuit adjust span first. Either R_1 or R_2 (or both) can be used to adjust span. As with the Figure 1 circuit this circuit has the possible disadvantage that the temperature to voltage conversion is inverting.

The following relationships can be used to calculate nominal resistor values for the Figure 2 circuit.

BASIC TRANSFER FUNCTION

$$V_O = (V_{BE} + 100\mu A \cdot R_{ZERO}) \cdot (1 + R_2/R_1) - 100\mu A \cdot R_2$$

CALCULATING RESISTOR VALUES

Set R_{ZERO} = 1kΩ (or use a 2kΩ pot)

$$R_1 = \frac{(\delta V_O/\delta T) \cdot (V_{BE25} + (R_{ZERO} \cdot 100\mu A) + T_C \cdot (T_{MIN} - 25°C)) - (T_C \cdot V_1)}{100\mu A \cdot ((\delta V_O/\delta T) - T_C)}$$

$$R_2 = R_1 \cdot \left(\frac{(\delta V_O/\delta T)}{T_C} - 1\right)$$

Where:

R_{ZERO} = Zero (offset) adjust resistor (Ω)

Others = as before

EXAMPLE

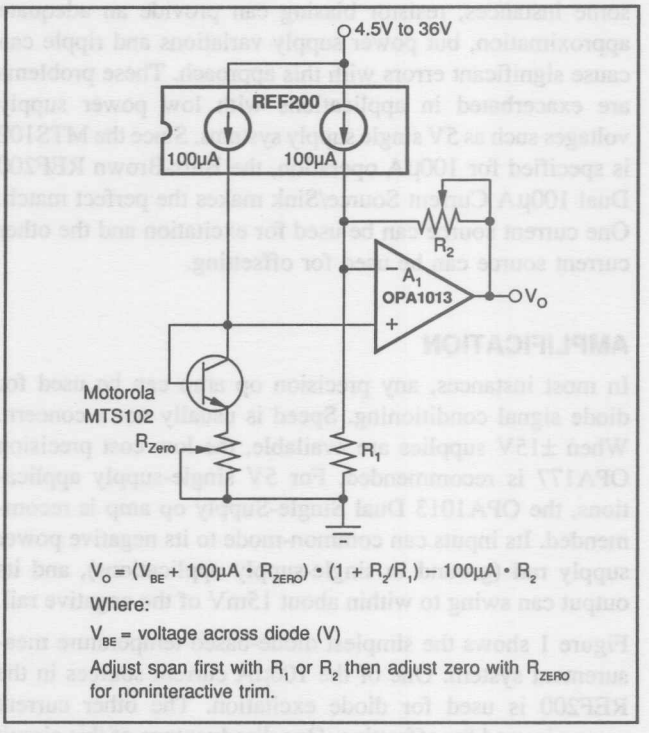
Design a temperature measurement system with a 0 to –1.0V output for a 0 to 100°C temperature.

T_{MIN} = 0°C

$\delta V_O/\delta T$ = (–1V – 0V)/(100°C – 0°C) = –0.01V/°C

If V_{BE25} = 0.595V, T_C = –0.002265V/°C, and
R_{ZERO} = 1kΩ (use 2kΩ pot)
R_1 = 9.717kΩ
R_2 = 33.18kΩ

For a 0 to –10V output with a 0 to 100°C temperature:
R_{ZERO} = 1kΩ (use 2kΩ pot)
R_1 = 7.69kΩ
R_2 = 331.8kΩ



$V_O = (V_{BE} + 100\mu A \cdot R_{ZERO}) \cdot (1 + R_2/R_1) - 100\mu A \cdot R_2$

Where:

V_{BE} = voltage across diode (V)

Adjust span first with R_1 or R_2 then adjust zero with R_{ZERO} for noninteractive trim.

Figure 2. Diode-based Temperature Measurement Circuit with Independent Span (gain) and Zero (offset) Adjustment.

For a noninverting temperature to voltage conversion, consider the circuit shown in Figure 3. This circuit is basically the same as the Figure 2 circuit except that the amplifier is connected to the low side of the diode. With this connection, the temperature to voltage conversion is noninverting. As before, if adjustment is required, adjust span with R_1 or R_2 first, then adjust zero with R_{ZERO}.

A disadvantage of the Figure 3 circuit is that it requires a negative power supply.

The following relationships can be used to calculate nominal resistor values for the Figure 3 circuit.

BASIC TRANSFER FUNCTION

$$V_O = (-V_{BE} - 100\mu A \bullet R_{ZERO}) \bullet (1 + R_2/R_1) + 100\mu A \bullet R_2$$

CALCULATING RESISTOR VALUES

R_1 = same as Figure 2
R_2 = same as Figure 2

Where:
Components = as before

EXAMPLE

Design a temperature measurement system with a 0 to 1.0V output for a 0 to 100°C temperature.

$T_{MIN} = 0°C$

$\delta V_O/\delta T = (1V - 0V)/(100°C - 0°C) = 0.01V/°C$

If $V_{BE25} = 0.595V$, $T_C = -0.002265V/°C$, and

$R_{ZERO} = 1k\Omega$
$R_1 = 9.717k\Omega$
$R_2 = 33.18k\Omega$

For a 0 to 10V output with a 0 to 100°C temperature:

$R_{ZERO} = 1k\Omega$
$R_1 = 7.69k\Omega$
$R_2 = 331.8k\Omega$

For a single-supply noninverting temperature to voltage conversion, consider the Figure 4 circuit. This circuit is similar to the Figure 2 circuit, except that the temperature-sensing diode is connected to the inverting input of the amplifier and the offsetting network is connected to the noninverting input. To prevent sensor loading, a second amplifier is connected as a buffer between the temp sensor and the amplifier. If adjustment is required, adjust span with R_1 or R_2 first, then adjust zero with R_{ZERO}.

The following relationships can be used to calculate nominal resistor values for the Figure 4 circuit.

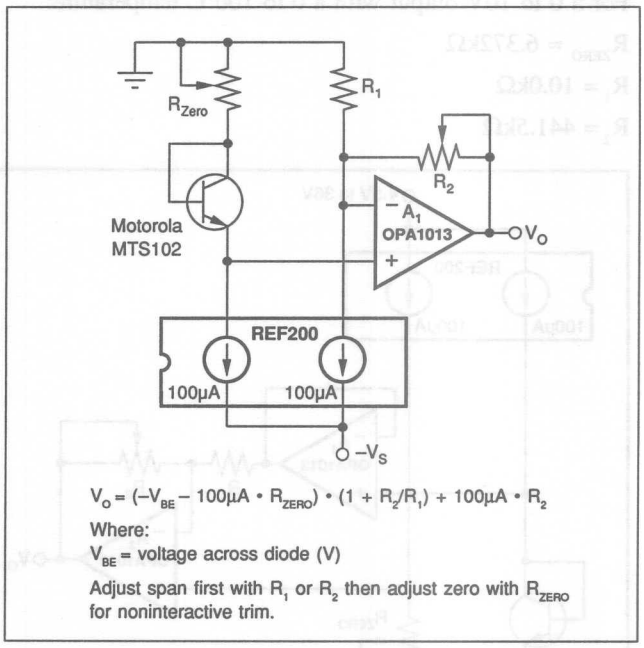


Figure 3. Positive Transfer Function Temperature Measurement Circuit with Independent Span (gain) and Zero (offset) Adjustment.

BASIC TRANSFER FUNCTION

$$V_O = 100\mu A \bullet R_{ZERO} \bullet (1 + R_2/R_1) - V_{BE} \bullet R_2/R_1$$

CALCULATING RESISTOR VALUES

$$R_{ZERO} = \frac{(T_C \bullet V_1) - (\delta V_O/\delta T) \bullet (V_{BE25} + T_C \bullet (T_{MIN} - 25°C))}{100\mu A \bullet (T_C - (\delta V_O/\delta T))}$$

$R_1 = 10k\Omega$ (arbitrary)

$$R_2 = -R_1 \bullet \left(\frac{(\delta V_O/\delta T)}{T_C}\right)$$

Where:
Components = as before

EXAMPLE

Design a temperature measurement system with a 0 to 1.0V output for a 0 to 100°C temperature.

$T_{MIN} = 0°C$

$\delta V_O/\delta T = (1V - 0V)/(100°C - 0°C) = 0.01V/°C$

If $V_{BE25} = 0.595V$, $T_C = -0.002265V/°C$, and

$R_{ZERO} = 5.313k\Omega$
$R_1 = 10.0k\Omega$
$R_2 = 44.15k\Omega$

For a 0 to 10V output with a 0 to 100°C temperature:

R_{ZERO} = 6.372kΩ

R_1 = 10.0kΩ

R_2 = 441.5kΩ

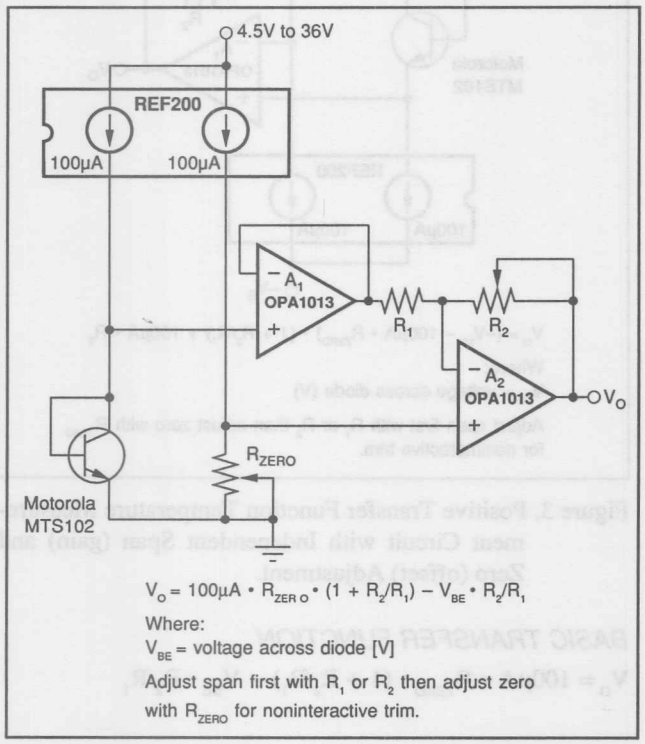


Figure 4. Single-supply Positive Transfer Function Temperature Measurement Circuit with Independent Span (gain) and Zero (offset) Adjustment.

For differential temperature measurement, use the circuit shown in Figure 5. In this circuit, the differential output between two temperature sensing diodes is amplified by a two-op-amp instrumentation amplifier (IA). The IA is formed from the two op amps in a dual OPA1013 and resistors R_1, R_2, R_3, R_4, and R_{SPAN}. R_{SPAN} sets the gain of the IA. For good common-mode rejection, R_1, R_2, R_3, and R_4 must be matched. If 1% resistors are used, CMR will be greater than 70dB for gains over 50V/V. Span and zero can be adjusted in any order in this circuit.

The following relationships can be used to calculate nominal resistor values for the Figure 5 circuit.

BASIC TRANSFER FUNCTION

$$V_O = ((V_{BE2} + 100\mu A \bullet R_{ZERO2}) - (V_{BE1} + 100\mu A \bullet R_{ZERO1})) \bullet GAIN$$

Where:

$$GAIN = 2 + 2 \bullet R_1/R_{SPAN}$$

CALCULATING RESISTOR VALUES

$$R_{SPAN} = \frac{-2 \bullet R_1 \bullet T_C}{(\delta V_O/\delta T) + 2 \bullet T_C}$$

$R_{ZERO1} = R_{ZERO2}$ = 500Ω (use 1kΩ pot for R_{ZERO})

Where:

R_{SPAN} = Span (gain) adjust resistor [Ω]

Others = as before

EXAMPLE

Design a temperature measurement system with a 0 to 1.0V output for a 0 to 1°C temperature differential.

T_{MIN} = 0°C

$\delta V_O/\delta T$ = (1V − 0V)/(1°C − 0°C) = 1.0V/°C

If V_{BE25} = 0.595V, T_C = −0.002265V/°C, and

R_{ZERO} = 1kΩ pot

R_1, R_2, R_3, R_4 = 100kΩ, 1%

R_{SPAN} = 455Ω

For a 0 to 10V output with a 0 to 1°C temperature differential:

R_{ZERO} = 1kΩ pot

R_1, R_2, R_3, R_4 = 100kΩ, 1%

R_{SPAN} = 45.3Ω

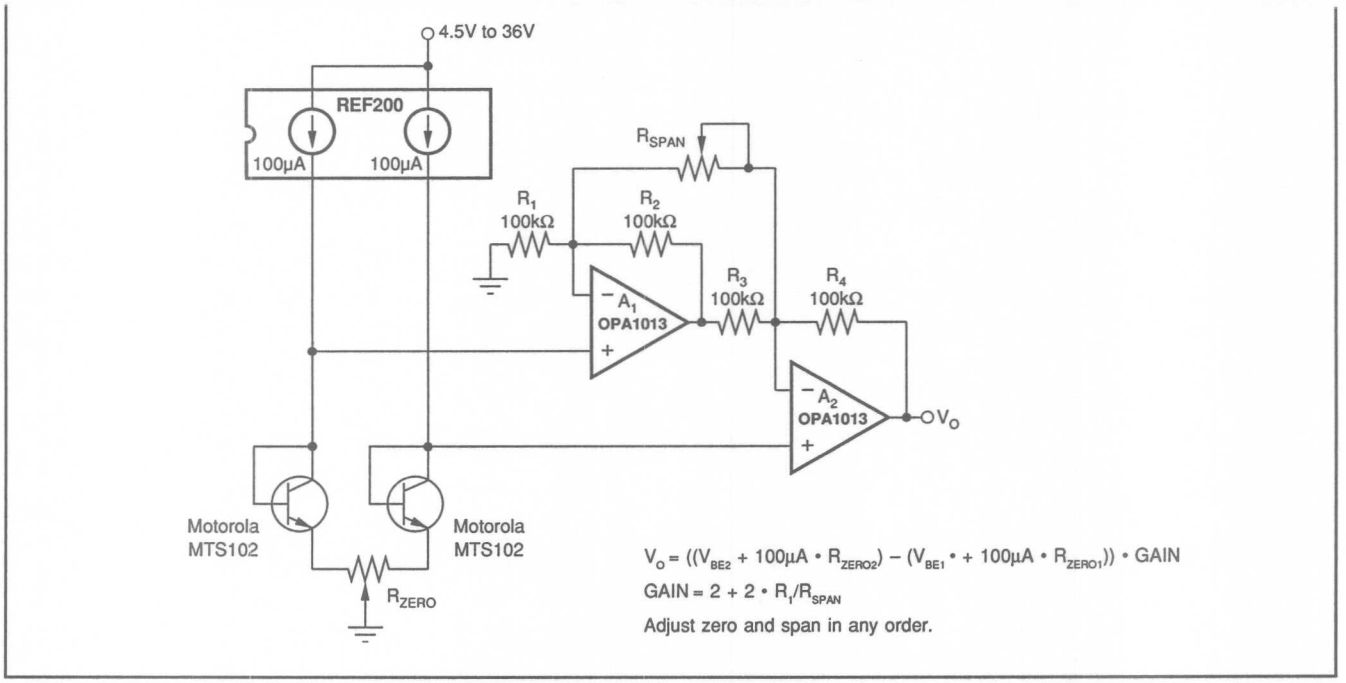


Figure 5. Differential Temperature Measurement Circuit.

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SINGLE-SUPPLY OPERATION OF ISOLATION AMPLIFIERS

By Rod Burt and R. Mark Stitt (602) 746-7445

For simplicity, many systems are designed to operate from a single external power supply. In battery powered systems such as aircraft and automotive, it's often a requirement. Isolation amplifiers such as the ISO120 and ISO122 can be easily modified for input side single-supply operation with the addition of an INA105 difference amplifier. With ISO amps, it's the isolated input side power supply which most often needs to be single supply. The output side of the ISO amp uses a split ±15V power supply, allowing a full ±10V output swing.

The difference amplifier has advantages as compared to traditional single-supply amplifiers. The inputs of a difference amplifier can swing to both the positive and negative power-supply rails. In fact, in the application shown in Figures 1 and 2, the input range of the circuit extends approximately 2V below ground (the negative power supply rail). This is because the resistors internal to the INA105 divide the input level in half as seen by the op amp.

The technique is illustrated in Figures 1 and 2 using the ISO120 and ISO122. These ISO amps are specified for operation from dual supplies as low as ±4.5V and can be operated with a total single power supply voltage as low as 9V. The circuit shown is designed for operation from a single +15V power supply. This allows a 0V to +5V input range.

The most common application is for a single ended input referred to ground as shown. For a differential input, pin 2 can be connected to a second input instead of ground. This provides a 0V to 5V differential input with common-mode to either rail.

To understand how the circuit works, consider the operation of the INA105 difference amplifier. The difference amplifier forces its output (pin 6) relative to its reference (pin 1) to be equal to the differential input (pin 3 – pin 2). The difference amplifier reference pin and the ISO amp common are held at approximately 5.1V by the 10kΩ resistor and the zener diode. This pseudo ground establishes an arbitrary acceptable operating point for the ISO amp. The difference amplifier then translates its input, relative to true ground, up to the 5.1V pseudo ground. In other words, a 0V to 5V input between pins 3 and 2 of the INA105 is seen as a 0V to 5V signal at the ISO amp input.

Isolated power is often at a premium and both the ISO120/122 and the INA105 operate on relatively low power. Common zener diodes, on the other hand, may require several mA for proper operation. The 1N4689 zener diode specified is a low level type designed for applications requiring low operating currents. It has a sharp breakdown voltage specified at a low 50μA.

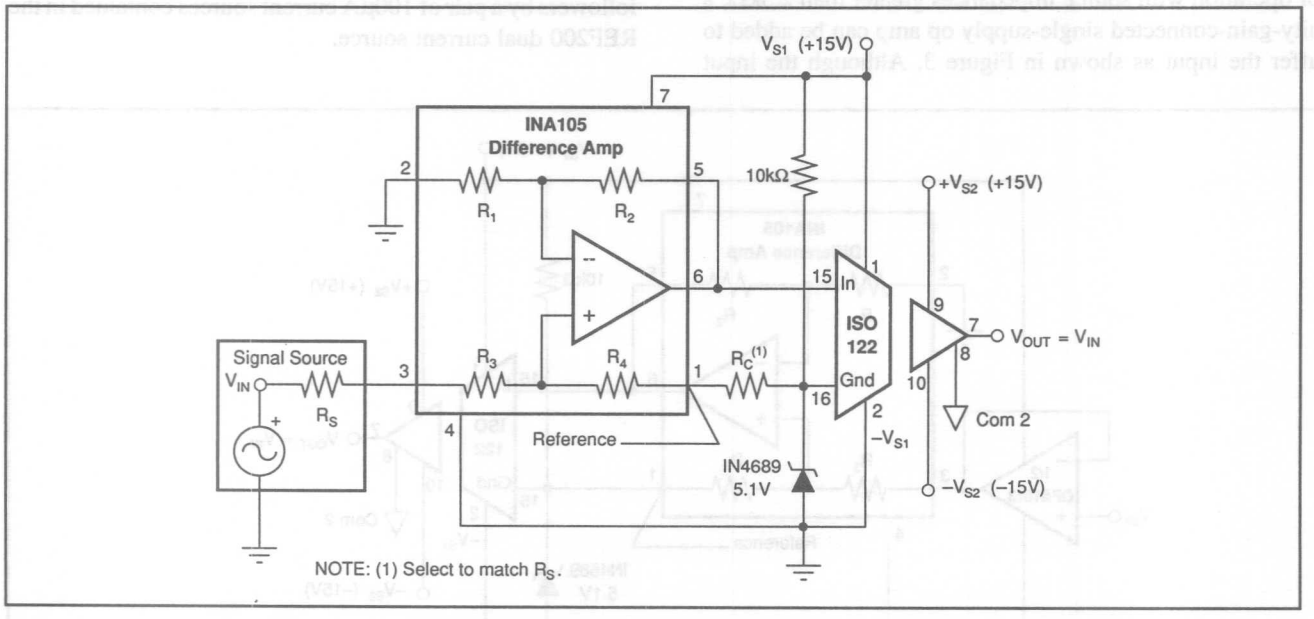

FIGURE 1. Single Supply Operation of the ISO122 Isolation Amplifier.

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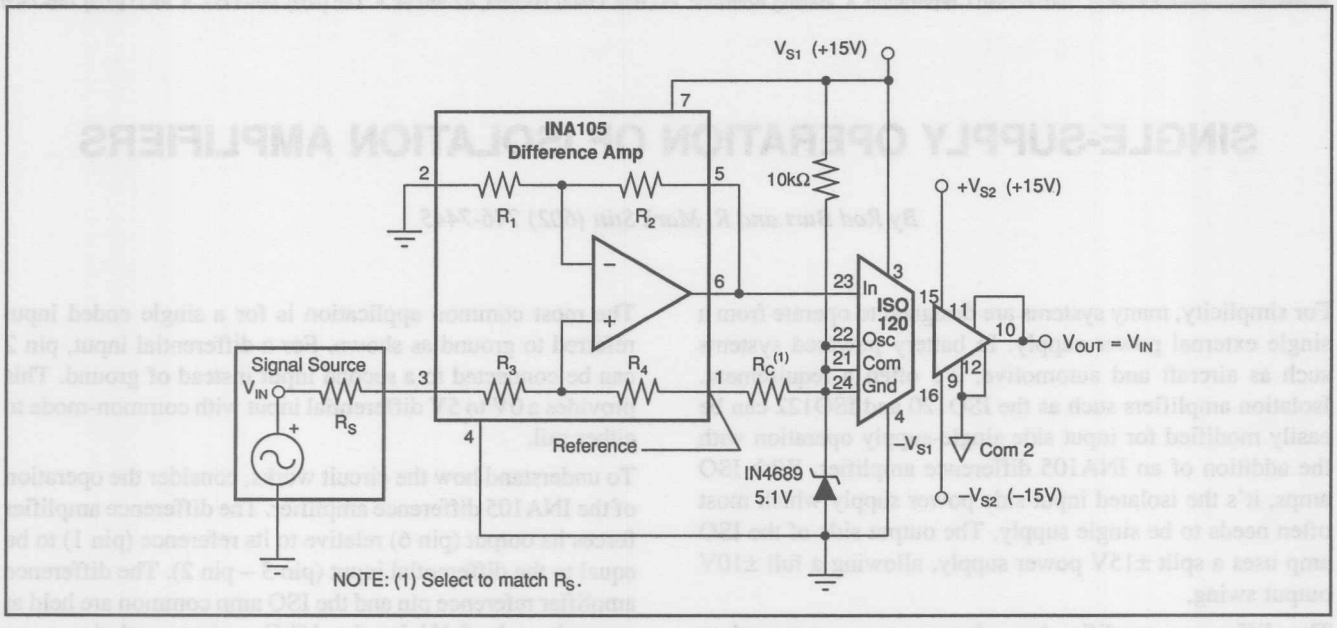

FIGURE 2. Single Supply Operation of the ISO120 Isolation Amplifier.

The accuracy of the INA105 difference amplifier relies on careful resistor ratio matching ($R_3/R_4 = R_1/R_2$). Any source impedance of the signal (R_S) adds to the difference resistor (R_3). For low source impedances, the error is acceptable. For better accuracy at higher source impedances, a compensating resistor (R_C) can be added to restore the ratio matching. The resistors in the INA105 are 25kΩ. For 0.1% gain accuracy, no compensating resistor is required with source impedances up to 25Ω. For source impedances up to 2.5kΩ, use a compensating resistor which matches R_S within 1%. If the source impedance is not known exactly, a trim pot can be used to adjust gain accuracy.

For operation with source impedances greater than 2.5kΩ, a unity-gain-connected single-supply op amp can be added to buffer the input as shown in Figure 3. Although the input range of the OPA1013 single-supply op amp includes the negative rail, its output can not quite swing all the way to the rail. The negative swing limit of this circuit is therefore ≈100mV—still adequate in many applications.

For an instrumentation amplifier (IA) front end, the other half of the OPA1013 can be connected to the inverting input of the INA105 (pin 2) as shown in Figure 4.

For a true single-supply ISO amp with high impedance differential inputs, the circuit shown in Figure 5 can be used. In this circuit, the inputs—and therefore the outputs—of the OPA1013s are level-shifted up a V_{BE} with a matched pair of PNP input transistors. The transistors are biased as emitter followers by a pair of 100µA current sources contained in the REF200 dual current source.

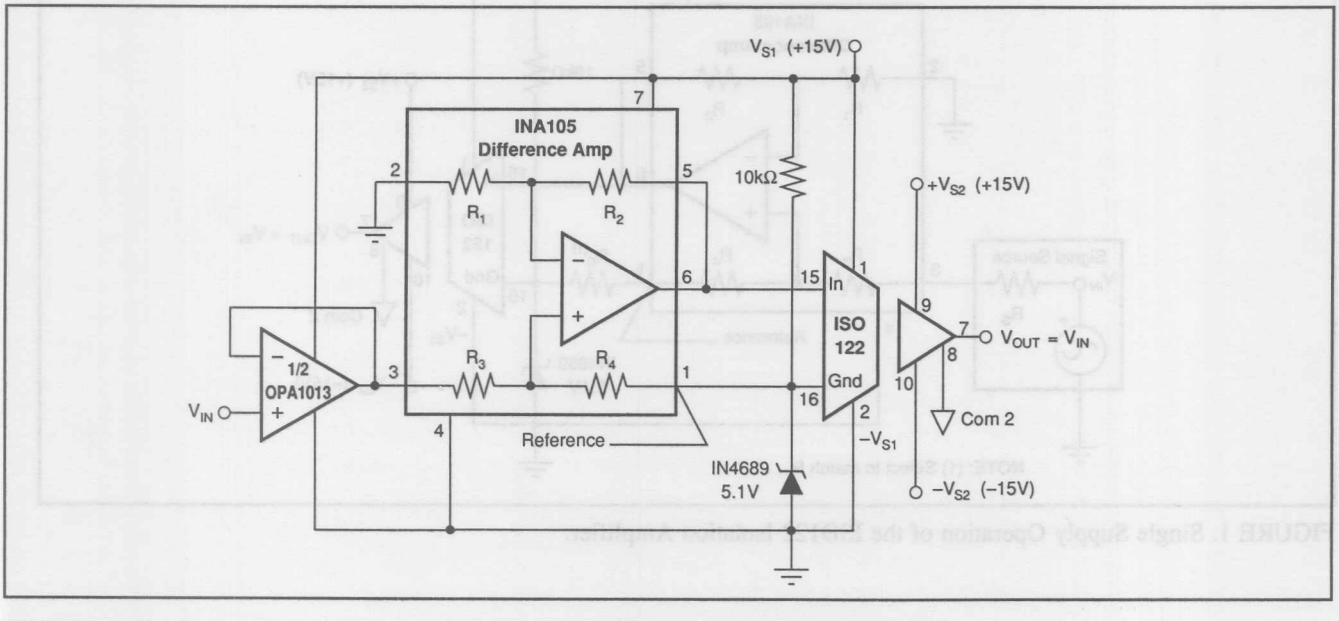

FIGURE 3. Single Supply (almost—see text), High Input Impedance Isolation Amplifier.

The circuits shown in this bulletin were designed for 0V to 5V operation from a single +15V power supply. With reduced range, operation from a lower voltage is feasible. For higher input range the circuit can be operated from a higher supply voltage. Table 1 shows the ranges obtainable for selected power supplies.

V_S (V)	INPUT RANGE FIGURES 1, 2 (V) [1]	INPUT RANGE FIGURES 3, 4 (V) [1]	INPUT RANGE FIGURE 5 (V) [1]
20+	–2 to +10	0.1 to +10	–0.3 to +10
15	–2 to +5	0.1 to +5	–0.3 to +5
12	–2 to +2	0.1 to +2	–0.3 to +2

Note: (1) Since the amplifier is unity gain, the input range is also the output range. The output can go to –2V since the output section of the ISO amp operates from dual supplies.

TABLE 1. Single-Supply ISO Amp Input Range vs Power Supply.

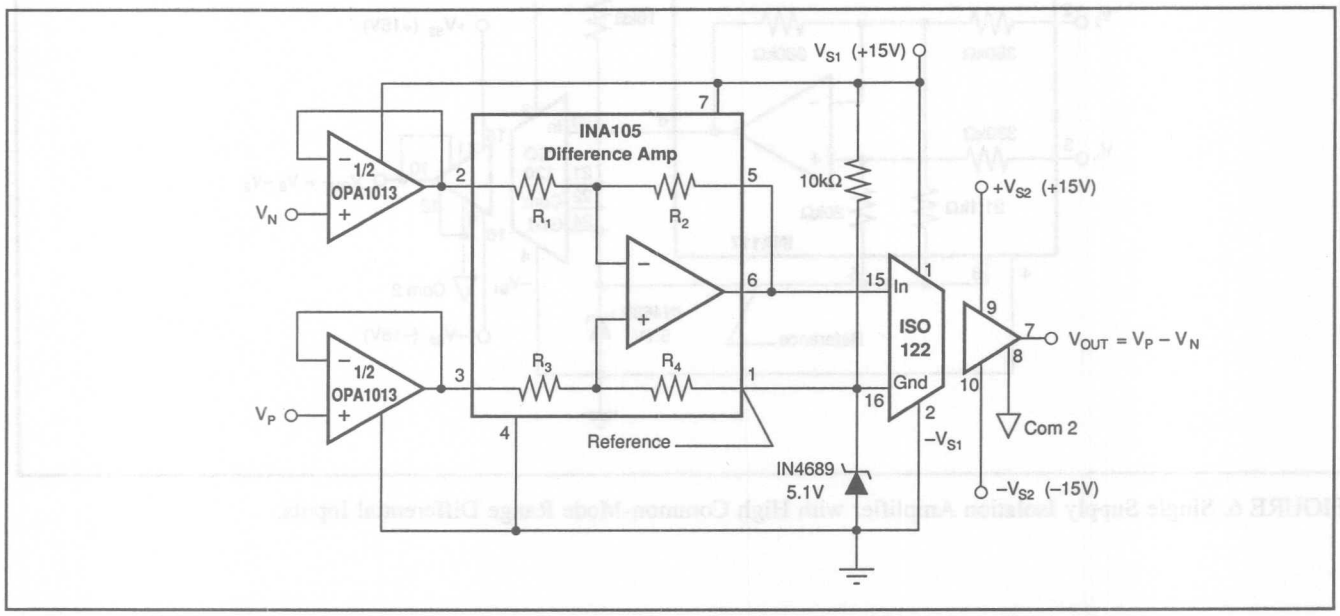

FIGURE 4. Single Supply (almost—see text), Isolation Amplifier with High-Impedance Differential Inputs..

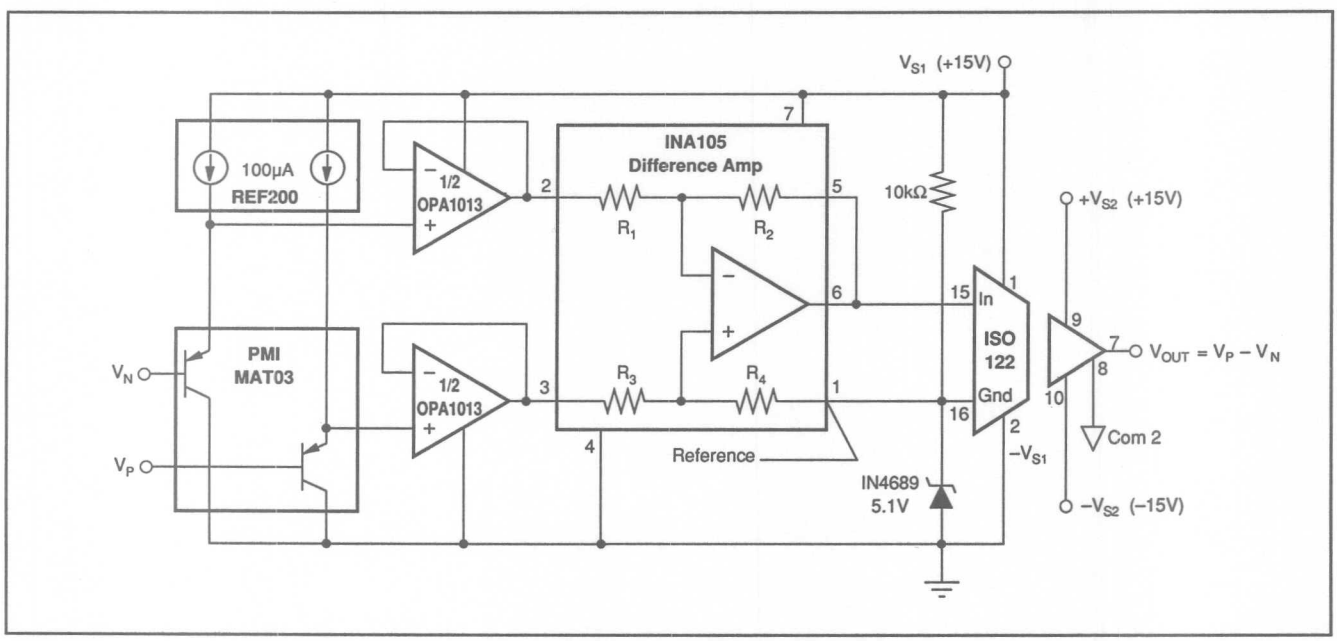

FIGURE 5. Single Supply Isolation Amplifier with High-Impedance Differential Inputs.

voltage differential inputs, an INA117 high common-mode voltage difference amplifier can be substituted for the INA105 difference amplifier as shown in Figure 6. With a +15V power supply, the input common mode range is approximately +125V, –50V. With a +12V supply, the input common mode range is approximately ±50V. Differential input range remains as shown in Table I for Figures 1 and 2.

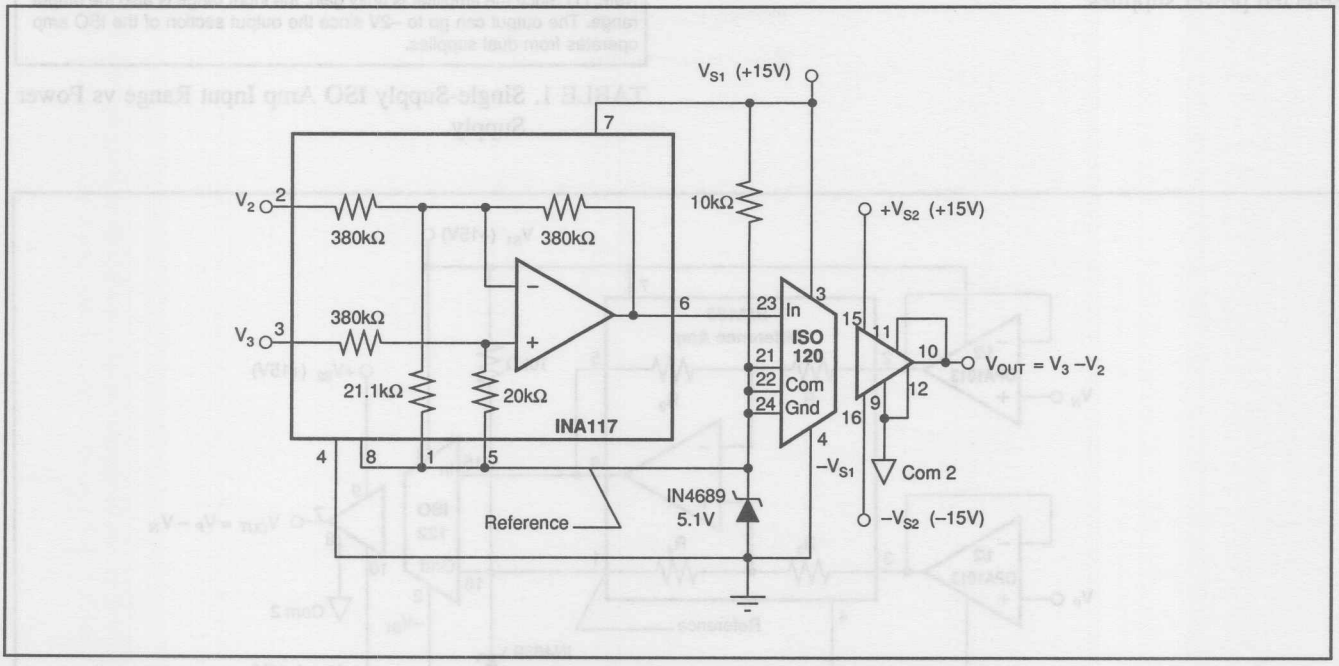

FIGURE 6. Single Supply Isolation Amplifier with High Common-Mode Range Differential Inputs.

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BOOST ISO120 BANDWIDTH TO MORE THAN 100kHz

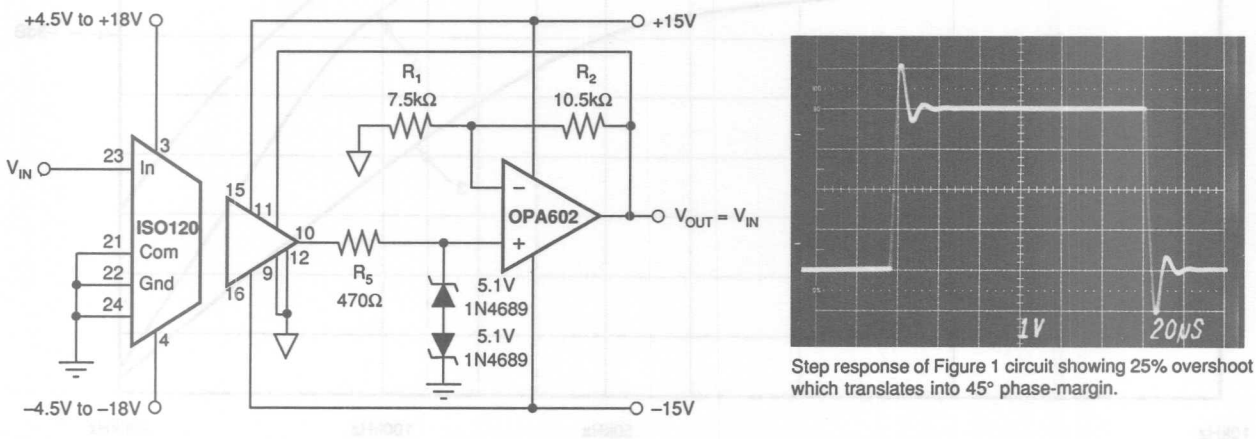
By R. Mark Stitt and Rod Burt (602) 746-7445

There has been considerable demand for high-bandwidth isolation amplifiers. The highest bandwidth Burr-Brown ISO amps are the ISO100 and the ISO120/121/122 family with bandwidths of about 50kHz. The ISO120/121 bandwidth can be boosted to more than 100kHz by adding gain in the feedback.

Adding gain in the feedback of the ISO120/121 increases bandwidth and decreases phase margin—see Figure 4. The ISO120 was designed with approximately 70° phase margin in the output stage for maximally flat magnitude response and a f_{-3dB} bandwidth of approximately 50kHz. With a gain of 2.4V/V in the feedback as shown in Figure 1, phase margin is decreased to an acceptable 45°. Due to gain peaking, the actual f_{-3dB} bandwidth is increased to almost 150kHz. With the addition of an input filter as shown in Figure 2, flat magnitude response with a bandwidth of greater than 100kHz is obtained. Since the added gain is within the ISO120 feedback loop, the overall gain of the isolation amplifier is unchanged (gain = 1).

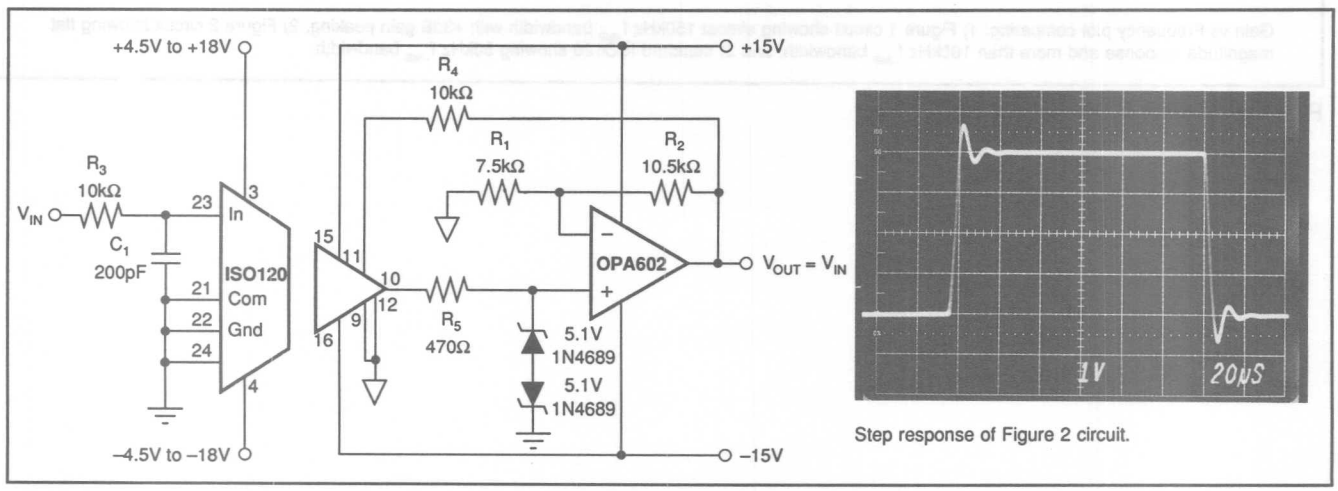
To verify the phase margin, analyze the step response of the Figure 1 circuit (shown in the Scope Photo 1). The 25% overshoot translates to a damping factor of 0.4 and 45° phase margin.

If the ISO120 is used in the clocked mode, maximum bandwidth is determined by the clock frequency. For 150kHz bandwidth and 45° phase margin with a gain of 2.4V/V in the ISO120 feedback, the clock frequency should be 500kHz. Lower clock frequencies will result in reduced phase margin and possible instability. Higher clock frequencies will result in better phase margin, but clock frequencies above 700kHz are not recommended.



Step response of Figure 1 circuit showing 25% overshoot which translates into 45° phase-margin.

FIGURE 1. ISO120 with f_{-3dB} Bandwidth Boosted to Approximately 150kHz.



Step response of Figure 2 circuit.

FIGURE 2. ISO120 with Flat Magnitude Response and f_{-3dB} Bandwidth Boosted to More Than 100kHz.

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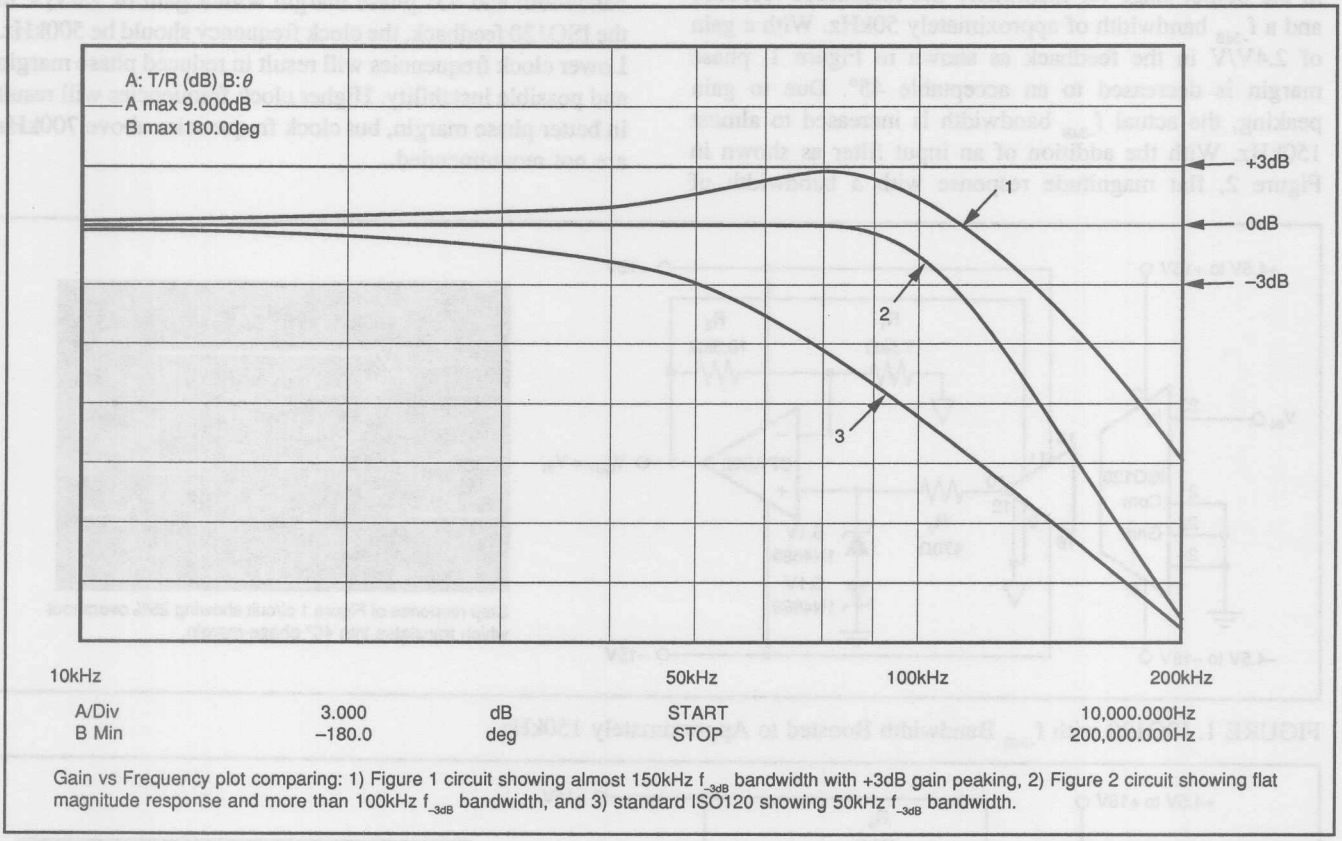
Adding gain in the feedback of the ISO120 can also increase its slew rate and full-power response. So long as the op amp providing gain in the feedback has adequate slew rate, the 2V/µs slew rate of the ISO120 is multiplied by its gain. When using an OPA602 with a gain of 2.4V/V in the feedback, the 30kHz 20Vp-p full-power response of the ISO120 is increased to more than 70kHz. Driving the OPA602 input below about –12V will cause signal inversion and possible circuit lock-up. The 470Ω/back-to-back zener network prevents possible lock-up by keeping the op amp input from being driven beyond its linear common-mode input range.

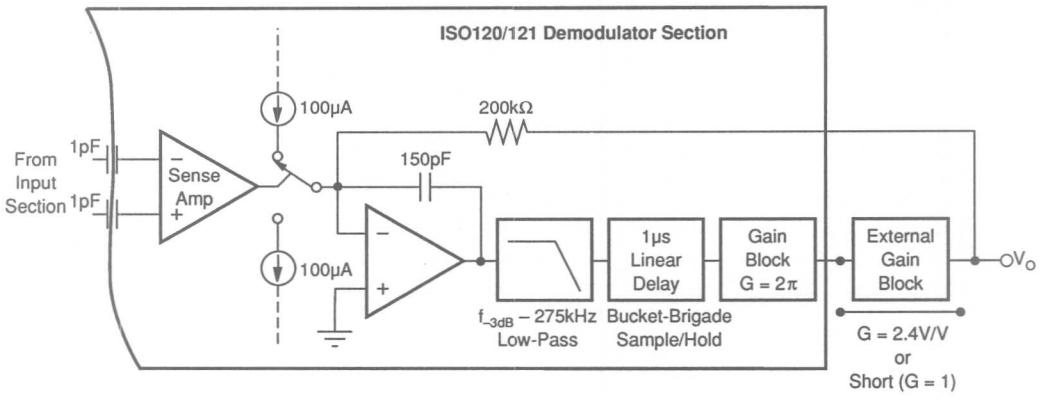
The addition of an input filter to compensate for the gain peaking, as shown in Figure 2, gives a flat magnitude response of more than 100kHz. In addition to the gain of 2.4V/V amplifier in the feedback, a simple 80kHz input filter formed by C_1 and R_3 is inserted at the input. The 10kΩ input resistor, R_3, decreases the ISO120 gain by about 5%. A matching 10kΩ resistor in the feedback, R_4, restores gain accuracy. The step response for the Figure 2 circuit is shown in the scope photo.

The Gain vs Frequency Plot, Figure 3, compares the response of the Figure 1 and Figure 2 circuits, to the standard ISO120. The top plot is the Figure 1 circuit showing about +3dB magnitude peaking and almost 150kHz f_{-3dB} bandwidth. The center plot is the Figure 2 circuit with the 80kHz input filter. The magnitude response is flat with an f_{-3dB} bandwidth greater than 100kHz. The bottom plot shows the standard ISO120 circuit with an f_{-3dB} bandwidth of about 50kHz.



Gain vs Frequency plot comparing: 1) Figure 1 circuit showing almost 150kHz f_{-3dB} bandwidth with +3dB gain peaking, 2) Figure 2 circuit showing flat magnitude response and more than 100kHz f_{-3dB} bandwidth, and 3) standard ISO120 showing 50kHz f_{-3dB} bandwidth.

FIGURE 3. Gain vs Frequency Plot.



The output demodulator section of the ISO120/121/122 consists of the integrator loop shown. This technique can not be applied to the ISO122 because the feedback connection is not available externally. Stability is determined by the phase margin at the open-loop response unity gain point, f_{UG}.

The unity-gain frequency is:

$$f_{UG} = \frac{6.28 \cdot gain_{EXT}}{2 \cdot \pi\ (200k\Omega) \cdot (150pF)} = 33kHz \cdot gain_{EXT}$$

The phase margin is approximated by:

$$180° - \underbrace{90°}_{\substack{200k\Omega,\ 150pF \\ integrator}} - \underbrace{\tan^{-1}(f_{UG}/275kHz)}_{\substack{higher\ order \\ poles}} - \underbrace{1\mu s \cdot f_{UG} \cdot 360°}_{\substack{sample/hold \\ delay^*}}$$

*The sample/hold delay is $1/(2 \cdot freq_{CLK})$. For a 500kHz clock frequency, the delay is 1µs. The free-running clock frequency is approximately 500kHz.

For $gain_{EXT} = 1$:

f_{UG} = 33kHz, Phase Margin = 70°, and

f_{-3dB} = 50kHz

For $gain_{EXT} = 2.4$:

f_{UG} = 80kHz, phase margin = 45°, and

f_{-3dB} = 150kHz with +3dB gain peaking at 80kHz.

FIGURE 4. Analysis of ISO120/121 Demodulator Section.

SYNCHRONIZATION OF ISO120/121 ISOLATION AMPLIFIERS

By Rod Burt and R. Mark Stitt (602) 746-7445

Internal clock circuitry in the ISO120/121 precision isolation amplifier (ISO amp) can be synchronized to an external clock signal. Synchronization to an external clock can be used to eliminate beat frequencies in multichannel systems or for rejection of specific AC signals and their harmonics—see the ISO120/121 product data sheet, PDS-820.

The external clock signal can be directly connected to the ISO120/121 if it is a sine or triangle wave of the proper amplitude. At clock frequencies above 400kHz, a square wave external clock can also be directly connected to the ISO120/121. Other clock signals can be used with the addition of the signal conditioning circuit shown in Figure 2.

SYNCHRONIZING TO A SINE OR TRIANGLE WAVE EXTERNAL CLOCK

The ideal external clock signal for the ISO120/121 is a ±4V sine wave or ±4V, 50% duty-cycle triangle wave. The *ext osc* pin of the ISO120/121 can be driven directly with a ±3V to ±5V sine or 25% to 75% duty-cycle triangle wave and the ISO amp's internal modulator/demodulator circuitry will synchronize to the signal.

EXTERNAL CLOCK FREQUENCY RANGE	C_1, C_2 ISO120/121 MODULATOR, DEMODULATOR EXTERNAL CAPACITOR
400kHz to 700kHz	none
200kHz to 400kHz	500pF
100kHz to 200kHz	1000pF
50kHz to 100kHz	2200pF
20kHz to 50kHz	4700pF
10kHz to 20kHz	0.01µF
5kHz to 10kHz	0.022µF

TABLE I. Recommended ISO120/121 External Modulator/Demodulator Capacitor Values vs External Clock Frequency.

EXTERNAL CLOCK FREQUENCY RANGE	C_x
400kHz to 700kHz	30pF
200kHz to 400kHz	180pF
100kHz to 200kHz	680pF
50kHz to 100kHz	1800pF
20kHz to 50kHz	3300pF
10kHz to 20kHz	0.01µF
5kHz to 10kHz	0.022µF

TABLE II. Recommended C_x Values vs Frequency for Figure 2 Circuit.

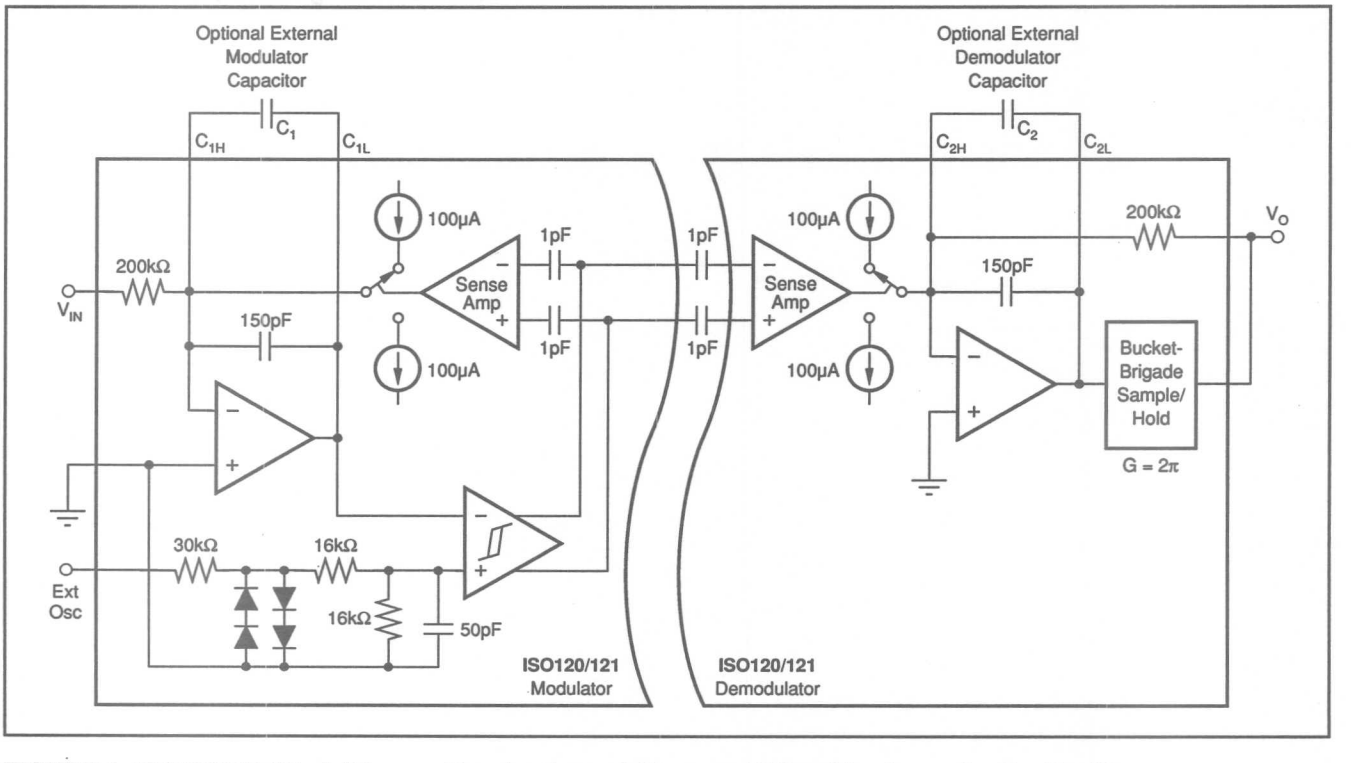


FIGURE 1. ISO120/121 Block Diagram Showing Internal Clamp and Filter Circuitry at the Ext Osc Pin.

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Synchronizing to signals below 400kHz requires the addition of two external capacitors to the ISO120/121. Connect one capacitor in parallel with the internal modulator capacitor and connect the other capacitor in parallel with the internal demodulator capacitor as shown in Figure 1.

The value of the external modulator capacitor, C_1, depends on the frequency of the external clock signal. Table I lists recommended values.

The value of the external demodulator capacitor, C_2, depends on the value of the external modulator capacitor. To assure stability, C_2 must be greater than $0.8 \cdot C_1$. A larger value for C_2 will decrease bandwidth and improve stability:

$$f_{-3dB} \approx \frac{1.2}{200k\Omega\,(150pF + C_2)}$$

Where:

$f_{-3dB} \approx -3dB$ bandwidth of ISO amp with external C_2 (Hz)

C_2 = External demodulator capacitor (F)

For example, with $C_2 = 0.01\mu F$, the f_{-3dB} bandwidth of the ISO120/121 is approximately 600Hz.

SYNCHRONIZING TO A 400kHz TO 700kHz SQUARE-WAVE EXTERNAL CLOCK

At frequencies above 400kHz, an internal clamp and filter provides signal conditioning so that a square-wave signal can be used to directly drive the ISO120/121. A square-wave external clock signal can be used to directly drive the ISO120/121 *ext osc* pin if: the signal is in the 400kHz to 700kHz frequency range with a 25% to 75% duty cycle, and ±3V to ±20V level. Details of the internal clamp and filter circuitry are shown in Figure 1.

SYNCHRONIZING TO A 10% TO 90% DUTY-CYCLE EXTERNAL CLOCK

With the addition of the signal conditioning circuit shown in Figure 2, any 10% to 90% duty-cycle square-wave signal can be used to drive the ISO120/121 ext osc pin. With the values shown, the circuit can be driven by a 4Vp-p TTL signal. For a higher or lower voltage input, increase or decrease the 1kΩ resistor, R_X, proportionally. e.g. for a ±4V square wave (8Vp-p) R_X should be increased to 2kΩ.

The value of C_X used in the Figure 2 circuit depends on the frequency of the external clock signal. Table II shows recommended capacitor values.

Note: For external clock frequencies below 400kHz, external modulator/demodulator capacitors are required on the ISO120/121 as before.

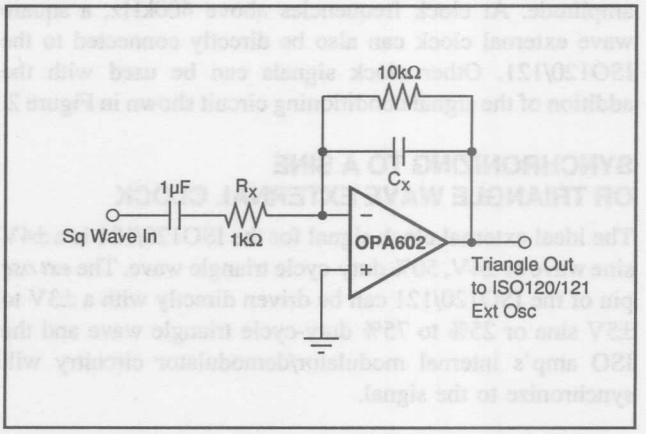

FIGURE 2. Square Wave to Triangle Wave Signal Conditioner for Driving ISO120/121 Ext Osc Pin.

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SIMPLE OUTPUT FILTER ELIMINATES ISO AMP OUTPUT RIPPLE AND KEEPS FULL BANDWIDTH

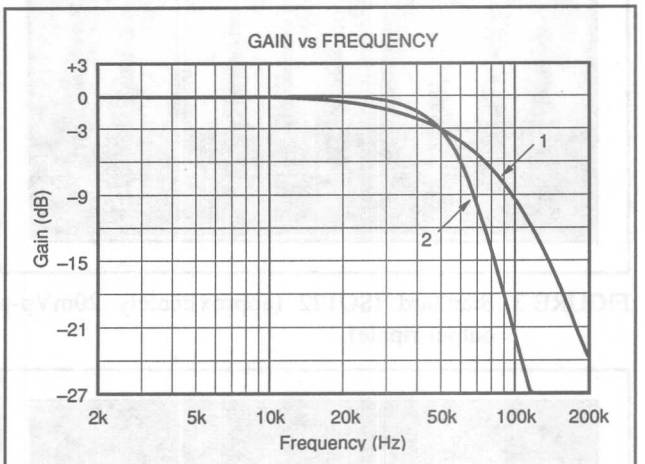
By Mark Stitt (602) 746-7445

The ISO120/121/122 isolation amplifiers (ISO amps) have a small (10-20mVp-p typ) residual demodulator ripple at the output. A simple filter can be added to eliminate the output ripple without decreasing the 50kHz signal bandwidth of the ISO amp.

The ISO120/121/122 is designed to have a 50kHz single-pole (Butterworth) signal response. By cascading the ISO amp with a simple 50kHz, Q = 1, two-pole, low-pass filter, the overall signal response becomes three-pole Butterworth. The result is a maximally flat 50kHz magnitude response and the output ripple reduced below the noise level.

Figure 1 shows the complete circuit. The two-pole filter is a unity-gain Sallen-Key type consisting of A_1, R_1, R_2, C_1, and C_2. The values shown give Q = 1 and f_{-3dB} bandwidth = 50kHz. Since the op amp is connected as a unity-gain follower, gain and gain accuracy of the ISO amp are unaffected. Using a precision op amp such as the OPA602 also preserves the DC accuracy of the ISO amp.

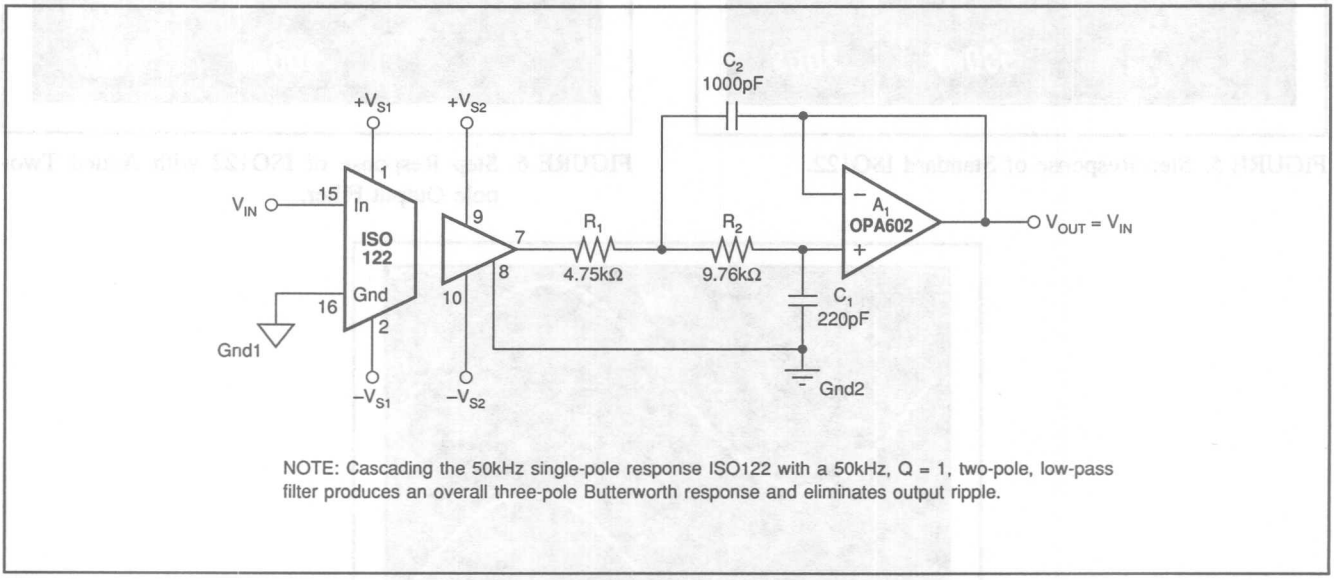
Figure 2 compares the magnitude response of the standard and filtered ISO amp. Figures 3 and 4 show the output ripple improvement. Figures 5 and 6 show the good step response of both the standard and filtered ISO amp.



1) Standard ISO122 has 50kHz single-pole (Butterworth) response.

2) ISO122 with cascaded 50kHz, Q = 1, two-pole, low-pass filter has three-pole Butterworth response.

FIGURE 2. Gain vs Frequency Plot.



NOTE: Cascading the 50kHz single-pole response ISO122 with a 50kHz, Q = 1, two-pole, low-pass filter produces an overall three-pole Butterworth response and eliminates output ripple.

FIGURE 1. ISO122 with Output Filter for Improved Ripple.

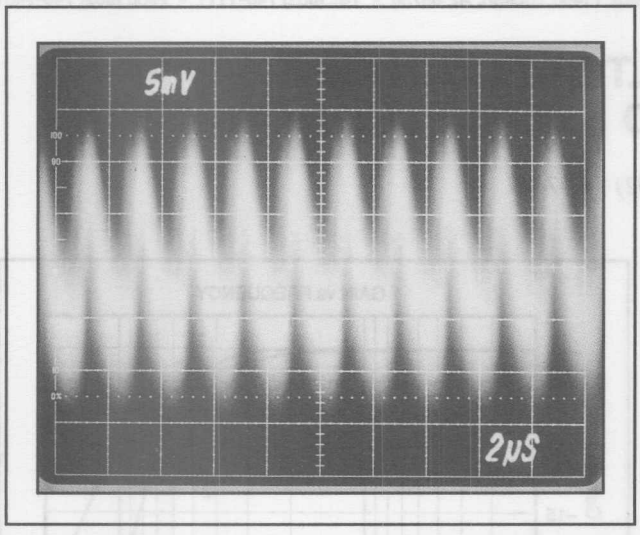


FIGURE 3. Standard ISO122 (approximately 20mVp-p output ripple).

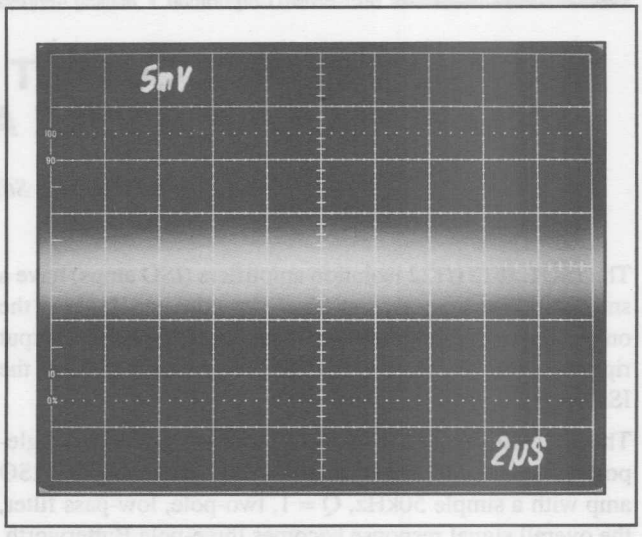


FIGURE 4. Filtered ISO122 (no visible output ripple).

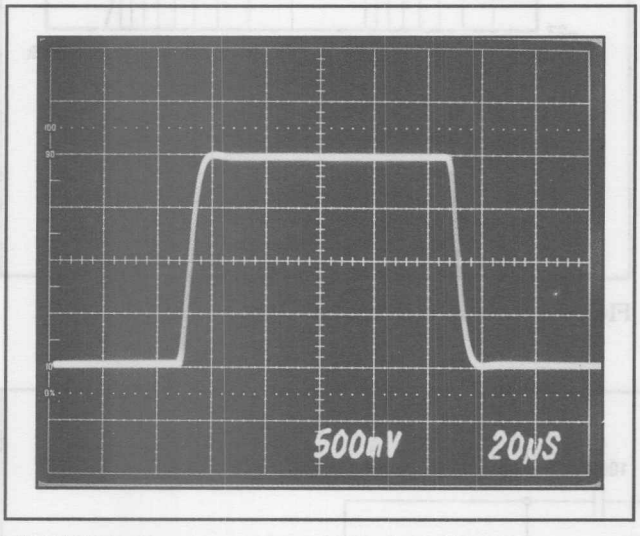


FIGURE 5. Step Response of Standard ISO122.

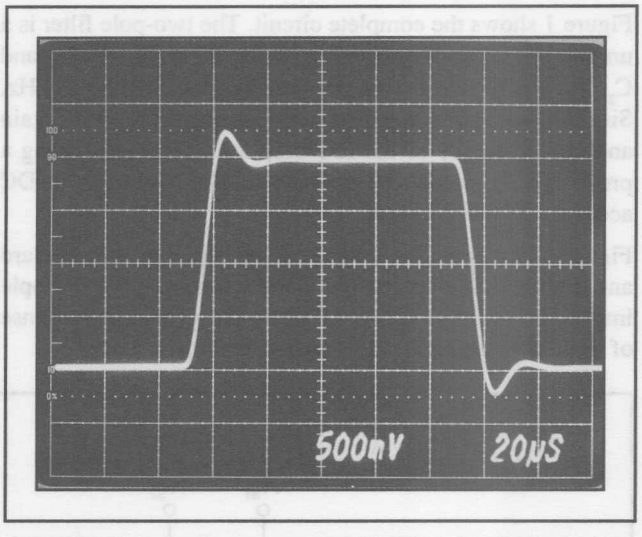
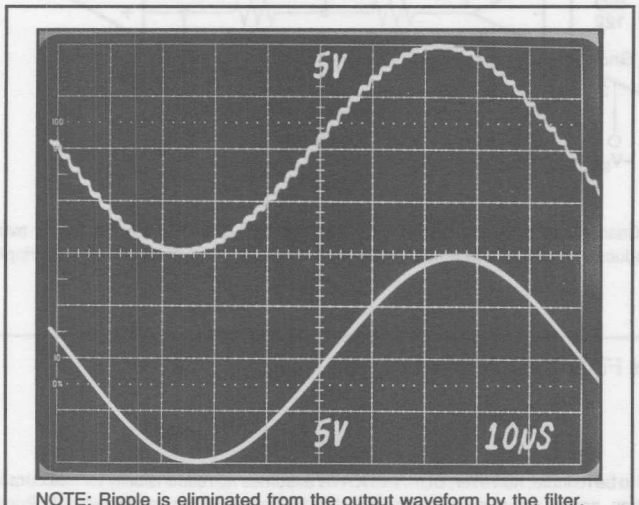


FIGURE 6. Step Response of ISO122 with Added Two-pole Output Filter.



NOTE: Ripple is eliminated from the output waveform by the filter.

FIGURE 7. Large-signal, 10kHz Sine-wave Response of ISO122 with and without Output Filter.

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VERY LOW COST ANALOG ISOLATION WITH POWER

By Mark Stitt (602) 746-7445

You can make a low-cost, precision analog isolation amplifier (ISO amp) with power by combining the ISO122 low-cost ISO amp with the HPR117 low-cost DC/DC converter. With isolated signal and isolated power in separate packages, complete application flexibility is assured.

The ISO122 features:

- Unity gain (±10V In to ±10V Out): ±0.05%
- 0.02% max nonlinearity
- 5mA quiescent current
- 140dB isolation mode rejection at 60Hz
- 1500Vrms continuous isolation rating (100% tested)

The HPR117 features:

- $V_{OUT} = V_{IN}$, ±5% (V_{IN} = 13.5V to 16.5V, I_{OUT} = 25mA)
- I_{OUT} = 25mA (750mW) continuous at 85°C
- 8mA quiescent current, no load
- 80% efficiency, full load
- Low output ripple
- 750VDC isolation rating

OUTPUT-SIDE POWERED ISO AMP

The most commonly used ISO amp configuration is shown in Figure 1. Both the ISO amp and the DC/DC converter are powered at the output side of the ISO amp. The HPR117 is connected to +15V and ground. The ISO122 is connected to ±15V and ground. The power-supply connections for the input side of the ISO amp are connected directly to the HPR117 output. No bypass capacitors are needed. The HPR117 has built-in 0.33µF bypass capacitors on both the input and outputs.

The isolated ±15V power output from the HPR117 can also be used for ancillary input-side circuitry such as input amplifiers and references. The ISO122 input section consumes about ±5mA. An additional ±20mA is available for other circuitry.

INPUT-SIDE POWERED ISO AMP

Some applications call for output-side isolation as shown in Figure 2. Isolated ±15V, 20mA auxiliary power is available on the output side for ancillary circuitry.

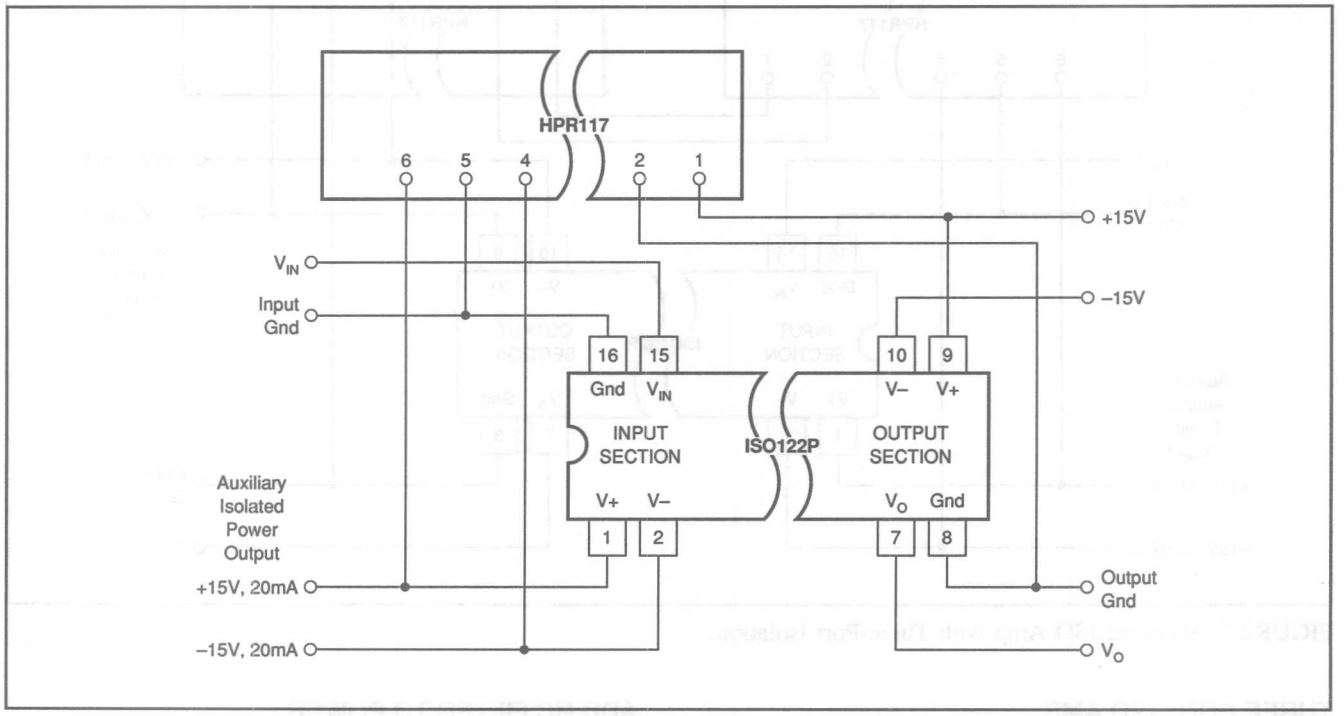

FIGURE 1. Output-Side Powered ISO Amp.

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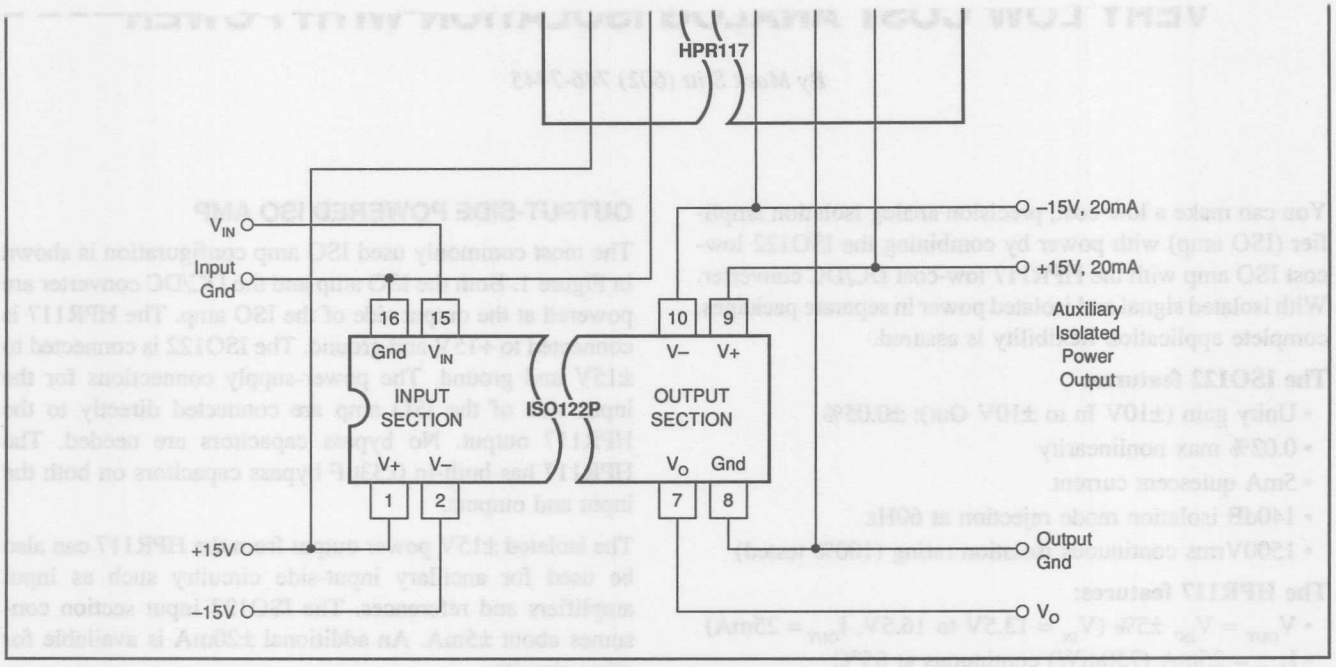

FIGURE 2. Input-Side Powered ISO Amp.

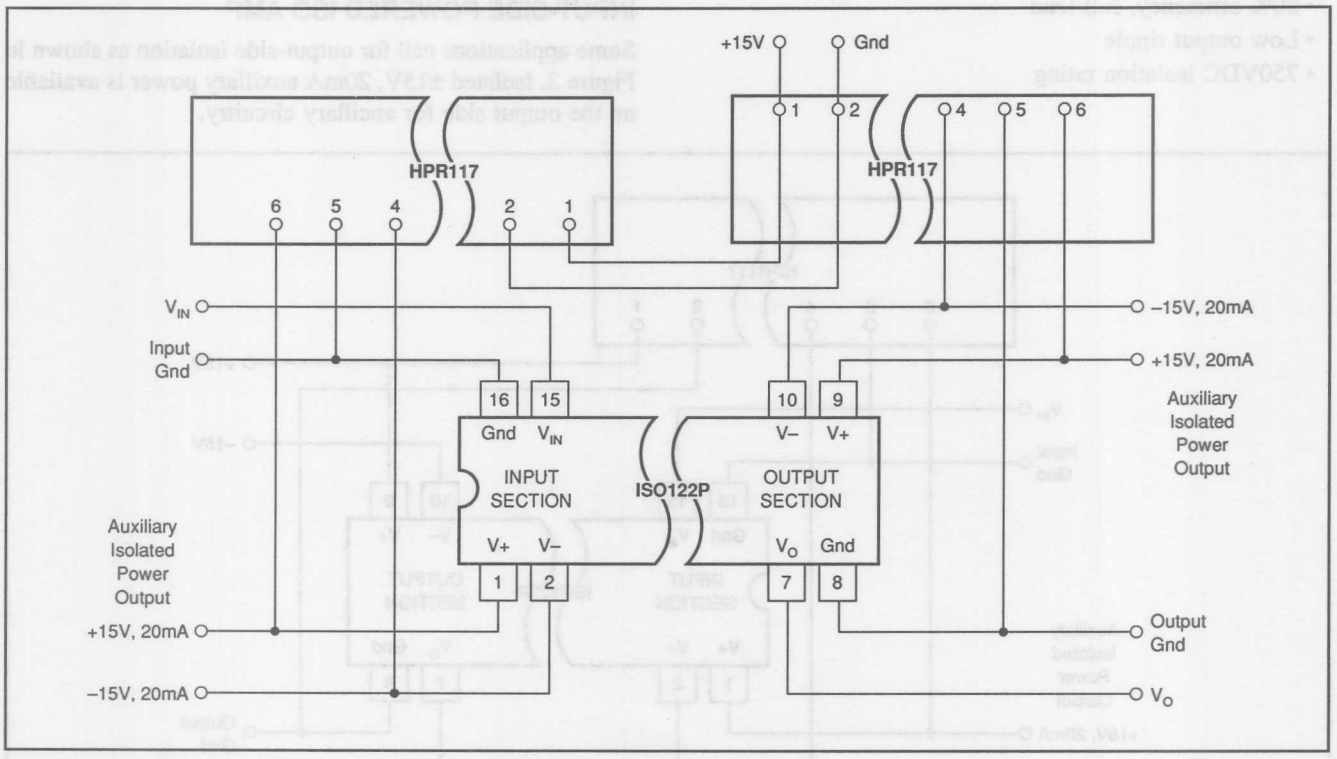

FIGURE 3. Powered ISO Amp with Three-Port Isolation.

THREE PORT ISO AMP

Some applications call for three-port isolation as shown in Figure 3. Both the input and output side of the ISO amp are isolated from the power-supply connection. Isolated ±15V, 20mA auxiliary power is available on both the input and output side of the ISO amp.

ADD RC FILTER TO POWER SUPPLY OUTPUT FOR LOW NOISE

Although performance is good using the ISO122 connected directly to the HPR117, best performance can be achieved with additional filtering. The output ripple of the HPR117 can interact with the ISO122 modulator/demodulator cir-

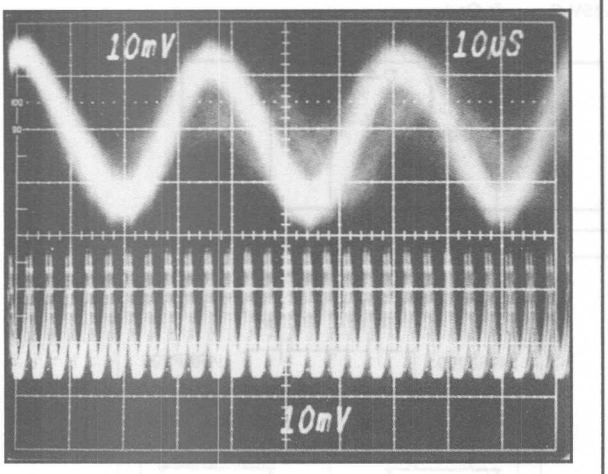

FIGURE 4. Oscilloscope Photograph Showing Typical HPR117 Power Supply Ripple (bottom trace) and Typical 30kHz, 30mVp-p Noise at the ISO122 Output Due to Aliasing of Power Supply Ripple.

cuitry through the power-supply pins resulting in an aliased noise signal within the signal bandwidth of the ISO amp. The 30kHz, 30mVp-p upper trace in Figure 4's scope photo is a typical example. The lower trace in the scope photo is the HPR117 output ripple with the ISO122 plus a 2kΩ load. Adding simple R, C filters in the outputs from the HPR117 as shown in Figure 5 eliminates the problem.

The R,C filter shown in Figure 5 can also be used with either the Figure 1 or Figure 2 circuit. Since the DC/DC converter can induce a substantial amount of ripple on input-side connections, filters may still be needed on both the input-side and output-side power supply connections of the ISO122 to prevent noise due to signal aliasing.

The filter resistors will degrade the load regulation of the DC/DC converters. In addition to the specified HPR117 load regulation, there will be an additional 50mV/mA drop through the 50Ω filter resistors. Although this results in only a 1.25V drop at the full-rated 25mA output, you may want to use smaller value resistors and commensurately larger value filter capacitors if power-supply sensitive ancillary circuitry is needed.

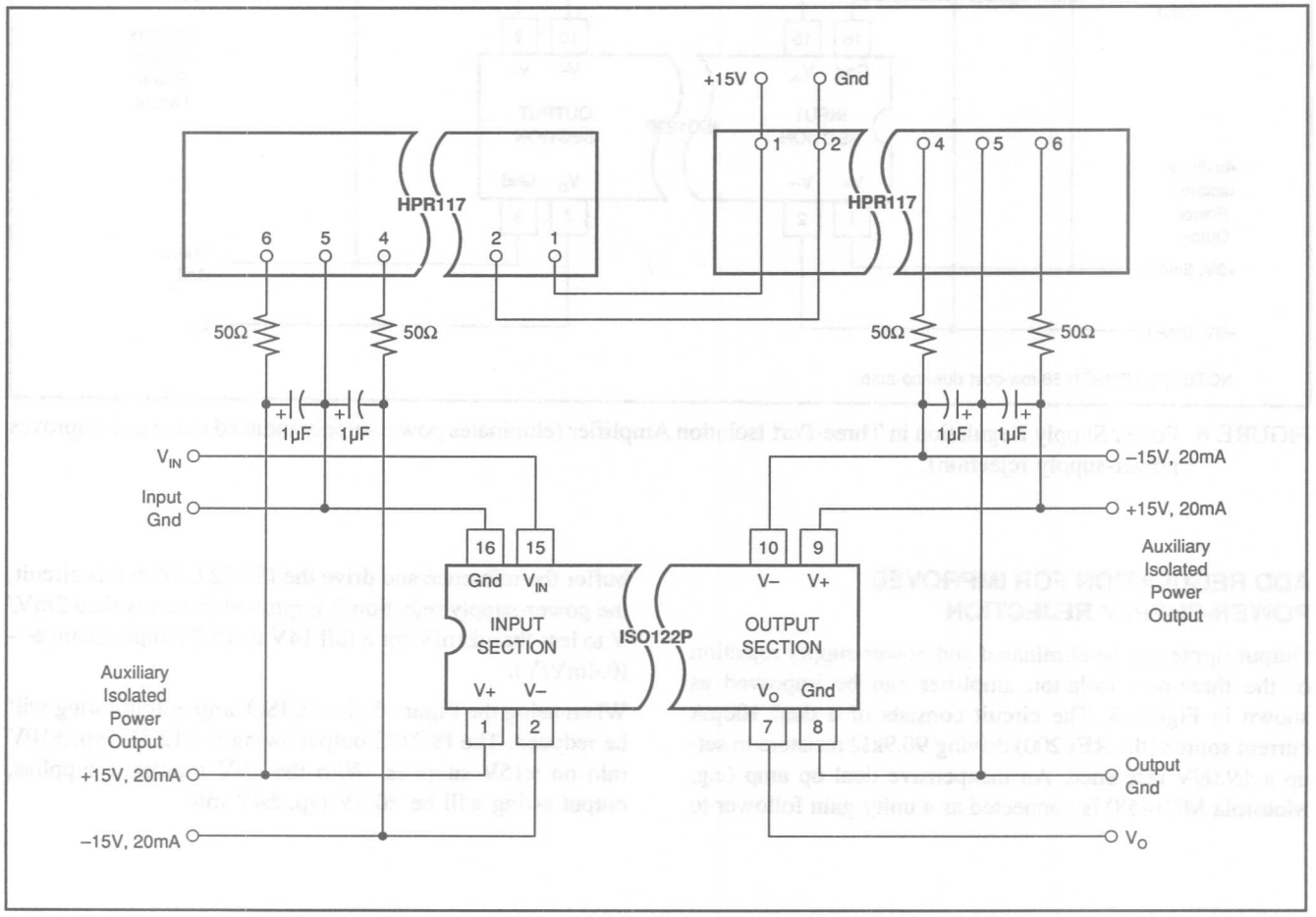

FIGURE 5. Three-Port Isolation Amplifier with R, C Power Supply Filters (eliminates power-supply induced noise).

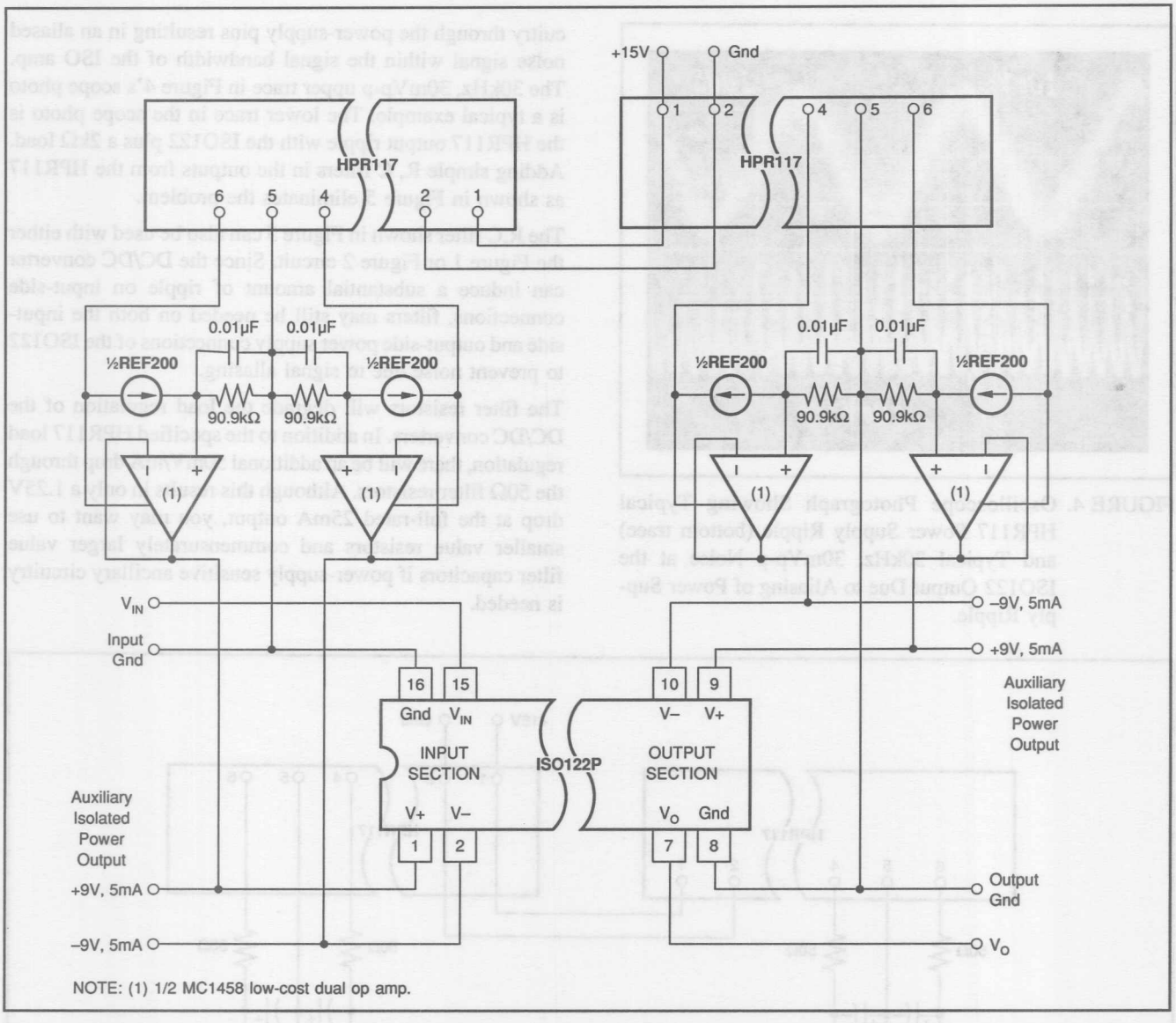

FIGURE 6. Power Supply Regulation in Three-Port Isolation Amplifier (eliminates power-supply induced noise and improves power-supply rejection).

ADD REGULATION FOR IMPROVED POWER-SUPPLY REJECTION

Output ripple can be eliminated and power-supply rejection of the three-port isolation amplifier can be improved as shown in Figure 6. The circuit consists of a dual 100µA current source (the REF200) driving 90.9kΩ resistors to set-up a ±9.09V reference. An inexpensive dual op amp (e.g. Motorola MC1458) is connected as a unity-gain follower to buffer the reference and drive the ISO122. With this circuit, the power-supply rejection is improved from a typical 2mV/V to less than ±1mV for a full 14V to 16.5V input change—(0.4mV/V).

When using the Figure 6 circuit, ISO amp output swing will be reduced. The ISO122 output swing is ±12.5V typ, ±10V min on ±15V supplies. With the ±9V regulated supplies, output swing will be ±6.5V typ, ±4V min.

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MAKE A PRECISION CURRENT SOURCE OR CURRENT SINK

By R. Mark Stitt (602) 746-7445

The introduction of the REF200 Dual Current Source has fostered a great deal of interest in current sources and current sinks. The AN-165 application guide, *Implementation and Application of Current Sources and Current Receivers*, was intended to answer customers' questions about design and applications of current sources/sinks and current to voltage converters of all kinds (not just the REF200).

A frequently asked question, not answered by the guide, has been: "How do I make the world's most accurate current source and current sink?" Figures 1 and 2 respectively show the circuits for making precision current sources and sinks.

The precision current source and sink are based on the new REF102 10.0V voltage reference. With 2.5ppm/°C V_{OUT} drift, and better than 5ppm/1000hrs long-term stability (see table on page 2), this buried-zener-based voltage reference offers the best performance available from a single-chip voltage reference today. The REF200 uses a band-gap type reference to allow low-voltage two-terminal operation. This makes it a good general-purpose part, but its drift and stability and initial accuracy cannot compare to that of the REF102.

The current source is shown in Figure 1. The voltage-follower connected op amp forces the voltage reference ground connection to be equal to the load voltage. The reference output then forces an accurate 10.0V across R_1 so that the current output is $10V/R_1$.

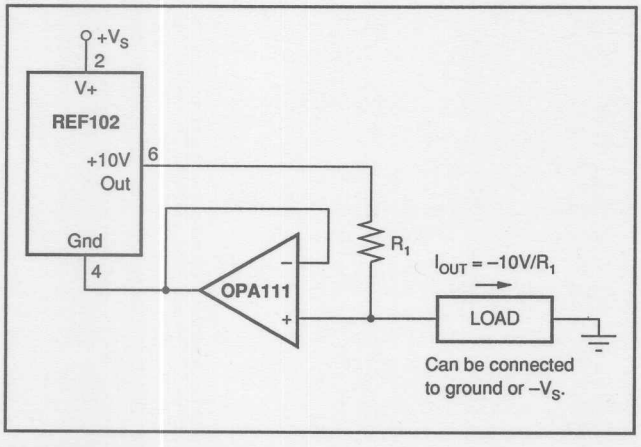

FIGURE 1. Precision Current Source.

The current sink is shown in Figure 2. The op amp drives both the voltage reference ground connection and the current-scaling resistor, R_1, so that the voltage reference output is equal to the load voltage. This forces –10.0V across R_1 so that the current sink output is $-10V/R_1$. The R_2, C_1 network provides local feedback around the op amp to assure loop stability. It also provides noise filtering. With the values shown, the reference noise is filtered by a single pole with $f_{-3dB} = 1/(2 \cdot \pi \cdot R_2 \cdot C_1) = 16kHz$.

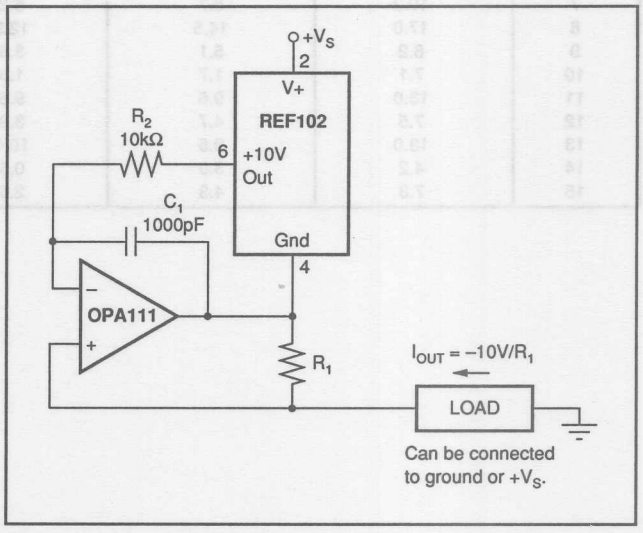

FIGURE 2. Precision Current Sink.

Compliance of the circuit depends on input and output range of the op amp used and the 11.4V minimum supply range of the REF102. The application guide goes into more detail.

Keep in mind that the accuracy of a voltage-reference-based current source depends on the absolute accuracy of the current scaling resistor (R_1). The absolute TCR and stability of the resistor directly affect the current source temperature drift and stability. If you use a 50ppm/°C resistor (common for 1% metal film resistors), the precision current source will have approximately 50ppm/°C drift with temperature—worse than the 25ppm/°C drift of a REF200.

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The performance of circuits using current source references depends only on the ratio accuracy of the scaling resistors. It is much easier to get good resistor ratio accuracy than to get good absolute accuracy, especially when using resistor networks.

Burr-Brown offers a wide variety of support components which are excellent choices for generation or conversion of current. Application Guide (AN-165) has proven valuable in selecting these components.

REF102CM +10.0V REFERENCE STABILITY vs TIME

T_A = 25°C, V_S = +15V.

UNIT	V_{OUT} CHANGE FROM 1 HR TO 168 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 1008 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 2016 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 3072 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 5136 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 14205 HRS [ppm]
1	6.8	5.5	7.1	4.7	8.2	11.7
2	5.1	1.0	1.2	–2.1	0.1	1.3
3	9.4	6.5	3.2	1.0	1.8	2.0
4	9.6	6.9	7.7	5.6	7.6	10.3
5	12.9	7.8	9.6	6.7	9.5	12.8
6	10.5	6.4	5.3	3.0	5.4	9.4
7	10.3	5.7	6.2	3.7	5.8	8.2
8	17.0	14.5	12.9	9.2	9.9	13.7
9	6.2	5.1	3.8	1.7	2.7	4.1
10	7.1	1.7	1.3	0.1	1.0	2.4
11	13.0	9.6	9.6	10.0	13.0	16.5
12	7.5	4.7	3.9	4.2	5.0	7.4
13	13.0	9.5	10.4	8.2	9.9	13.7
14	4.2	3.0	0.5	–0.3	4.2	2.8
15	7.3	4.3	2.6	1.8	4.1	3.9

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VOLTAGE-REFERENCE FILTERS

By R. Mark Stitt (602) 746-7445

IMPROVED VOLTAGE-REFERENCE FILTER HAS SEVERAL ADVANTAGES

- LOW OUTPUT IMPEDANCE AT HIGH FREQUENCY FOR DRIVING DYNAMIC LOADS SUCH AS HIGH-SPEED A/D CONVERTERS
- IMPROVED NOISE FILTERING
- BETTER ACCURACY BY ELIMINATING CAPACITOR LEAKAGE ERRORS
- DRIVES LARGE CAPACITIVE LOADS

The Burr-Brown REF102 is a buried-zener-based precision 10.0V reference. It has better stability and about five times lower output noise than band-gap-based voltage references such as the PMI REF-10. Still, its output noise is about 600µVp-p at a noise bandwidth of 1MHz (the output noise of the PMI REF-10 is about 3,000µVp-p at 1MHz).

So far as we know, the stability with time of the REF102 is significantly better than any other single-chip voltage reference on the market. We plan more characterization of stability vs time, but it will probably not be available this year. The following preliminary data is all we have for now. The devices used were off-the-shelf. They were not burned-in, or otherwise stabilized prior to this stability test.

Noise of a voltage reference can be reduced by filtering its output. Broadband noise can be reduced by the square-root of the reduction in noise bandwidth. Filtering the output of the reference to reduce the noise bandwidth by 100/1 (from 1MHz to 10kHz, for example) can reduce the noise by 10/1 (from 600µVp-p to 60µVp-p).

The conventional circuit, shown in Figure 1, uses a single-pole RC filter and a buffer amplifier. One problem with this circuit is that leakage current through the filter capacitor, C_1, flows through R_1 resulting in DC error. Furthermore, changes in leakage with temperature result in drift. The relatively low RC time constants often needed dictate large capacitor values prone to this problem.

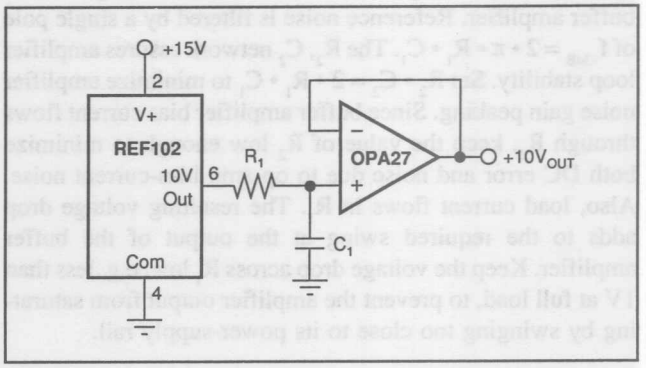

FIGURE 1. Voltage Reference with Conventional Filter.

REF102CM +10.0V REFERENCE STABILITY vs TIME

T_A = 25°C, V_S = +15V.

UNIT	V_{OUT} CHANGE FROM 1 HR TO 168 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 1008 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 2016 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 3072 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 5136 HRS [ppm]	V_{OUT} CHANGE FROM 1 HR TO 14205 HRS [ppm]
1	6.8	5.5	7.1	4.7	8.2	11.7
2	5.1	1.0	1.2	–2.1	0.1	1.3
3	9.4	6.5	3.2	1.0	1.8	2.0
4	9.6	6.9	7.7	5.6	7.6	10.3
5	12.9	7.8	9.6	6.7	9.5	12.8
6	10.5	6.4	5.3	3.0	5.4	9.4
7	10.3	5.7	6.2	3.7	5.8	8.2
8	17.0	14.5	12.9	9.2	9.9	13.7
9	6.2	5.1	3.8	1.7	2.7	4.1
10	7.1	1.7	1.3	0.1	1.0	2.4
11	13.0	9.6	9.6	10.0	13.0	16.5
12	7.5	4.7	3.9	4.2	5.0	7.4
13	13.0	9.5	10.4	8.2	9.9	13.7
14	4.2	3.0	0.5	–0.3	4.2	2.8
15	7.3	4.3	2.6	1.8	4.1	3.9

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noise of the buffer amplifier. The noise of the buffer amplifier acts at the buffer's full unity-gain bandwidth adding to the output noise of the circuit. Even if the noise at the output of the RC filter is zero, the noise added by the buffer can be intolerable in many applications. The improved filter, shown in Figure 2, solves both problems.

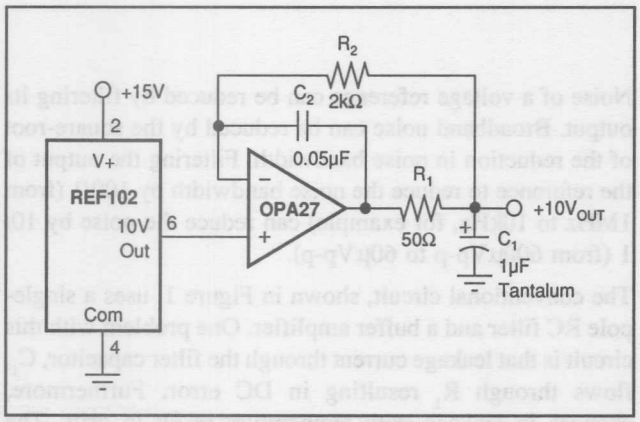

FIGURE 2. Voltage Reference with Improved Filter.

The improved filter places the RC filter at the output of the buffer amplifier. Reference noise is filtered by a single pole of $f_{-3dB} = 2 \cdot \pi \cdot R_1 \cdot C_1$. The R_2, C_2 network assures amplifier loop stability. Set $R_2 \cdot C_2 = 2 \cdot R_1 \cdot C_1$ to minimize amplifier noise gain peaking. Since buffer amplifier bias current flows through R_2, keep the value of R_2 low enough to minimize both DC error and noise due to op amp bias-current noise. Also, load current flows in R_1. The resulting voltage drop adds to the required swing at the output of the buffer amplifier. Keep the voltage drop across R_1 low, e.g. less than 1V at full load, to prevent the amplifier output from saturating by swinging too close to its power-supply rail.

both the voltage reference and the buffer is filtered. Since the filter is in the feedback loop of the buffer amplifier, C_1 leakage current errors reacting with R_1 are divided down to an insignificant level by the loop gain of the buffer amp. The feedback also keeps the DC output impedance of the improved filter near zero. Also, leakage through C_2 is negligible since the voltage across it is nearly zero.

At high frequency, the output impedance of the improved filter is low due to C_1. The reactance of a 1µF capacitor is 0.16Ω at 1MHz. For an A/D converter reference, connect C_1 as close to the reference input pin as possible.

The improved filter can drive large capacitive loads without stability problems. Just keep $(C_{LOAD} + C_1) \cdot R_1 < 0.5 \cdot R_2 \cdot C_2$.

There is one caution with the improved filter. Although the output impedance is low at both high frequencies and DC, it peaks at midband frequencies. Reduced loop gain due to the R_2, C_2 network is responsible. A peak output impedance of about $0.7 \cdot R_1$ occurs near the filter pole frequency. If lower midband output impedance is required, R_1 must be reduced and C_1 increased accordingly.

MAKE A PRECISION –10V REFERENCE

By R. Mark Stitt (602) 746-7445

The need for a precision –10.0V reference arises often. For example, the best way to get a 0V to +10V output from a CMOS MDAC is to use a –10V reference (see Figures 4-6). ADI/PMI has the REF-08 –10V reference, but it has limited performance. Although Burr-Brown offers no –10V reference, the REF102 precision +10.0V reference can be accurately converted to a precision –10.0V reference. The circuit is simple and requires no precision components. The 2.5ppm/°C temperature drift of the Burr-Brown REF102 is twenty times better than the 50ppm/°C best grade of the PMI REF-08. (Even our lowest grade is five times better.)

The simplest approach for converting a REF102 into a –10.0V reference is shown in Figure 1. The only extra component is a 1kΩ resistor connected to $-V_S$. This circuit is useful, but has limitations. Maximum expected load current plus maximum reference quiescent current must be supplied by the resistor at minimum $-V_S$. Changes in current resulting from load and power supply variations must be driven by the reference. The excess current through the reference reduces its accuracy due to drift from self-heating and thermal feedback. Changes in reference output current due to power-supply variations translate into line regulation error. Voltage reference load regulation is not usually as good as line regulation. Finally, the output impedance due to the resistor pull-down causes settling problems with dynamic loads.

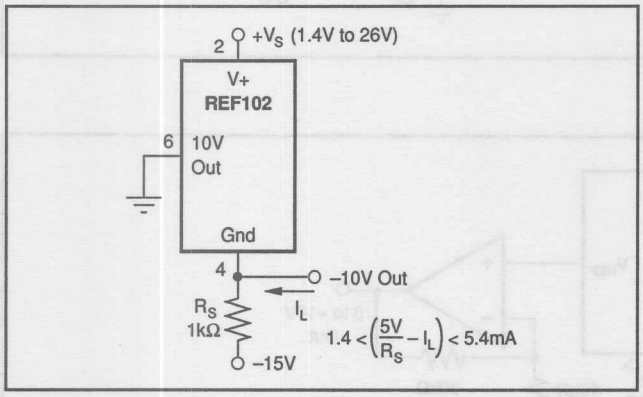

FIGURE 1. Simple –10V Reference.

The circuit shown in Figure 2 solves these problems. As in Figure 1, no precision resistors are needed. The error contributed by the op amp is negligible (the OPA27 0.6µV/°C V_{OS}/dT adds only 0.06 ppm/°C drift to the –10V reference). As a bonus, the circuit incorporates noise filtering.

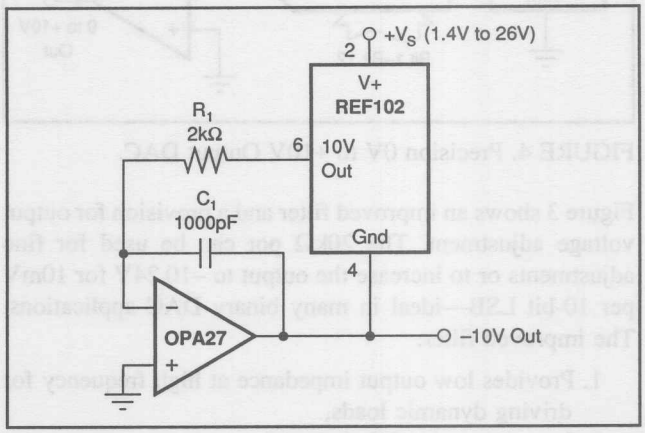

FIGURE 2. Improved –10V Reference.

To understand how the circuit works, notice that the reference is in the feedback loop of the op amp. The op amp output forces the Gnd connection of the reference to exactly –10.0V so that the voltage at the op amp inverting input is the same as at its noninverting input (ground). Since no current flows into the op amp input, the reference output current remains at zero, eliminating voltage reference thermal feedback or load regulation errors. The R_1, C_1 network assures loop stability and provides noise filtering. Reference noise is filtered by a single pole of $f_{-3dB} = 1/(2 \cdot \pi \cdot R_1 \cdot C_1)$. Bias current flowing through R_1 can produce DC errors and noise. If a lower filter pole is needed, keep R_1 = 2kΩ and increase C_1 to preserve accuracy.

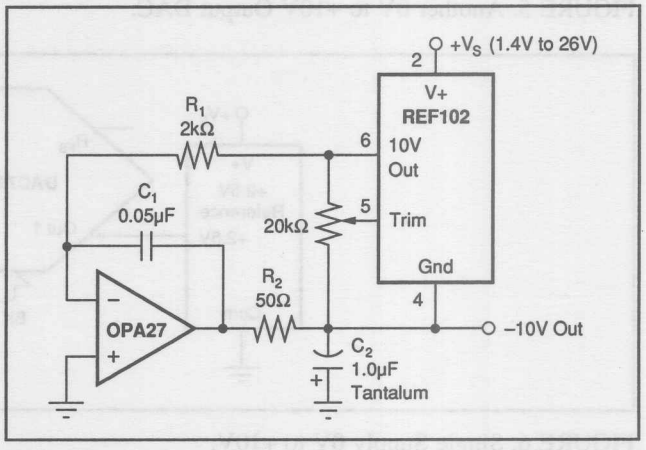

FIGURE 3. Improved –10V Reference with Improved Filter, with V_{OUT} Trim.

5

Application Bulletin Number 4

Printed in U.S.A. June, 1991

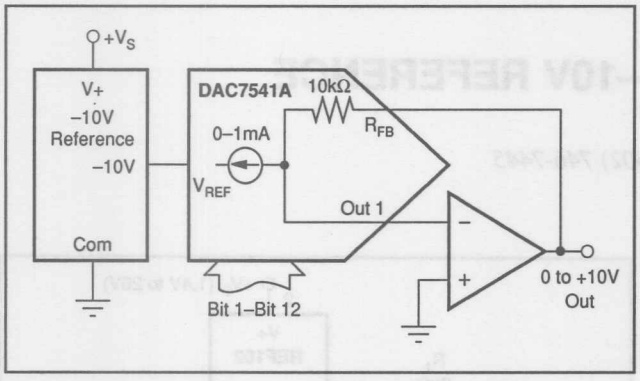

FIGURE 4. Precision 0V to +10V Output DAC.

Figure 3 shows an improved filter and a provision for output voltage adjustment. The 20kΩ pot can be used for fine adjustments or to increase the output to –10.24V for 10mV per 10-bit LSB—ideal in many binary DAC applications. The improved filter:

1. Provides low output impedance at high frequency for driving dynamic loads,
2. Improves noise filtering, and
3. Drives large capacitive loads—see AB-003.

Figure 4 shows the preferred way to connect a CMOS MDAC for a 0 to +10V output. This approach is less expensive and provides better accuracy than the other approaches shown below.

The circuit shown in Figure 5 is commonly used to get a 0 to +10V output with a CMOS MDAC. The disadvantage with this circuit is that it requires an extra op amp and pair of precision resistors for each DAC. Also, settling time increases because two amplifiers must settle in the signal path. For good settling time, both amplifiers must be fast settling. Then settling time increases by the square-root-of-the-sum-of-the-squares of settling time for each amplifier.

The circuit shown in Figure 6 can also be used to get a 0 to +10V output from a CMOS MDAC. The problem with this circuit is nonlinearity due to code-dependent voltage across the switches within the DAC. Using a 2.5V reference and gain at the output, as shown, mitigates this error, but you still need a pair of precision resistors for each DAC. The appropriate use for this circuit is in +5V single-supply applications. With a 2.5V reference and a unity-gain, single-supply buffer, the output will be 0 to +2.5V.

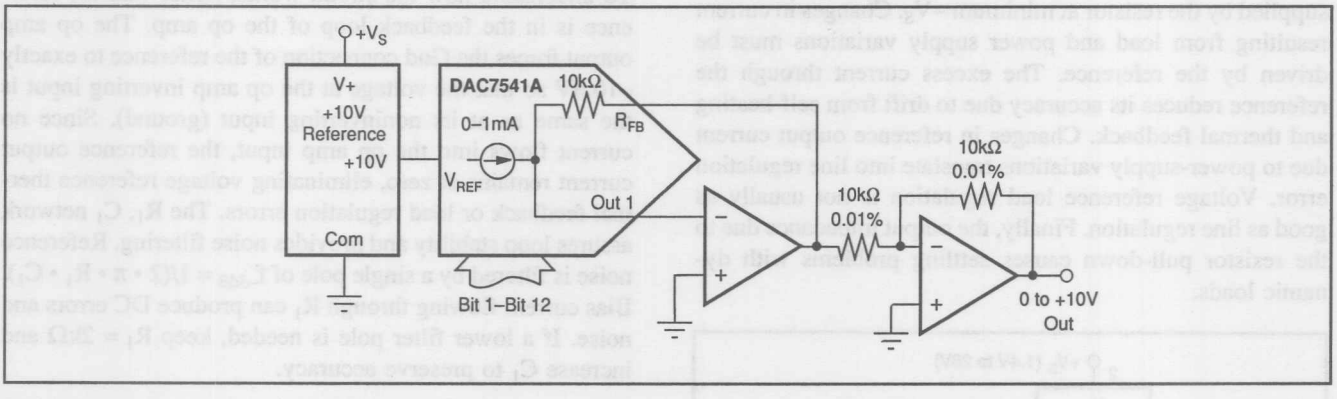

FIGURE 5. Another 0V to +10V Output DAC.

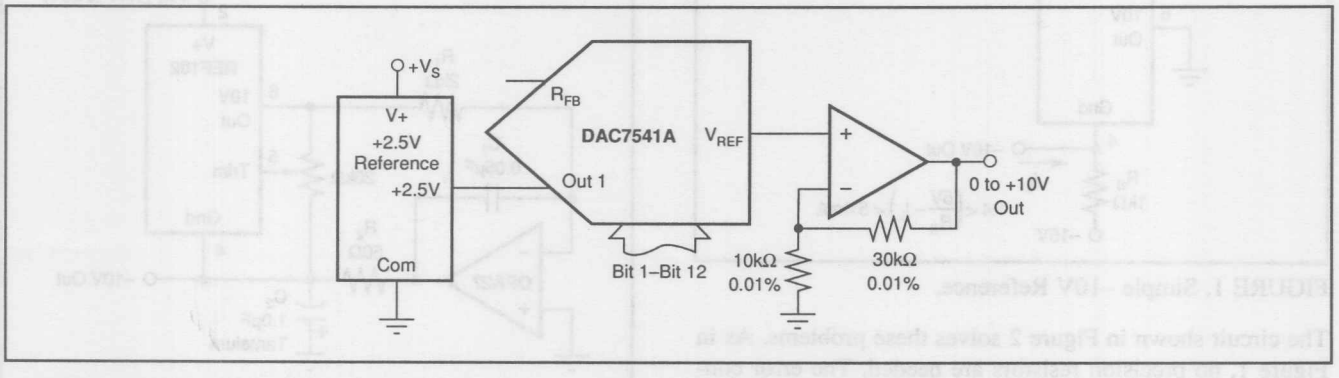

FIGURE 6. Single Supply 0V to +10V.

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Make A Precision ±10V Reference

By R. Mark Stitt, (602) 746-7445

Many systems require the combination of both a positive and a negative precision 10.0V reference. ADI offers several hybrid ±10V references. Although Burr-Brown offers no ±10V reference at this time, we do have some simple two-chip solutions which are accurate and can be more cost effective. (The *lowest* cost grades of ADI's ±10V references are priced at $37.25 (AD2702) and $42.10 (AD2712) each in 25+ quantities.)

Figure 1 shows one two-chip solution. It uses the super-stable REF102 +10.0V precision reference and an INA105 difference amplifier connected as a precision unity gain inverting amplifier. The REF102CM has 2.5ppm/°C max drift. The INA105BM adds drift to the –10.0V output of 1ppm/°C max due to V_{OS}/dT and 5ppm/°C due to gain drift. The V_{OUT} error of the REF102CM is ±2.5mV max. The INA105BM adds ±10mV max error to the –10.0V reference.

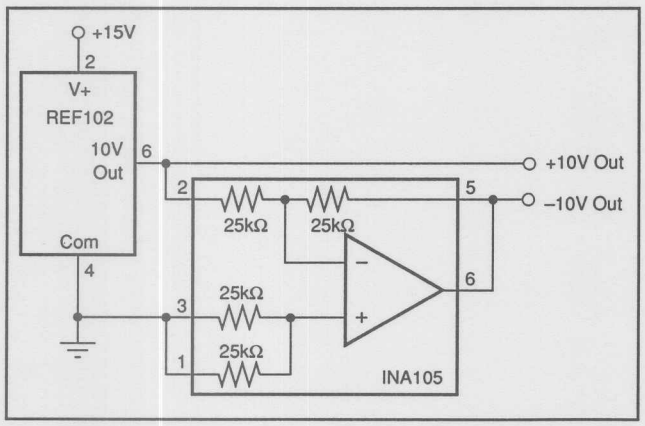

FIGURE 1. Precision Two-Chip ±10.0V Reference.

Both of the V_{OUT} errors are adjustable to zero as shown in Figure 2. Because the adjustment range is small, instability in the trim components is negligible. Since the $+V_{OUT}$ adjustment affects $-V_{OUT}$, adjust $+V_{OUT}$ first.

If you need a 1ppm/°C reference, use the REF101 as shown in Figure 3. The REF101 contains the precision resistors needed for the –10V inverter. For a ±10.0V reference, the only additional component needed is an op amp. The 0.6µV/°C V_{OS}/dT of the OPA27AM adds a negligible 0.06ppm/°C drift to the negative reference.

For lowest parts cost, consider the ±10V reference shown in Figure 4. The unity-gain-inverting amplifier in this circuit uses 1% resistors and a 100Ω pot to trim the –10.0V reference output. When using standard 1% film resistors, a $-V_{OUT}$ drift of 50ppm/°C or more should be expected.

The REF101 and REF102 are buried-zener-based references. They have better stability and much lower noise than standard band-gap-based voltage references. Still, there are instances when even lower noise is required. The standard way to lower noise is to lower the noise bandwidth at the output of the reference by filtering (see Application Bulletin 3).

The circuit shown in Figure 5 includes noise reduction filters on both the +10V and –10V reference outputs. The improved filter design shown has several advantages:

1) low output impedance at high frequency for driving dynamic loads,
2) improved noise filtering, and
3) ability to drive large capacitive loads.

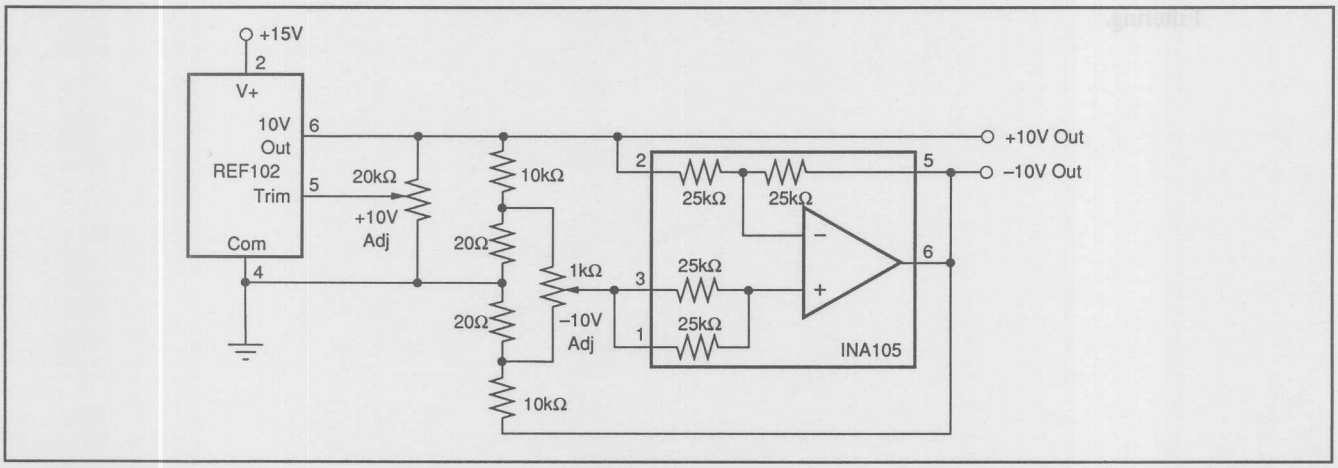

FIGURE 2. Precision Two-Chip ±10V Reference with $\pm V_{OUT}$ Trim.

Printed in U.S.A. March, 1990

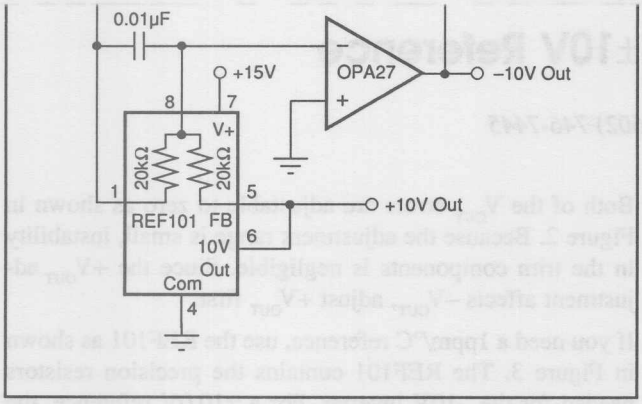

FIGURE 3. Precision 1ppm/°C ±10V Reference.

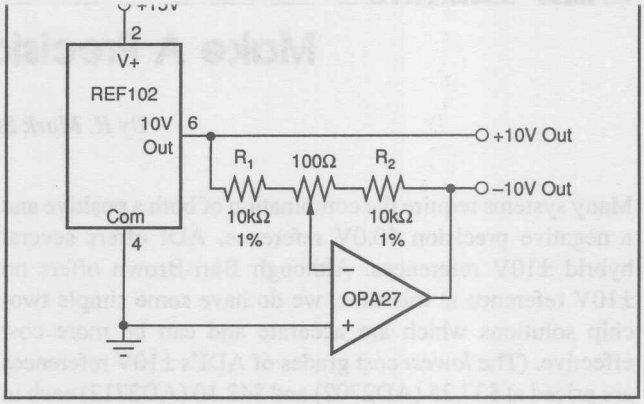

FIGURE 4. ±10V Reference Using 1% Resistors.

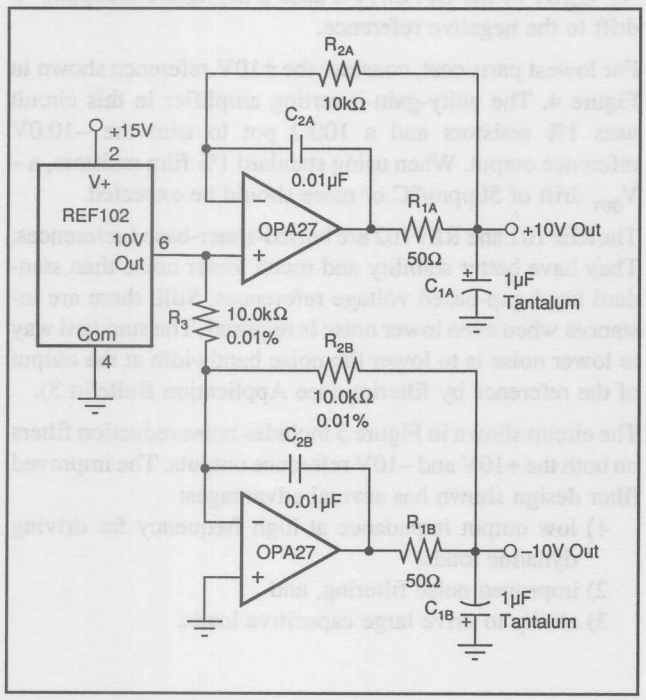

FIGURE 5. Precision ±10.0V Reference with Output Filtering.

Make a –10V to +10V Adjustable Precision Voltage Source

By R. Mark Stitt, (602) 746-7445

Many situations require a precision voltage source which can be adjusted through zero to both positive and negative output voltages. An example is a bipolar power supply. Have you ever adjusted your unipolar lab supply down to 0V, then swapped the output leads and adjusted it back up to get a negative voltage output? What happened to your circuit when the input from the low impedance source went open circuit? Were you able to actually adjust the output to 0V, or did a small voltage offset limit the range? This precision bipolar voltage source can solve these problems.

Perhaps the most obvious implementation of a bipolar voltage source would be to use a bipolar voltage reference. However, a simpler solution is to use a single voltage reference and a precision unity-gain inverting amplifier. If you use a precision difference amplifier for the unity-gain inverting amplifier, the circuit requires just two chips and a potentiometer.

To understand how the circuit works, first consider the –1.0V/V to +1.0V/V linear gain control amplifier shown in Figure 1. An INA105 difference amplifier is used in a unity-gain inverting amplifier configuration. A potentiometer is connected between the input and ground. The slider of the pot is connected to the noninverting input of the unity-gain inverting amplifier. (The noninverting input of a unity-gain inverting amplifier would normally be connected to ground.) With the slider at the bottom of the pot, the circuit is a normal precision unity-gain inverting amplifier with a gain of –1.0V/V ±0.01% max. With the slider at the top of the pot, the circuit is a normal precision voltage follower with a gain of +1.0V/V ±0.001% max. With the slider in the center, there is equal positive and negative gain for a net gain of 0V/V. The accuracy between –1.0V/V and +1.0V/V will normally be limited by the accuracy of the pot. Precision 10-turn pots are available with 0.01% linearity.

The –1.0V/V to +1.0V/V linear gain control amplifier has many applications. With the addition of a precision +10.0V reference as shown in Figure 2, it becomes a –10V to +10V adjustable precision voltage source.

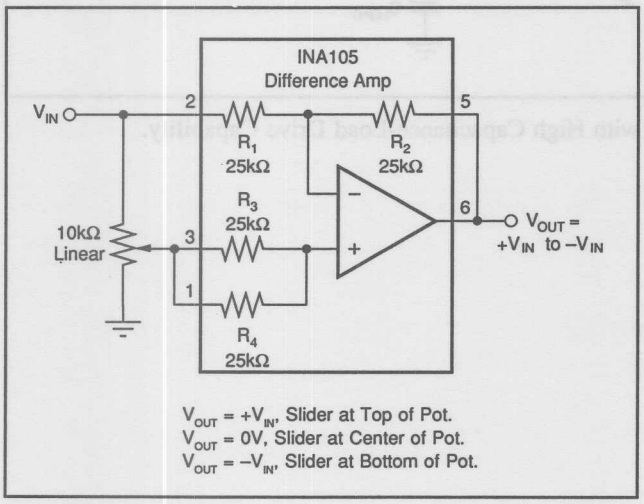

FIGURE 1. –1.0V/V to +1.0V/V Linear Gain Control Amplifier.

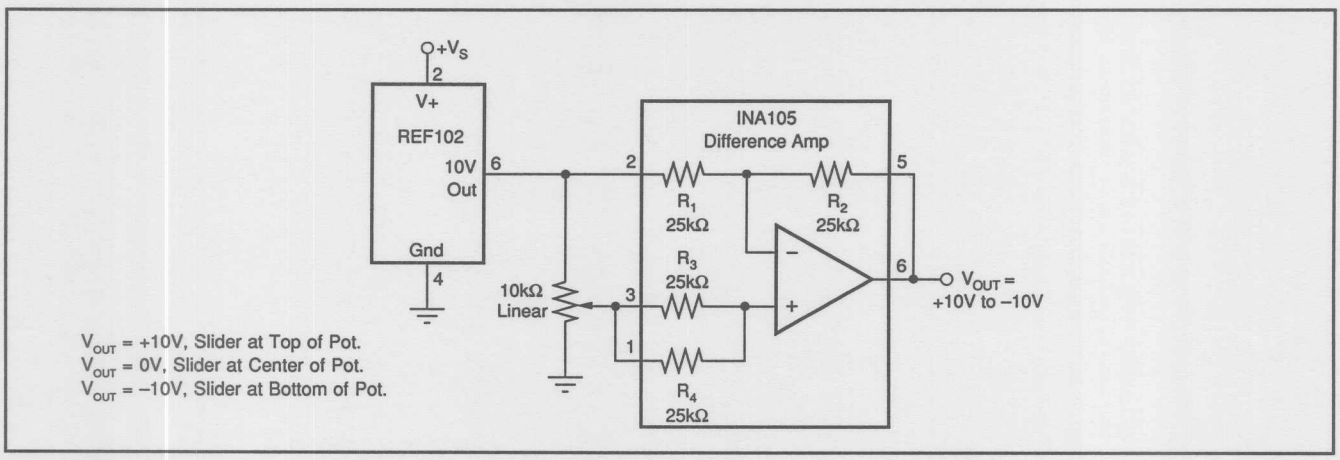

FIGURE 2. –10V to +10V Adjustable Precision Voltage Source.

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In many instances adjustable voltage sources need the ability to drive high-capacitance loads such as power-supply bypass capacitors. The additional circuitry needed to drive high capacitance is shown in Figure 3. For stability, keep $C_{LOAD} \cdot R_3 < 0.5 \cdot R_2 \cdot C_2$. Since access to the op amp inverting input is needed, the unity-gain inverting amplifier is made with an op amp and discrete resistors. For precision, R_1 and R_2 must be accurately matched. Also, load current flows in R_3. The resulting voltage drop adds to the required swing at the output of the op amp. Keep the voltage drop across R_3 low —less than 1V at full load—to prevent the amplifier output from swinging too close to its power-supply rail.

For applications with substantial volume (e.g. 5k ea/year) a version of the INA105 with the op amp inverting input brought out is available as a special (2A660). Inquire with marketing about price and delivery.

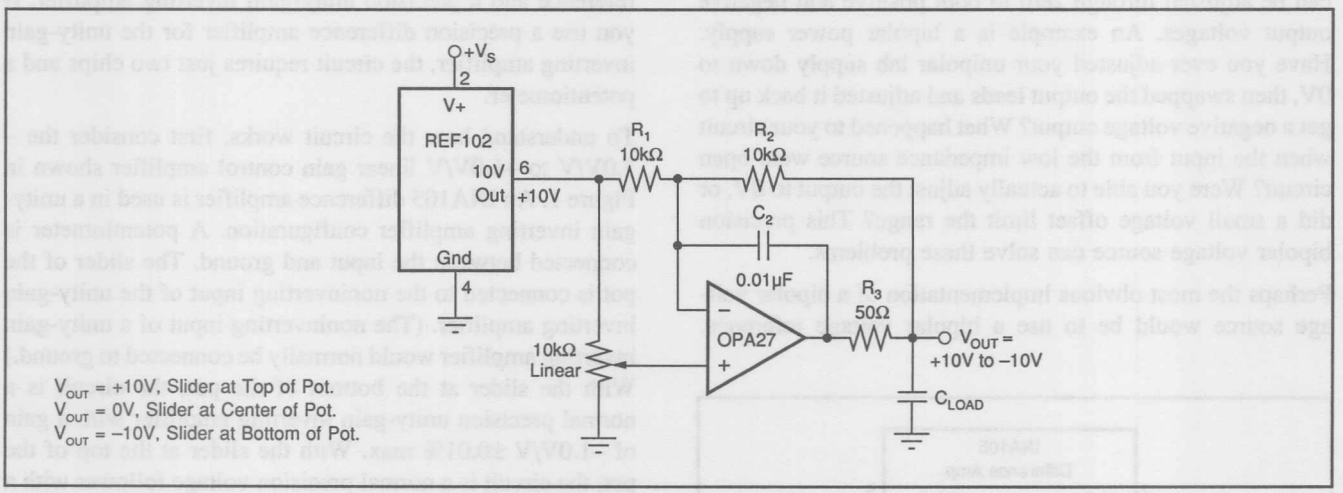

FIGURE 3. –10V to +10V Adjustable Precision Voltage Source with High Capacitance-Load Drive Capability.

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LOW POWER SUPPLY VOLTAGE OPERATION OF REF102 10.0V PRECISION VOLTAGE REFERENCE

By R. Mark Stitt (602) 746-7445

Two of the most important specifications for a voltage reference are noise and stability with time. The zener-based REF102 10.0V voltage reference has much better noise and stability than band-gap-based references.

An advantage that band-gap-based references have in some applications is the ability to operate from lower voltage power supplies. This is because the basic band gap voltage is approximately 1.2V as compared to 6V to 8V for a zener diode. As a 10.0V reference, the REF102 requires a minimum 11.4V V_S. If the higher performance of a REF102 is required, there are several options for operation on lower supply voltages.

If a negative supply is available, it may be possible to operate the REF102 on a positive supply as low as 4.5V. Another option is to use one of the simple DC/DC converter circuits shown to operate the REF102 from a single +5V power supply.

The simplest option for reduced supply operation of a REF102 is to add a unity-gain inverter to make a ±5.0V reference as shown in Figure 1. This allows the REF102 to be used on ±9V power supplies, for example. The minimum voltage for V+ is actually 6.4V (the output of the REF102 can operate within 1.4V of its positive supply).

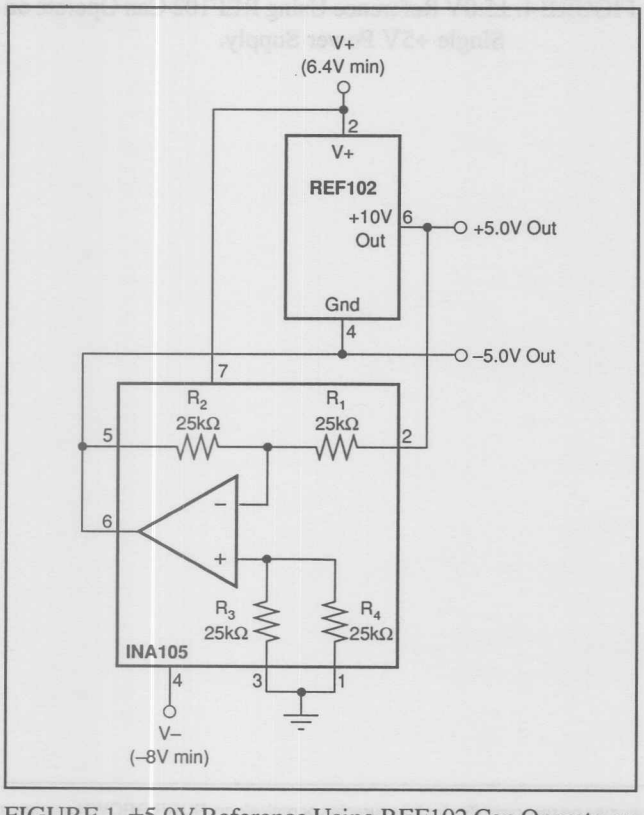

FIGURE 1. ±5.0V Reference Using REF102 Can Operate on $+V_S$ = +6.4V, $-V_S$ = –8V.

The minimum negative supply depends on the amplifier used for the unity-gain inverter. With an INA105 difference amp used for the unity-gain inverter, the negative power supply must be at least –8V.

To operate the REF102 on a minimum $+V_S$ of 4.5V, use an INA106 gain-of-10 difference amplifier for the inverter as shown in Figure 2. With the INA106, the reference outputs are +1.0V and –9.0V. The 4.5V minimum $+V_S$ rating is due to the output swing limit of the INA106. The negative supply must be at least –12V.

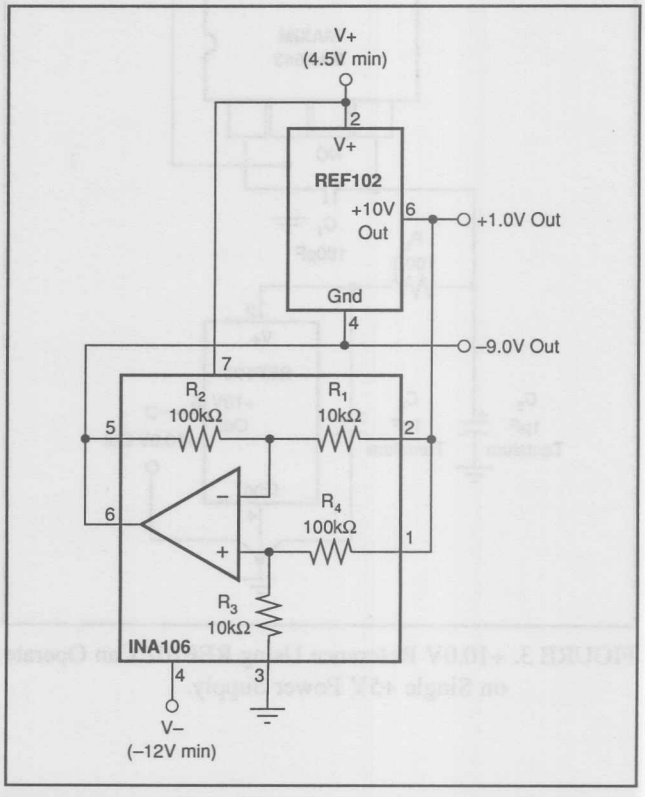

FIGURE 2. +1.0V, –9.0V Reference Using REF102 Can Operate on $+V_S$ = +4.5V, $-V_S$ = –12V.

Printed in U.S.A. June, 1990

When only a single +5V power supply is available, the REF102 can be operated by boosting the 5V supply with one of the many inexpensive DC/DC converter chips available.

A single 5V supply can be boosted to a regulated 15V with a flyback converter as shown in Figure 3. The Maxim MAX643 is basically a self-contained DC/DC converter in an 8-pin plastic DIP. The only additional components needed to convert 5V to a regulated 15V are a single external inductor and a few bypass capacitors. R_6 and C_3 add additional ripple filtering. Good results were obtained with an inductor made from 16 turns of #16 wire on a TDK HC52 T5-10-2.5 core. See the Maxim data sheet for more information regarding the DC/DC converter.

Another option is to boost a single 5V supply to ±10V to drive a ±5.0V reference as shown in Figure 4. The Maxim MAX681 is a completely self-contained DC/DC converter using charge-pump techniques to convert 5V to ±10V.

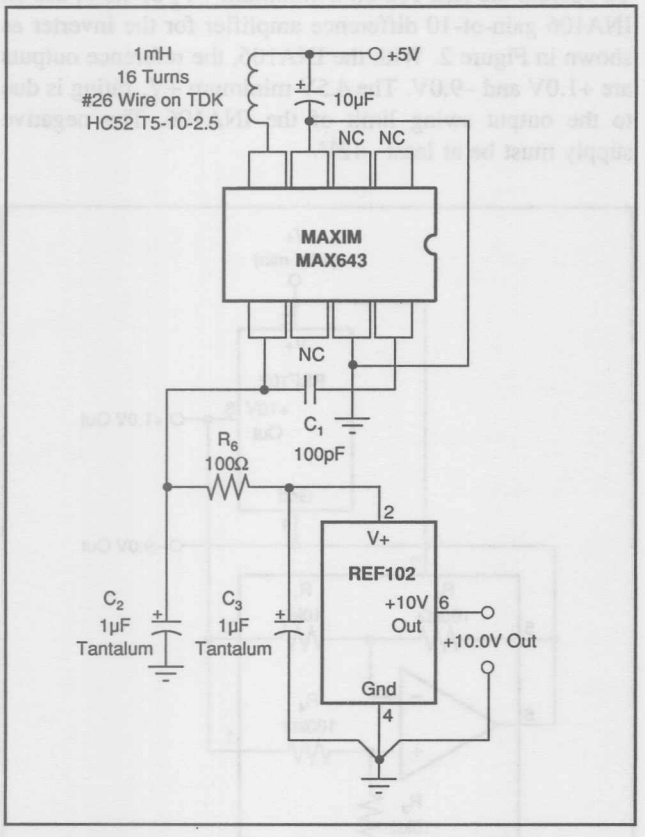

FIGURE 3. +10.0V Reference Using REF102 Can Operate on Single +5V Power Supply.

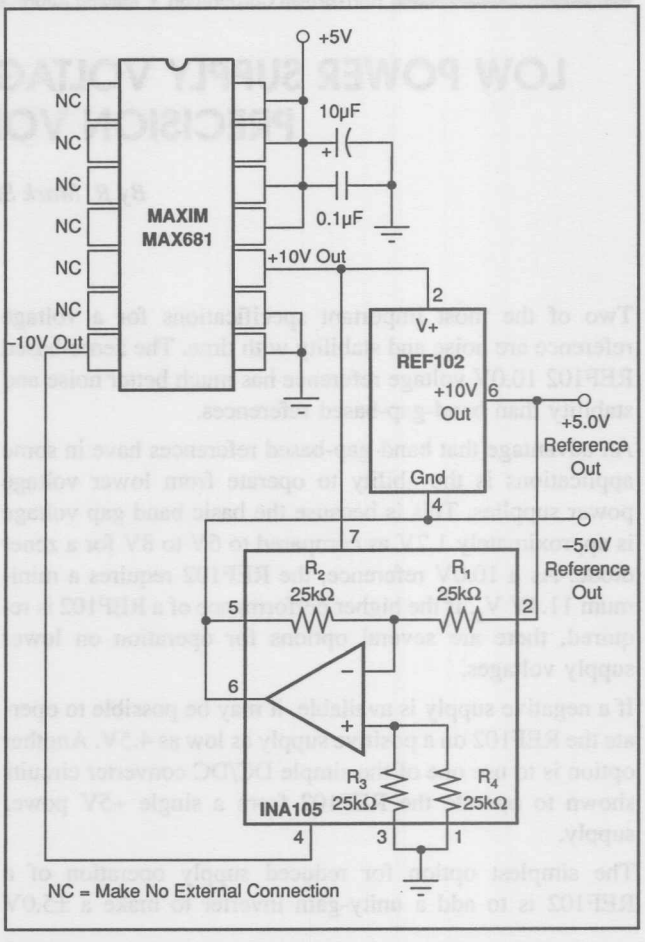

FIGURE 4. ±5.0V Reference Using REF102 Can Operate on Single +5V Power Supply.

By Bruce Trump and R. Mark Stitt (602) 746-7445

Although low-pass filters are vital in modern electronics, their design and verification can be tedious and time consuming. The Burr-Brown FilterPro™ program makes it easy to design unity-gain low-pass active filters. The program supports the most commonly used all-pole filters: Butterworth, Chebyshev, and Bessel.

Butterworth—maximally flat magnitude. This filter has the flattest possible pass-band magnitude response. Attenuation is –3dB at the design cutoff frequency. Attenuation above the cutoff frequency is a moderately steep –20dB/decade/pole. The pulse response of the Butterworth filter has moderate overshoot and ringing.

Chebyshev—equal ripple magnitude. (Sometimes translated Tschebyscheff or Tchevysheff). This filter response has steeper attenuation above the cutoff frequency than Butterworth. This advantage comes at the penalty of amplitude variation (ripple) in the pass-band. Unlike Butterworth and Bessel responses, which have 3dB attenuation at the cutoff frequency, Chebyshev cutoff frequency is defined as the frequency at which the response falls below the ripple band. For even-order filters, all ripple is above the 0dB DC response, so cutoff is at 0dB—see Figure 1a. For odd-order filters, all ripple is below the 0dB DC response, so cutoff is at –(ripple) dB—see Figure 1b. For a given number of poles, a steeper cutoff can be achieved by allowing more pass-band ripple. The Chebyshev has even more ringing in its pulse response than the Butterworth.

Bessel—maximally flat delay, (also called Thomson). Due to its linear phase response, this filter has excellent pulse response (minimal overshoot and ringing). For a given number of poles, its magnitude response is not as flat, nor is its attenuation beyond the –3dB cutoff frequency as steep as the Butterworth. It takes a higher-order Bessel filter to give a magnitude response similar to a given Butterworth filter, but the pulse response fidelity of the Bessel filter may make the added complexity worthwhile.

SUMMARY

Butterworth

Advantages—Maximally flat magnitude response in the pass-band.

Disadvantages—Overshoot and ringing in step response.

Chebyshev

Advantages—Better attenuation beyond the pass-band than Butterworth.

Disadvantages—Ripple in pass-band. Even more ringing in step response than Butterworth.

Bessel

Advantages—Excellent step response.

Disadvantages—Even poorer attenuation beyond the pass-band than Butterworth.

FilterPro™, Burr-Brown Corp.

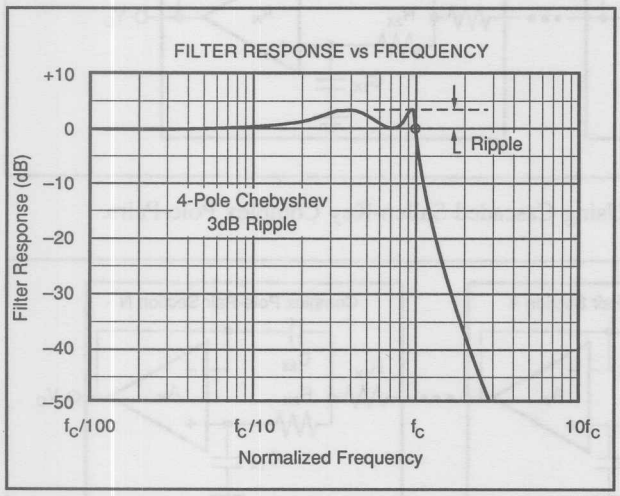

FIGURE 1a. Response vs Frequency of Even-Order (4-pole), 3dB-Ripple Chebyshev Filter Showing Cutoff at 0dB.

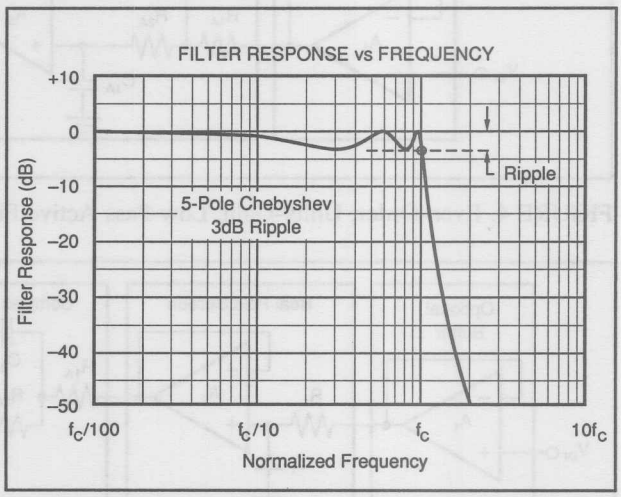

FIGURE 1b. Response vs Frequency of Odd-Order (5-pole), 3dB-Ripple Chebyshev Filter Showing Cutoff at –3dB.

Printed in U.S.A. August, 1991

Even-order filters designed with this program consist of cascaded sections of Sallen-Key complex pole-pairs.

Odd-order filters contain an additional real-pole section. Figures 2 to 5 show the recommended cascading arrangement. Lower Q stages are placed ahead of high Q stages to prevent op amp output saturation due to gain peaking. The program can be used to design filters up to 7th order.

USING THE FilterPro™ PROGRAM

With each data entry, the program automatically calculates values for filter components. This allows you to use a "what if" spreadsheet-type design approach. For example, you can quickly determine, by trial-and-error, how many poles are needed for a given roll-off.

RESISTOR VALUES

The program automatically selects standard capacitor values and calculates exact resistor values for the filter you have selected. In the "1% display" option, the program calculates the closest standard 1% resistor values. To select standard 1% resistor values, use the arrow keys to move the cursor to the **Display** menu selection. Then press **<ENTER>**. Because the program selects the closest 1% resistor for one resistor in each pole-pair, and then calculates the exact value for the second resistor before selecting the closest 1% value for the second resistor, it produces the most accurate filter design that can be implemented with 1% resistors.

Using the "Scale Resistors" menu option allows you to scale the computer-selected resistor value to match the application. The default value of 10kΩ is suggested for most applications.

Higher resistor values, e.g. 100kΩ, can be used with FET-input op amps. At temperatures below about 70°C, DC errors and excess noise due to op amp input bias current will be small. However, noise due to the resistors will be increased by the square-root of resistor increase.

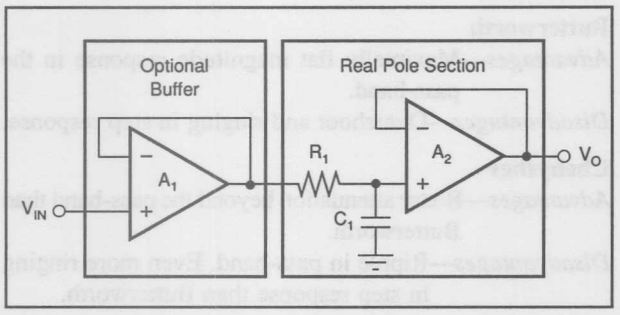

FIGURE 2. Real Pole Section (unity-gain, first-order Butterworth) $f_{-3dB} = 1/(2\pi R_1C_1)$

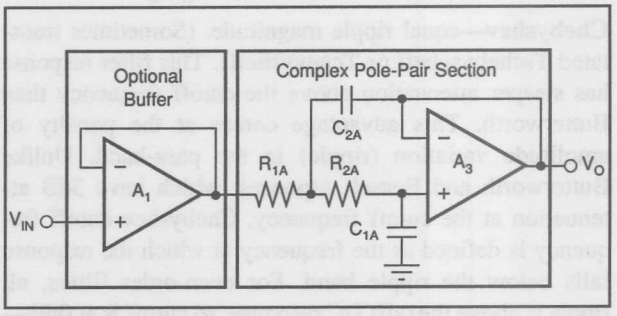

FIGURE 3. Second-Order, Unity-Gain, Low-Pass Filter Using Sallen-Key Configuration for Complex Pole-Pair.

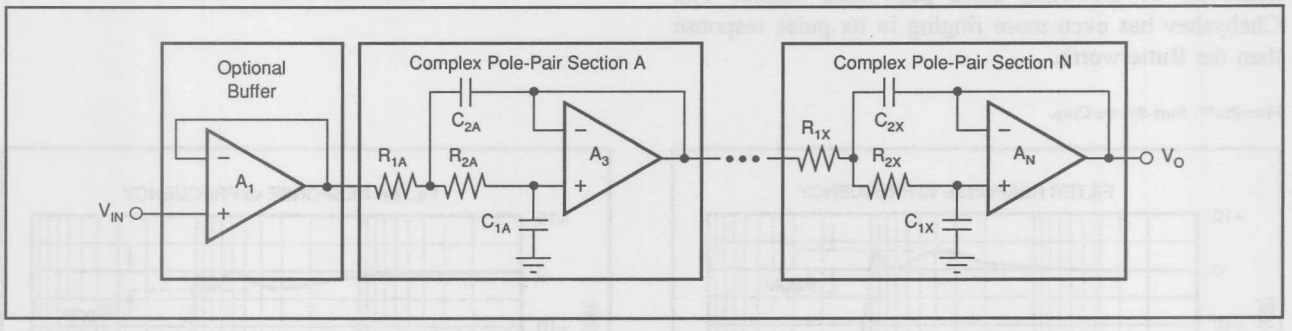

FIGURE 4. Even-Order, Unity-Gain, Low-Pass Active Filter Using Cascaded Sallen-Key Complex Pole-Pairs.

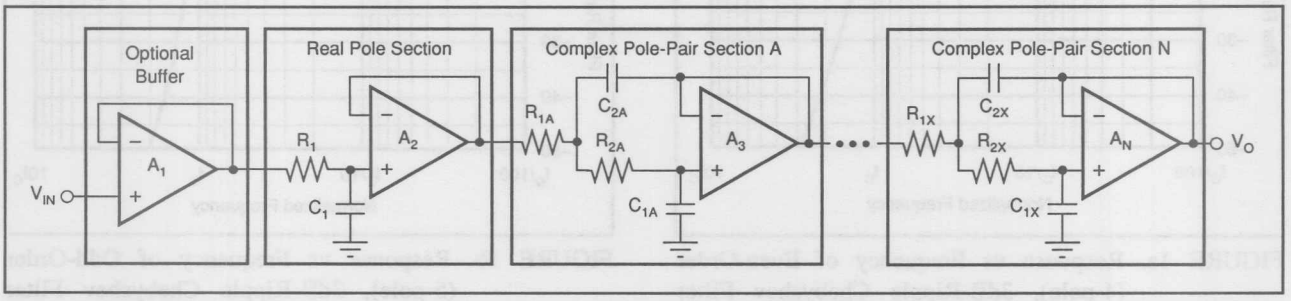

FIGURE 5. Odd-Order, Unity-Gain, Low-Pass Active Filter Using One Real Pole Followed by Cascaded Sallen-Key Complex Pole-Pairs.

Lower resistor values, e.g. 500Ω, are a better match for high-frequency filters using the OPA620 op amp.

Capacitor Values

Compared to resistors, capacitors with tight tolerances are more difficult to obtain and can be much more expensive. Using the "capacitor menu" option allows you to enter actual measured capacitor values. The program will then select exact or closest standard 1% resistor values as before. In this way, an accurate filter response can be assured with relatively inexpensive components.

If the common-mode input capacitance of the op amp used in a filter section is more than approximately 0.25% of C_1, it must be considered for accurate filter response. A capacitor menu option allows you to change the values of program-selected capacitors as explained earlier. To compensate for op amp capacitance, simply add the value of the op amp common-mode input capacitance to the actual value of C_1. The program then automatically recalculates the exact or closest 1% resistor values for accurate filter response.

Op Amp Selection

It is important to choose an op amp that can provide the necessary DC precision, noise, distortion, and bandwidth.

In a low-pass filter section, maximum gain peaking at f_n (the section's natural frequency) is very nearly equal to Q. As a rule of thumb, for a unity-gain Sallen-Key section, the op amp bandwidth should be at least $100 \cdot Q^3 \cdot f_n$. For a real-pole section, op amp bandwidth should be at least $50 \cdot f_n$. For example, a 20kHz 5-pole Butterworth filter needs a 8.5MHz op amp in the Q = 1.62 section.

To aid in selection of the op amp, a program option can display f_n and Q for each section. Press **<ENTER>** in the Display option of the menu. Although Q is formally

Attach Disk Sleeve Here.

Call (602) 741-3978 to down-load a DOS-compatible executable file. Down-load the FILTER1 file from the components, analog circuit functions area. File transfers are supported by XMODEM, Kermit, ASCII and Sealink protocols. Communications settings are 300/1200/2400 baud, 8-N-1.

Or,

Call John Conlon, Applications Engineer
(800) 548-6132 for a DOS compatible 5-1/4" disk.

defined only for complex poles, it is convenient to use a Q of 0.5 for calculating the op amp gain required in a real-pole section.

The slew rate of the op amp must be greater than $\pi \cdot V_{Op\text{-}p} \cdot$ FILTER BANDWIDTH for adequate full-power response. For example, a 100kHz filter with 20Vp-p output requires an op amp slew-rate of at least 6.3V/µs. Burr-Brown offers an excellent selection of op amps which can be used for high performance active filters. The guide below lists some good choices.

OP AMP SELECTION GUIDE, (IN ORDER OF INCREASING SLEW RATE.)
T_A = 25°C, V_S=±15V, specifications typ, unless otherwise noted, min/max specifications are for high-grade model.

OP AMP MODEL	BW typ (MHz)	FPR[1] typ (kHz)	SR typ (V/µs)	V_{os} max (µV)	V_{os}/dT max (µV/°C)	NOISE at 10kHz (nV/√Hz)	C_{CM}[3] (pF)
OPA177	0.6	3	0.2	10	±0.1	8	1
OPA27	8	30	1.9	25	±0.6	2.7	1
OPA2107[2] dual	4.5	280	18	500	±5	8	4
OPA2604[2] dual	10	400	25	2000	±5 typ	10	10
OPA602[2]	6	500	35	250	±2	12	3
OPA404[2] quad	6	500	35	1000	±3 typ	12	3
OPA627[2]	16	875	55	100	±0.8	4.5	7
OPA620 (V_S = ±5V)	300	16MHz (5Vp-p)	250	500	±8 typ	2.3 (at 1MHz)	1

NOTES: (1) Unless otherwise noted, FPR is full power response at 20Vp-p as calculated from slew rate. (2) These op amps have FET inputs. (3) Common-mode input capacitance.

CAPACITOR SELECTION

Capacitor selection is very important for a high-performance filter. Capacitor behavior can vary significantly from ideal, introducing series resistance and inductance which limit Q. Also, nonlinearity of capacitance vs voltage causes distortion.

Common ceramic capacitors with high dielectric constants, such as "high-K" types can cause errors in filter circuits. Recommended capacitor types are: NPO ceramic, silver mica, metallized polycarbonate; and, for temperatures up to 85°C, polypropylene or polystyrene.

THE UAF42 UNIVERSAL ACTIVE FILTER

For other filter designs, consider the Burr-Brown UAF42 Universal Active Filter. It can easily be configured for a wide variety of low-pass, high-pass, or band-pass filters. It uses the classical state-variable architecture with an inverting amplifier and two integrators to form a pole-pair. The integrators include on-chip 1000pF, 0.5% capacitors. This solves one of the most difficult problems in active filter implementation—obtaining tight tolerance, low-loss capacitors at reasonable cost.

Simple design procedures for the UAF42 allow implementation of Butterworth, Chebyshev, Bessel, and other types of filters. An extra FET-input op amp in the UAF42 can be used to form additional stages or special filter types such as band-reject and elliptic. The UAF42 is available in a standard 14-pin DIP. For more information about the UAF42 request Burr-Brown Product Data Sheet PDS-1070.

EXAMPLES OF FILTER RESPONSE

Figures 6a and 6b show actual measured magnitude response plots for 5th-order 20kHz Butterworth, 3dB Chebyshev and Bessel filters designed with the program. The op amp used in all filters was the OPA627. As can be seen in Figure 5, the initial roll-off of the Chebyshev filter is fastest and the roll-off of the Bessel filter is the slowest. However, each of the 5th-order filters ultimately rolls off at –N • 20dB/decade, where N is the filter order (–100dB/decade for a 5-pole filter).

The oscilloscope photographs show the step response for each filter. As expected, the Chebyshev filter has the most ringing, while the Bessel has the least.

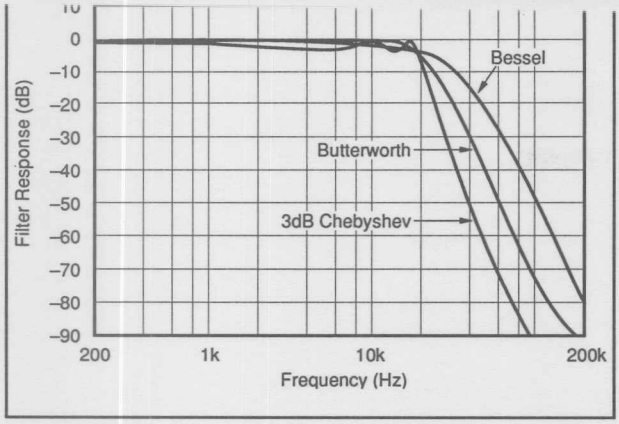

FIGURE 6a. Gain vs Frequency for 5th-Order 20kHz Butterworth, 3dB Chebyshev, and Bessel Unity-Gain Low-Pass Filters Showing Overall Filter Response.

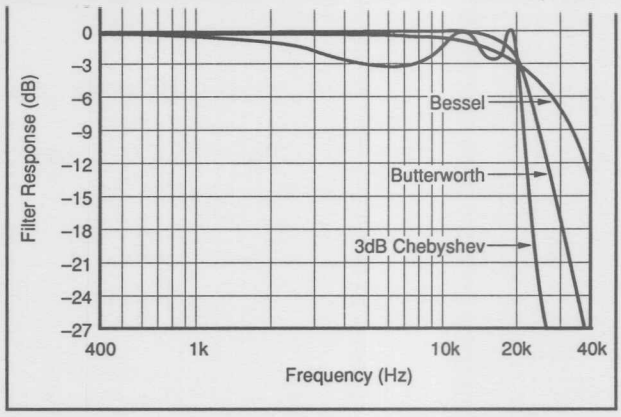

FIGURE 6b. Gain vs Frequency for 5th-Order 20kHz Butterworth, 3dB Chebyshev, and Bessel Unity-Gain Low-Pass Filters Showing Transition Band Detail.

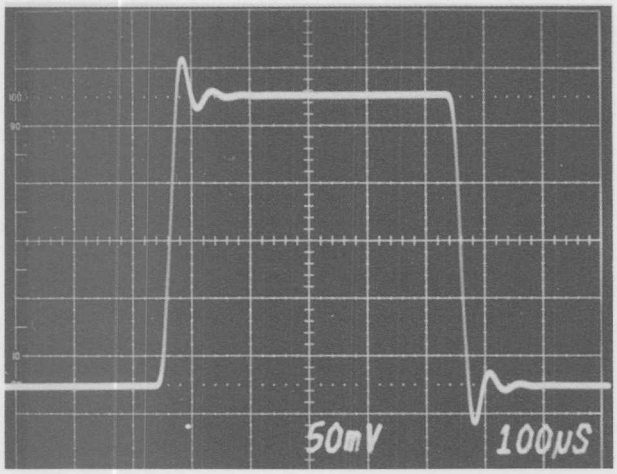

FIGURE 7. Step Response of 5th-Order 20kHz Butterworth Low-Pass Filter.

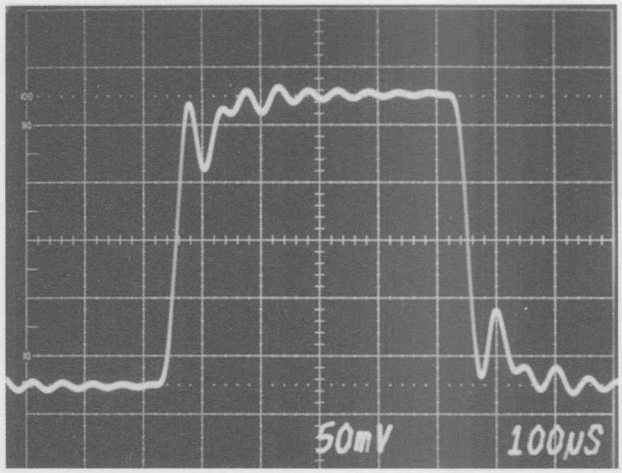

FIGURE 8. Step Response of 5th-Order 20kHz 3dB Ripple Chebyshev Low-Pass Filter.

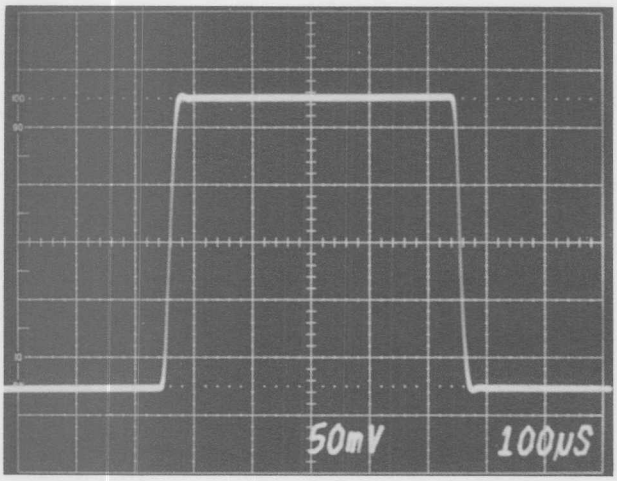

FIGURE 9. Step Response of 5th-Order 20kHz Bessel Low-Pass Filter.

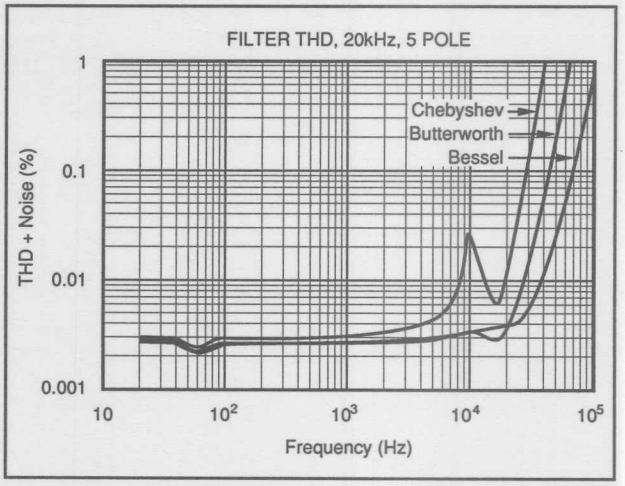

FIGURE 10. Measured Distortion for the Three 20kHz Low-Pass Filters.

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FAST SETTLING LOW-PASS FILTER

By Rod Burt and R. Mark Stitt (602) 746-7445

Noise reduction by filtering is the most commonly used method for improving signal-to-noise ratio. The increase in settling time, however, can be a serious disadvantage in some applications such as high-speed data acquisition systems. The nonlinear filter described here is a simple way to get a four-to-one improvement in settling time as compared to a conventional filter.

To understand the circuit, first consider the dynamics of a single-pole RC filter (Figure 1). Filtering reduces broadband or "white" noise by the square root of the bandwidth reduction as shown by the following calculation:

$$e_n^2 = \int_{f_1}^{f_2} e_B^2 \, df = e_B^2 \cdot f \Big|_{f_1}^{f_2}$$

$$e_n = e_B (f_2 - f_1)^{1/2}$$

Where:
e_n = total noise (Vrms)
e_B = broadband noise ($V/\sqrt{Hz}$)
f_1, f_2 = frequency range of interest (Hz)

In other words, if the frequency range ($f_2 - f_1$) is reduced by a factor of 100, the total noise would be reduced by a factor of 10.

Unfortunately, settling time depends on bandwidth. The penalty for the noise reduction is increased settling time. For a single-pole filter, the time needed for the signal to settle to any given accuracy can be calculated as follows:

For V_O/V_{IN} at time = t_S

$$\frac{V_O}{V_{IN}} = 1 - e^{-(t_S/[R_1 \cdot C_1])}$$

$$-\left(\frac{V_O}{V_{IN}} - 1\right) \cdot 100 = \%$$

therefore

$$t_S = -\ln(\%/100) \cdot R_1 \cdot C_1$$

Where:
t_S = settling time (s)
% = percent accuracy at t_S
$R_1 \cdot C_1$ = RC time constant ($\Omega \cdot F$) or (s)

For example, if a settling to 0.01% is needed,

$$\ln(0.01/100) = -9.2$$

In other words, it takes 9.2 $R_1 \cdot C_1$ time constants for an input step to settle to within 0.01% of its final value.

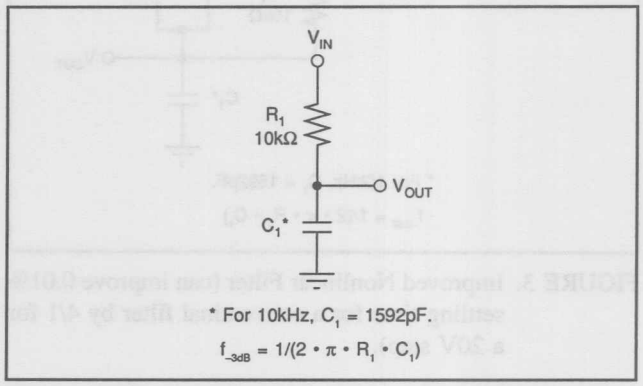

FIGURE 1. Conventional Single-Pole RC Filter.

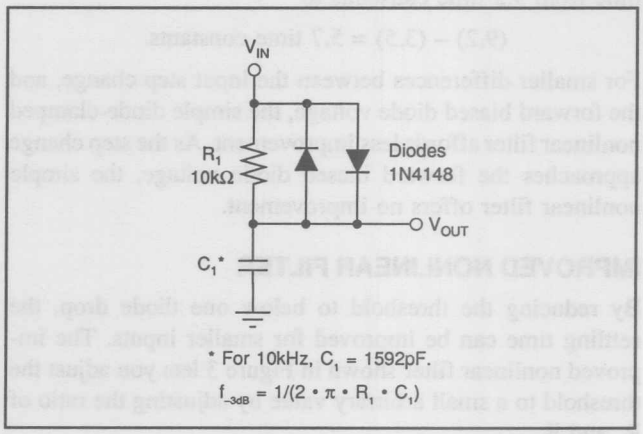

FIGURE 2. Diode-Clamped Nonlinear Filter (can improve 0.01% settling time for a conventional filter by 2/1 for a 20V step).

NONLINEAR FILTER

To understand how a nonlinear filter can improve settling time, consider the simple diode clamped nonlinear filter, shown in Figure 2. Settling time is improved because the filter capacitor, C_1, is charged faster through the low forward biased diode impedance (R_{ON}) during the initial portion of a large input step change. When the difference between the input and output voltage becomes less than the forward biased diode drop (about 0.6V), the diode turns off and C_1 reacts with R_1 alone. At this point, the circuit behaves like a normal single-pole RC filter.

Assuming diode R_{ON} is negligible, the improvement in settling time depends on the ratio of the input step voltage to the forward biased diode voltage. For a step of –10V to +10V (a 20V step), the improvement is ln(0.60/20) or 3.5 time constants. In other words, for a 20V step, the simple

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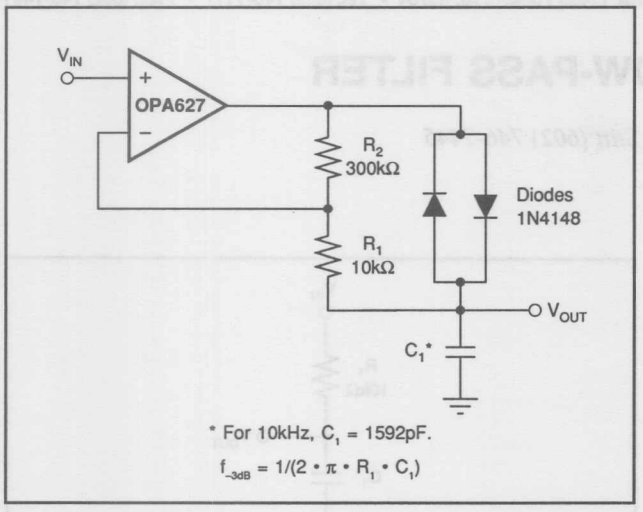


FIGURE 3. Improved Nonlinear Filter (can improve 0.01% settling time for a conventinal filter by 4/1 for a 20V step).

diode clamped nonlinear filter can improve 0.01% settling time from 9.2 time constants to

$$(9.2) - (3.5) = 5.7 \text{ time constants.}$$

For smaller differences between the input step change, and the forward biased diode voltage, the simple diode-clamped nonlinear filter affords less improvement. As the step change approaches the forward biased diode voltage, the simple nonlinear filter offers no improvement.

IMPROVED NONLINEAR FILTER

By reducing the threshold to below one diode drop, the settling time can be improved for smaller inputs. The improved nonlinear filter shown in Figure 3 lets you adjust the threshold to a small arbitrary value by adjusting the ratio of R_1 and R_2.

To see how the improved nonlinear filter works, notice that the op amp forces the voltage at its inverting input to be the same as at the noninverting input. For small differences between the output voltage and the input voltage, the difference is dropped across the 10kΩ resistor, R_1, and the filter behaves like a single-pole filter with an $R_1 \cdot C_1$ time constant. The voltage divider formed by R_1 and R_2 amplifies the voltage difference across R_1, as seen at the top of R_2, by $(1 + R_2/R_1)$. As the voltage across the R_1, R_2 divider becomes larger, one of the diodes (which one depends on signal polarity) begins to conduct, and the capacitor is rapidly charged through it. This occurs at a voltage difference between the input and output of about $0.6V/(1 + R_2/R_1)$ or about 20mV with the values shown. With the diode forward biased, the time constant of the filter becomes very small, limited only by op amp slew rate or current limit.

To determine the component values for the improved nonlinear filter, consider the noise-reduction requirements of the filter. For example, if you want to filter the noise of a 20V full-scale signal to 0.01% resolution, the peak noise must be filtered to less than 0.01% of 20V, i.e. 2mV peak.

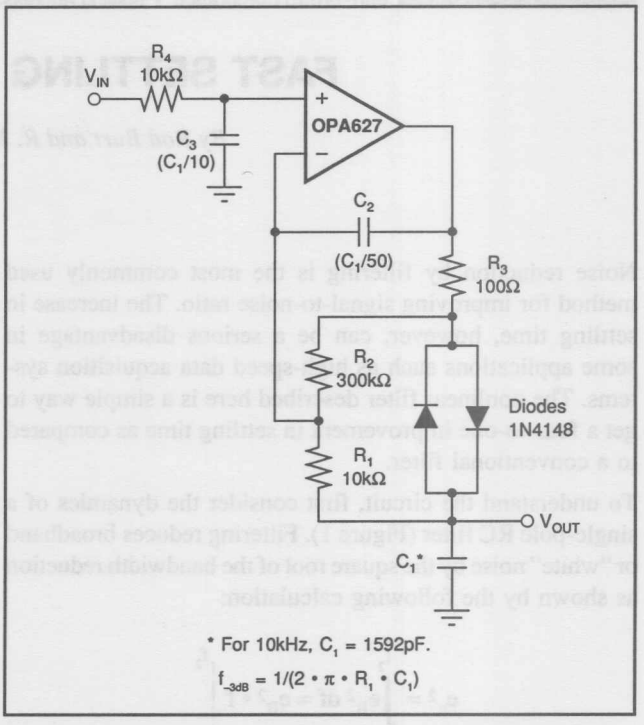


FIGURE 4. Improved Nonlinear Filter with R_4, C_3 Prefilter and R_3, C_2 Network to Assure Op Amp Stability in Driving C_1.

A clamp threshold of ten times this peak (20mV) is an arbitrary but ample threshold. The component values shown in Figure 3 set the filter's threshold to 20mV. For a 20V step as before, the improvement in settling time is ln(0.02/20) = 6.9 time constants. In other words, for a 20V step, the improved nonlinear filter can improve 0.01% settling time from 9.2 time constants to (9.2) – (6.9) = 2.3 time constants—a four-to-one improvement.

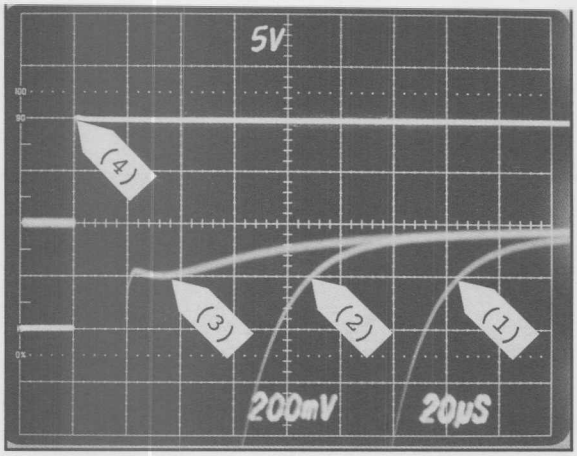
SOME SIGNALS REQUIRE PREFILTERING

In some instances, the input signal may have noise peaks above the 20mV threshold of the nonlinear filter. If the noise of the input signal to the nonlinear filter is greater than the 20mV threshold, the filter will mistake the noise for a step input and fail to filter it out. To prevent this situation an input prefilter can be added to the nonlinear filter as shown in Figure 4.

The prefilter's bandwidth is set by R_4 and C_3. To minimize the prefilter's effect on settling time, its bandwidth is set ten times higher than the bandwidth of the nonlinear filter. At this higher bandwidth, the prefilter's effect on settling time is negligible, and the noise at the prefilter's output is $\sqrt{10}$ times greater than 2mV (a little over 6mV peak). A noise level of 6mV provides a comfortable margin for a 20mV threshold.

ASSURE OP AMP STABILITY

Op amps tend to become unstable and oscillate when driving large capacitive loads. The C_2, R_3 network, shown in Figure 4, assures op amp stability when driving large values of C_1



Traces 1 to 3 show settling response for the various filters. Gain of the signals is 100V/V, so each division of the scope graticule represents 2mV (i.e. each division = 0.01%).

Trace 1 is a standard 10kHz single-pole RC filter.

Trace 2 is a diode-clamped 10kHz nonlinear filter.

Trace 3 is the improved 10kHz nonlinear filter shown in Figure 4.

Trace 4 is the ±10V input signal at 5V/division.

FIGURE 5. Settling-Time Response of Standard and Nonlinear Filters.

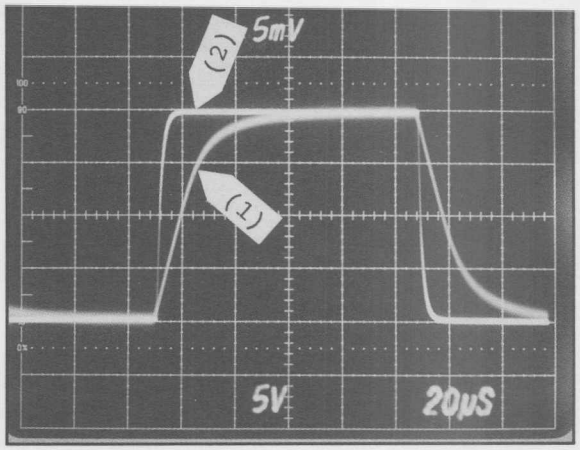
through the low impedance of the forward biased diode network. The C_2, R_3 network may not be needed if C_1 is small.

When choosing the op amp for the improved filter, make sure it has high output drive capability for charging C_1, and that its slew rate, settling time, and DC precision are adequate for the necessary filter response. The OPA627 shown has an excellent combination of DC precision, high slew rate, fast settling time and high output drive capability. The 16MHz bandwidth of the OPA627 gives excellent results for filters with –3dB bandwidths up to 100kHz. Also, notice that the op amp noise adds (at unity gain) to the signal noise. When a low noise op amp is used, this noise will be negligible in most instances.

The OPA627 contributes only a 6% increase in noise to the minimum theoretical noise of the 10kΩ resistor used in the filter. Remember that noise adds as the square root of the sum of the squares. To determine how much the $4.5nV/\sqrt{Hz}$ noise of the OPA627 adds to the $12.8nV/\sqrt{Hz}$ noise of the 10kΩ resistor, calculate the noise of the two components and compare that to the noise of the resistor alone:

$$\sqrt{(4.5)^2 + (12.8)^2}\ /12.8 = 1.06, \text{ a 6\% increase}$$

Figure 5 is a triple exposure scope photo showing the filter output error settling time response for the three circuits to a –10V to +10V input step (20V). The bandwidth of each filter is set to 10kHz. The settling response is in a gain of 100 so that each box represents 2mV, or 0.01% of a 20V step. The filter has settled to 0.01% when the trace is within one box of the base grid.



Trace 1 shows 10kHz single-pole filter response for a ±10mV input step.

Trace 2 shows fast response for a ±10V input step.

FIGURE 6. Comparison of Large and Small Signal Step Response of the Improved Nonlinear Filter.

FILTER TYPE	THEORETICAL SETTLING TIME (time constants)	THEORETICAL SETTLING TIME (µs)(1)
Single-Pole RC	9.2	147
Diode-Clamped Nonlinear	5.7	91
Improved Nonlinear	2.3	37

NOTE: (1) Settling to 0.01% of final value for a 10kHz filter.

TABLE I. Theoretical Settling Times for Various Filters.

For a 10kHz filter, one RC time constant is 15.9µs. Ignoring input slew rate, and diode forward resistance (good approximations for the 10kHz filter when using an OPA627 op amp), the theoretical settling times are shown in Table I.

Notice that the actual measurements shown by the scope photos agree to the theoretical values within the resolution of the photographs.

Figure 6 is a double exposure scope photograph of the improved nonlinear filter operating at a high and low signal level. At the low level (a ±10mV input step), the response is that of a 10kHz single-pole RC filter as expected. At the high level (a ±10V input step), the greatly improved settling response is observed.

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A LOW NOISE, LOW DISTORTION DESIGN FOR ANTIALIASING AND ANTI-IMAGING FILTERS

By Rick Downs (602) 746-7327

Many customers have requested more information about the analog low-pass filters that appear in many of our PCM audio data sheets. They are used for antialiasing in front of ADCs or for smoothing on the output of DACs. The following bulletin is an excellent primer on the subject. —Ed.

In any digitizing system, antialiasing and anti-imaging filters are used to prevent the signal frequencies from "folding back" around the sample frequency and causing false (or alias) signals from appearing in the signal we are attempting to digitize. Very often, these filters must be very complex, high order analog filters in order to do their job effectively.

As sampling rates of converter systems have increased, however, oversampling may be used to reduce the filters' stopband attenuation requirements[1][2]. In digital audio systems, 4x oversampling may be used, and it can be shown[3] that for an antialiasing filter (which precedes the ADC), a simple sixth order filter may be used. For the output side, after the DAC, a simple third order filter may be used. Realizing these filters in a way that maintains extremely low noise and low distortion then becomes a challenge.

Compact disk player manufacturers began using a filter topology that was described many years ago—the Generalized Immittance Converter (GIC)[4]. This topology allows one to easily realize active filters beginning from a passive filter design. In addition, the GIC filter provides extremely low distortion and noise, at a reasonable cost. Compared with more familiar feedback filter techniques, such as Sallen & Key filter topologies, the GIC filter can be shown to have superior noise gain characteristics, making it particularly suitable for audio and DSP type applications[5].

We use this type of filter on our demonstration fixtures for the PCM1750 and PCM1700, dual 18-bit ADC and DAC, respectively. When sending out schematics of these demonstration fixtures, very often the first question is, "What are those filters anyway?" Well, they're GIC filters, and here's how you design them and how they perform. Stepping through this design process will allow you to modify these designs for a different cutoff frequency for your particular application. A more detailed treatment of the theory behind these filters may be found in Huelsman and Allen[6].

As stated above, for oversampling digital audio applications, third and sixth order filters are adequate. Thus, we may design our first GIC filter by designing a third order filter. The filter characteristic most desirable for sensitive DSP type applications is linear-phase. The linear-phase filter is sometimes called a Bessel (or Thomson) filter. The linear-phase filter has constant group delay. This means that the phase of the filter changes linearly with frequency, or that

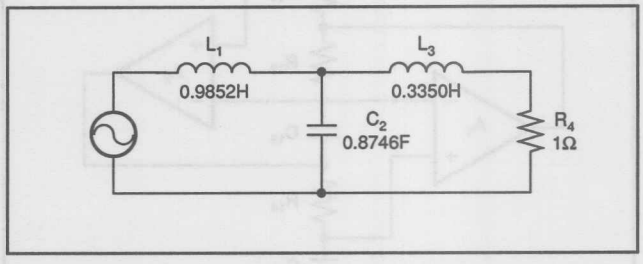

FIGURE 1. Passive Third Order, Linear-Phase, Low-Pass Filter Prototype.

the group delay is constant. These filters maintain phase information for sensitive DSP applications such as correlation, and preserve transient response. These characteristics are critical in audio applications as well, because they affect sound quality greatly.

Thus, we begin the design process by selecting a passive, third order linear-phase filter design that will be realized using this active approach. The passive design shown in Figure 1 is neither a Butterworth nor a Bessel response; it is something in between. The component values for this particular response, optimized for phase linearity and stopband attenuation, were found through exhaustive computer simulations and empirical analysis. Component values for standard Butterworth and Bessel responses may be found in standard filter tables, such as those available in Huelsman and Allen[7]. This circuit is then transformed to an active circuit by multiplying all circuit values by 1/s, which changes all inductors to resistors, all resistors to capacitors, and all capacitors to Frequency Dependent Negative Resistors (FDNRs). These FDNRs have the characteristic impedance of

$$\frac{1}{s^2C}$$

and may be realized using the GIC circuit. Thus, L_1 becomes R_1, C_2 becomes $1/s^2C_2$, L_3 becomes R_3, and the terminating resistor R_4 becomes C_4, as shown in Figure 2.

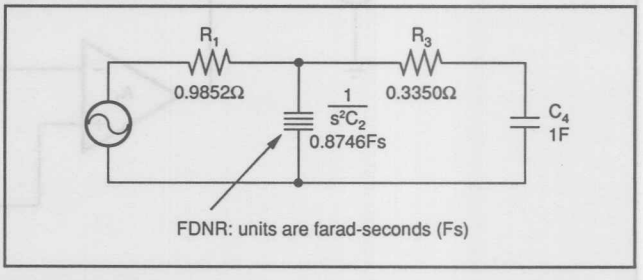

FIGURE 2. Filter of Figure 1 Transformed by Multiplying All Component Values by 1/s.

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The FDNR is then realized by the GIC circuit shown in Figure 3. The value of the FDNR is determined by

$$D = (R_{12} \cdot R_{14} \cdot C_{13} \cdot C_{15})/R_{11}$$

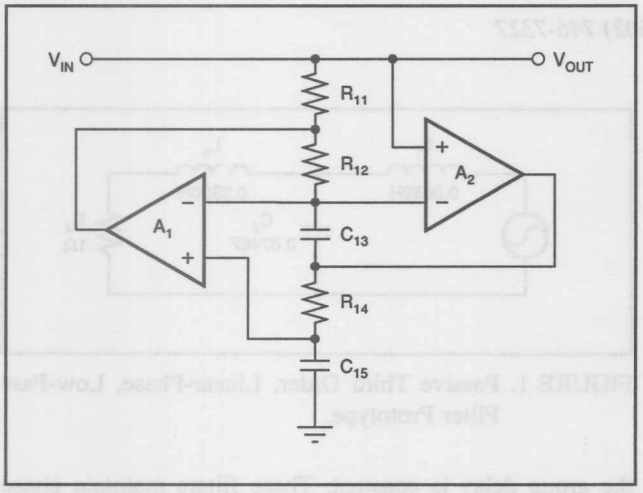

FIGURE 3. Frequency Dependent Negative Resistor (FDNR) Realized Using Generalized Immittance Converter (GIC).

Thus by setting $R_{11} = R_{12} = 1$ and $C_{13} = C_{15} = 1$, D is entirely determined by the value of R_{14}. For the FDNR of Figure 2, $R_{14} = 0.8746\Omega$.

The entire third order filter circuit is shown in Figure 4. This circuit now must be scaled in frequency to give the desired cutoff frequency, and then must be scaled in impedance to allow for the use of reasonable sized component values.

The filter circuits found in filter tables, such as that in Figure 1 and the active realization of this passive circuit (Figures 2 and 4), are designed for a cutoff frequency of $\omega = 1$ rad/s. To make the filter have the cutoff frequency we desire, we must scale it in frequency by the scaling factor

$$\Omega_N = 2\pi f_c$$

This scaling factor is applied to all frequency-determining components—capacitors in this case. The example filter will be designed for audio, so we might consider a cutoff frequency of 20kHz. However, linear-phase filters tend to roll-off very slowly, causing 1-2dB attenuation before the cutoff frequency; generally audio systems prefer to have their frequency response out to 20kHz to be within 0.1dB. The example filter then will have a cutoff frequency of 40kHz, commonly used in many of today's CD players. All capacitor values are divided by the frequency scaling factor, so $C_{13} = C_{15} = C_4 = 3.98\mu F$.

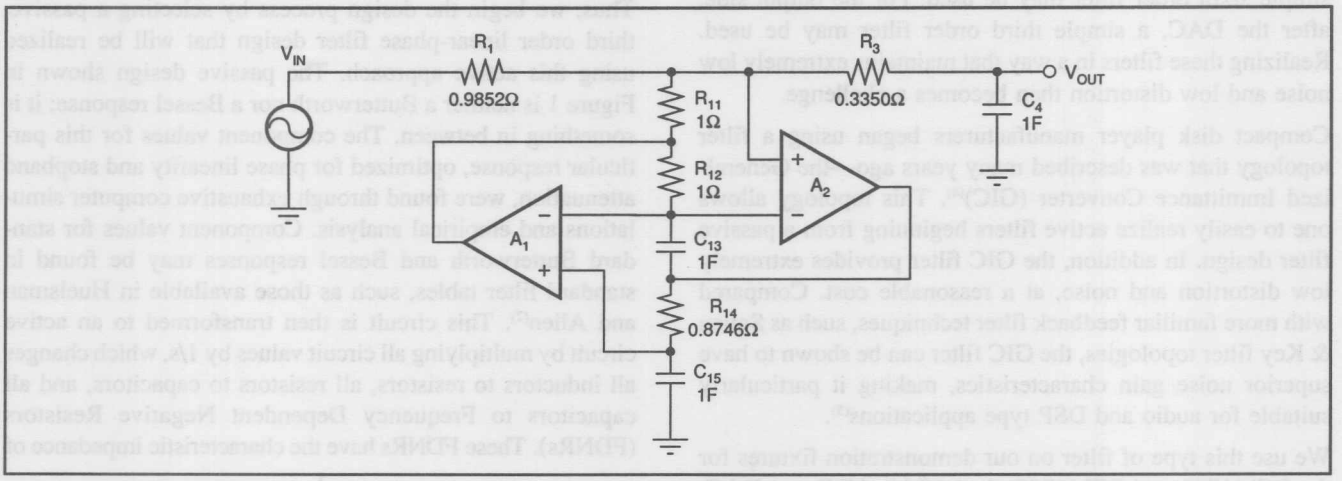

FIGURE 4. Third Order, Linear-Phase Realization of Circuit Shown in Figure 2.

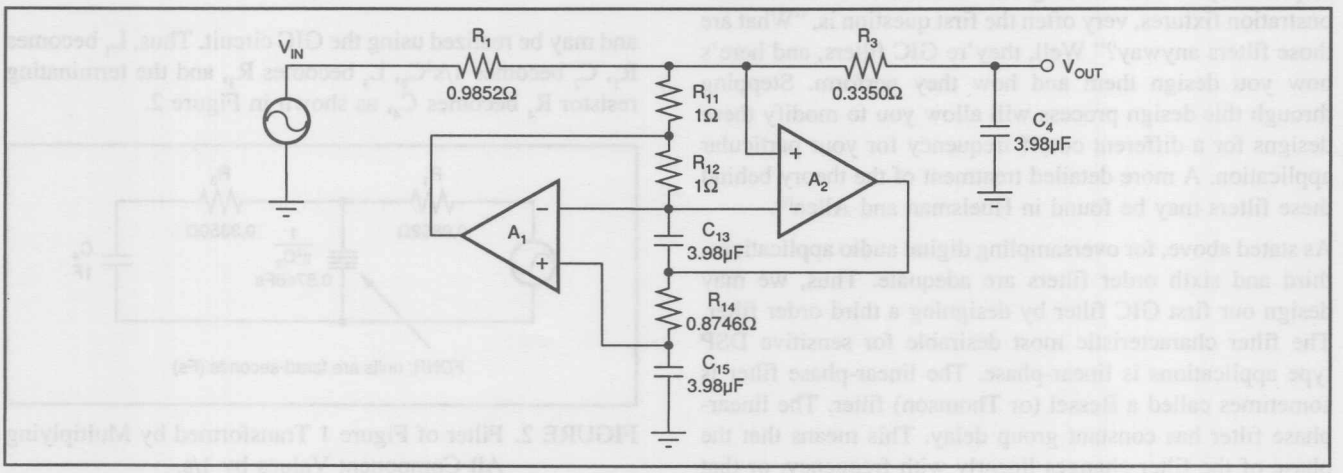

FIGURE 5. Circuit of Figure 4 Scaled to a 40kHz Cutoff Frequency.

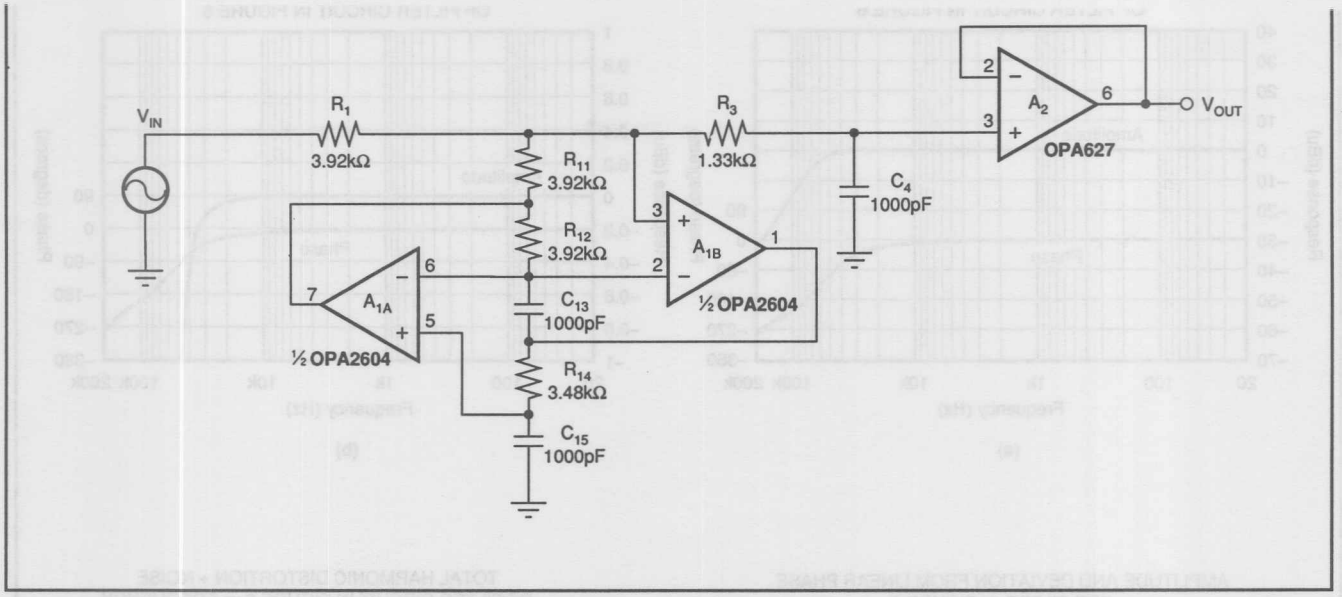

FIGURE 6. Circuit of Figure 5 Scaled in Impedance (note use of buffer amplifier to reduce output impedance of the filter).

The filter (Figure 5) could now be built, but the large capacitor values and low resistance values could pose practical problems. To alleviate this, the impedances of the circuit are scaled by an impedance scale factor:

$$Z_n = \frac{\text{Present C value}}{\text{Desired C value}}$$

By choosing the desired C value as 1000pF, $Z_n = 3.97 \times 10^3$. This impedance scaling factor then is multiplied by all resistor values to find the new resistor values, and divides all the capacitor values, taking them from the present values to the desired capacitance.

The final filter design is shown in Figure 6. Since the output impedance of this filter is relatively high, it's a good idea to buffer the output using an op amp voltage follower. Amplitude and phase response of this filter is shown in Figure 7a. Figure 7b is a closer look at the amplitude response in the passband—the frequency response is flat well within 0.1dB out to 20kHz.

Figure 7c is a plot of the frequency response of the filter (solid line) and the filter's deviation from linear phase (dotted line). Note the phase scale; the phase response is well within 0.1° of linear phase in the 1kHz-20kHz region, where the ear is most sensitive to phase distortion.

Figure 7d is a plot of the total harmonic distortion plus noise (THD + N) of this filter versus frequency. At about –108dB, this would be suitable for digital systems with true 18-bit converter performance!

To make a sixth order filter, you can repeat the design process above from a passive realization and directly implement a filter. This implementation is very sensitive to the gain-bandwidth product (GBW) match of all of the op amps used, however; for a 40kHz cutoff frequency, an op amp with extremely high GBW would be required. An example of a sixth order, 40kHz Butterworth filter realized in this fashion is shown in Figure 8, but its frequency response (Figure 9) is less than hoped for due to the GBW limitations described above.

A simpler solution is to cascade two of the third order sections designed above. This cascaded design (Figure 10) works equally well for most applications.

Figure 11 (a-d) shows the performance of this cascaded filter design. Note that the phase linearity and THD + N are still excellent using this approach.

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(4) S.K. Mitra, *Analysis and Synthesis of Linear Active Networks*, John Wiley & Sons, Inc., New York, pg. 494, 1969.

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(6) L.P. Huelsman, P.E. Allen, *Introduction to the Theory and Design of Active Filters*, McGraw-Hill, New York, 1980.

(7) Ibid.

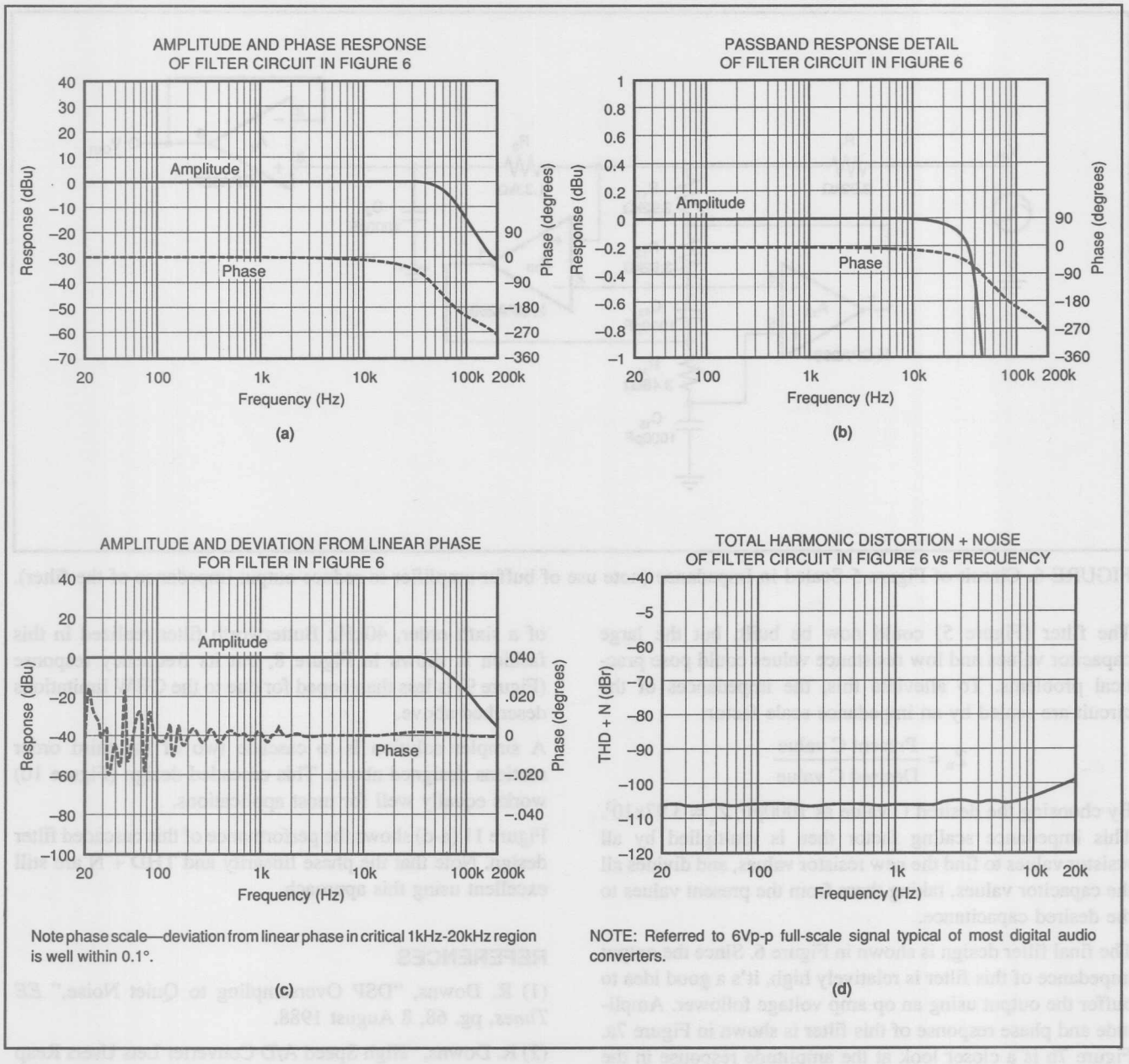

FIGURE 7. Performance Details of Figure 6 Circuit.

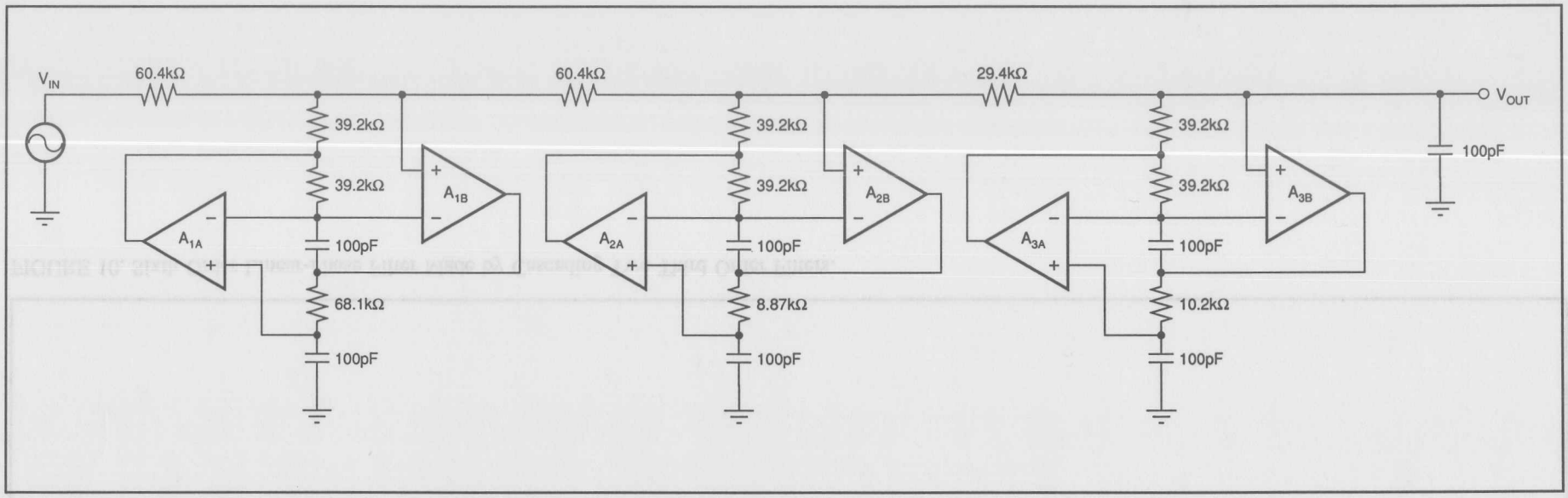

FIGURE 8. Sixth Order Butterworth Filter Realized by Method Outlined in Text (actual circuit would require output buffer amplifier to lower output impedance).

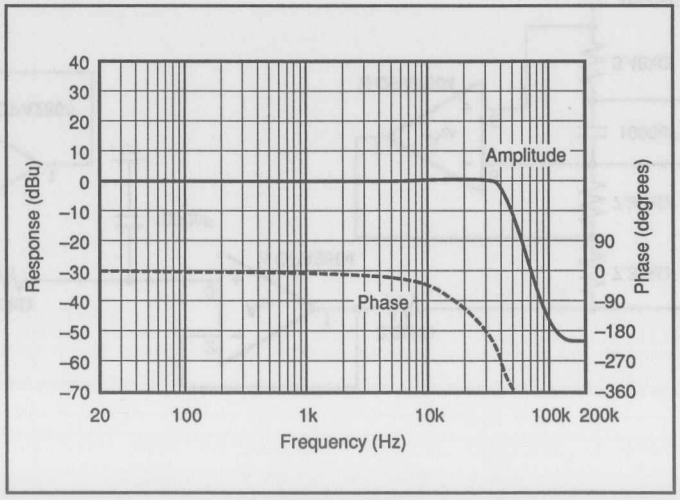

FIGURE 9. Amplitude (solid line) and Phase (dotted line) Response of Filter Circuit in Figure 8. (Note flattening of stopband response near 150kHz due to inadequate GBW of operational amplifiers used.)

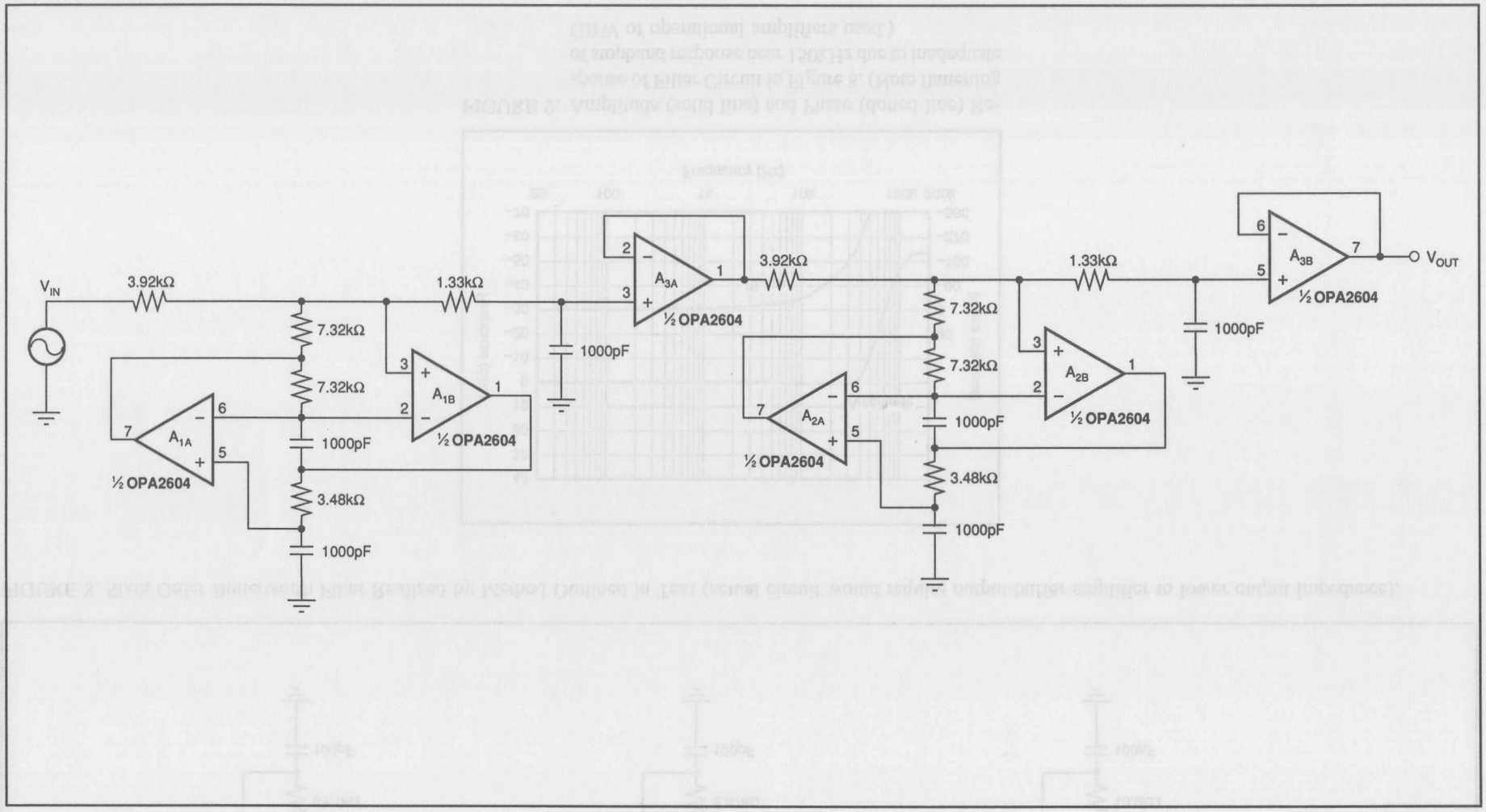

FIGURE 10. Sixth Order Linear-Phase Filter Made by Cascading Two Third Order Filters.

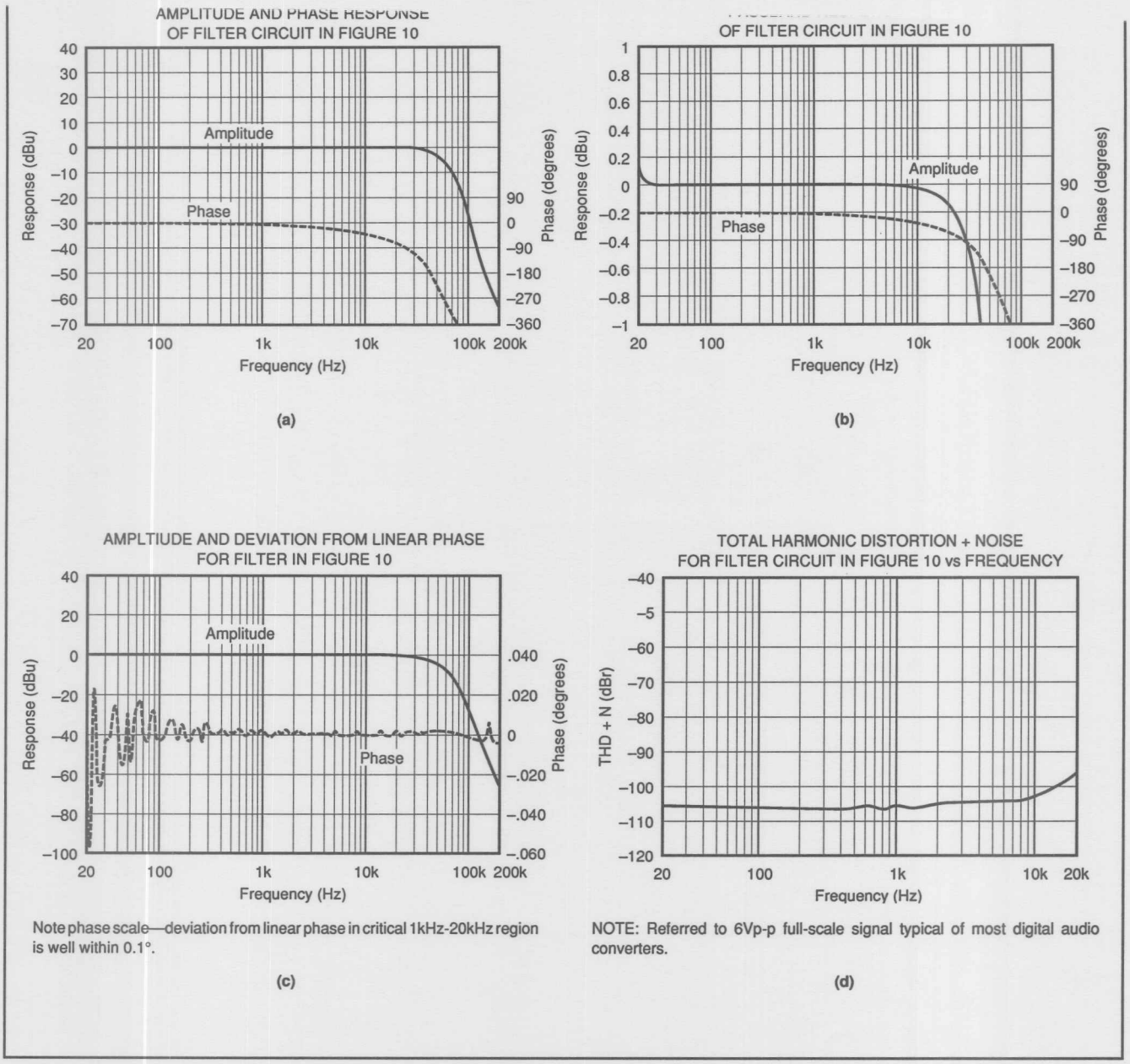

FIGURE 11. Performance Details of Figure 10 Circuit.

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MFB LOW-PASS FILTER DESIGN PROGRAM

By Bruce Trump and R. Mark Stitt (602) 746-7445

Although low-pass filters are vital in modern electronics, their design and verification can be tedious and time consuming. The Burr-Brown FilterPro™ program, FILTER2, makes it easy to design low-pass active filters. The program is intended to aid in the design of low-pass filters implemented with the Multiple Feedback (MFB) topology. Because there are instances where the Sallen-Key filter topology is a better choice, the program also supports Sallen-Key low-pass filter design.

An ideal low-pass filter would completely eliminate signals above the cutoff frequency, and perfectly pass signals below cutoff (in the pass-band). In real filters, various trade-offs are made in an attempt to approximate the ideal. Some filter types are optimized for gain flatness in the pass-band, some trade-off gain variation (ripple) in the pass-band for steeper roll-off, still others trade-off both flatness and rate of roll-off in favor of pulse-response fidelity. FILTER2 supports the three most commonly used all-pole filter types: Butterworth, Chebyshev, and Bessel.

Butterworth (maximally flat magnitude). This filter has the flattest possible pass-band magnitude response. Attenuation is –3dB at the design cutoff frequency. Attenuation above the cutoff frequency is a moderately steep –20dB/decade/pole. The pulse response of the Butterworth filter has moderate overshoot and ringing.

Chebyshev (equal ripple magnitude). (Also transliterated Tschebychev, Tschebyscheff or Tchevysheff.) This filter type has steeper attenuation above the cutoff frequency than Butterworth. This advantage comes at the penalty of amplitude variation (ripple) in the pass-band. Unlike Butterworth and Bessel responses, which have 3dB attenuation at the cutoff frequency, Chebyshev cutoff frequency is defined as the frequency at which the response falls below the ripple band. For even-order filters, all ripple is above the 0dB-gain DC response, so cutoff is at 0dB—see Figure 1A. For odd-order filters, all ripple is below the 0dB-gain DC response, so cutoff is at –(ripple) dB—see Figure 1B. For a given number of poles, a steeper cutoff can be achieved by allowing more pass-band ripple. The Chebyshev has even more ringing in its pulse response than the Butterworth.

Bessel (maximally flat time delay). (Also called Thomson.) Due to its linear phase response, this filter has excellent pulse response (minimal overshoot and ringing). For a given number of poles, its magnitude response is not as flat, nor is its attenuation beyond the –3dB cutoff frequency as steep as the Butterworth. It takes a higher-order Bessel filter to give a magnitude response which approaches that of a given Butterworth filter, but the pulse response fidelity of the Bessel filter may make the added complexity worthwhile.

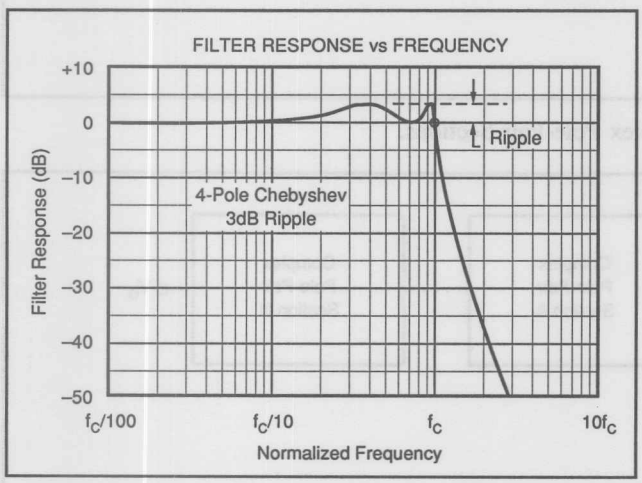

FIGURE 1A. Response vs Frequency of Even-Order (4-pole), 3dB Ripple Chebyshev Filter Showing Cutoff at 0dB.

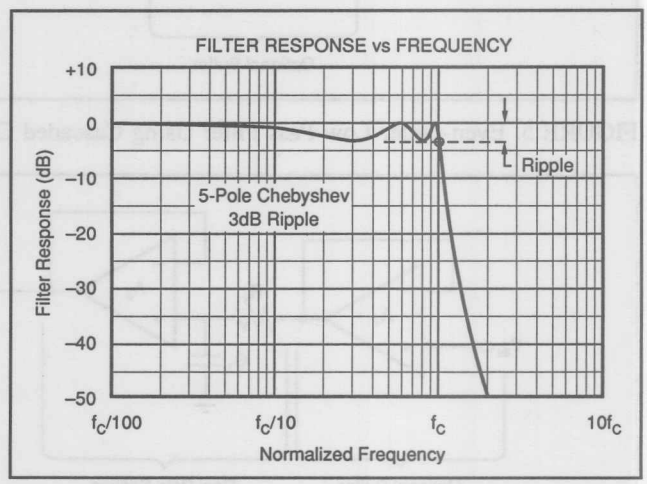

FIGURE 1B. Response vs Frequency of Odd-Order (5-pole), 3dB Ripple Chebyshev Filter Showing Cutoff at –3dB.

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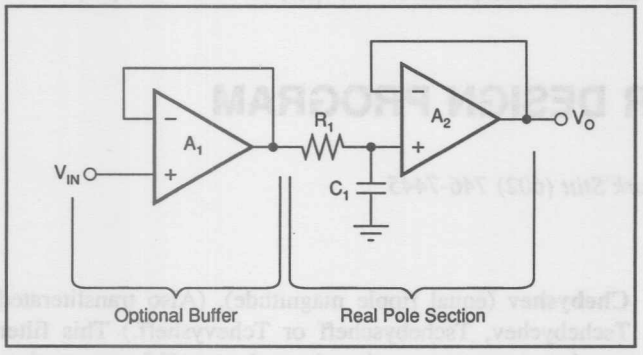

FIGURE 2. Real Pole Section (Unity-Gain, First-Order Butterworth; $f_{-3dB} = 1/2 \cdot \pi \cdot R_1 \cdot C_1$).

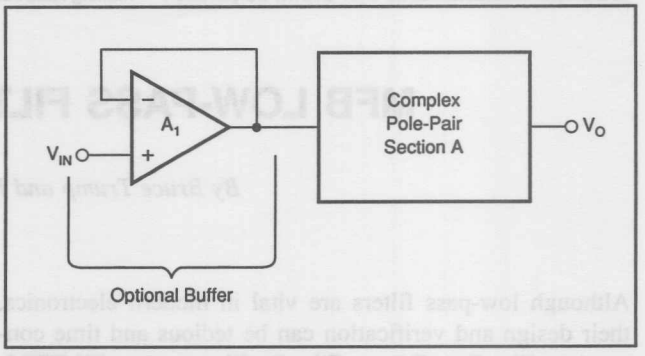

FIGURE 3. Second-Order Low-Pass Filter.

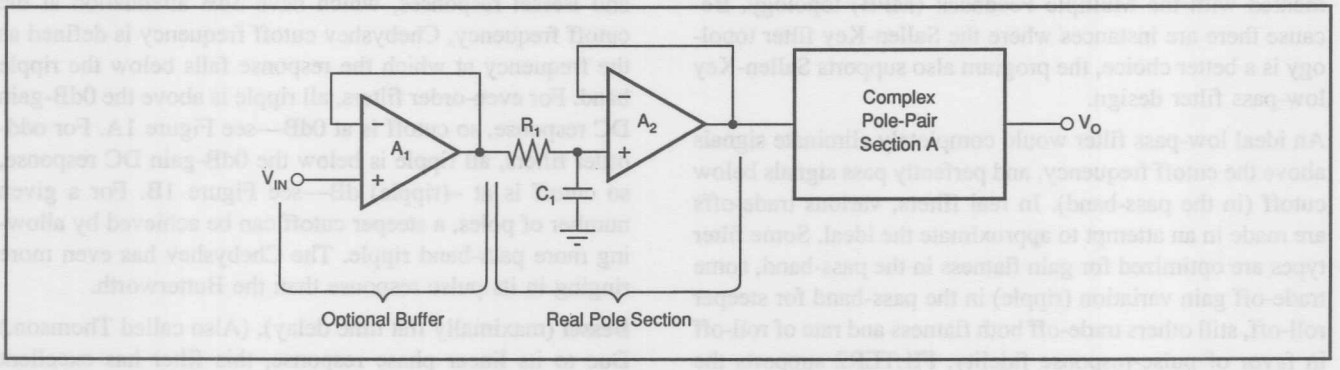

FIGURE 4. Third-Order Low-Pass Filter.

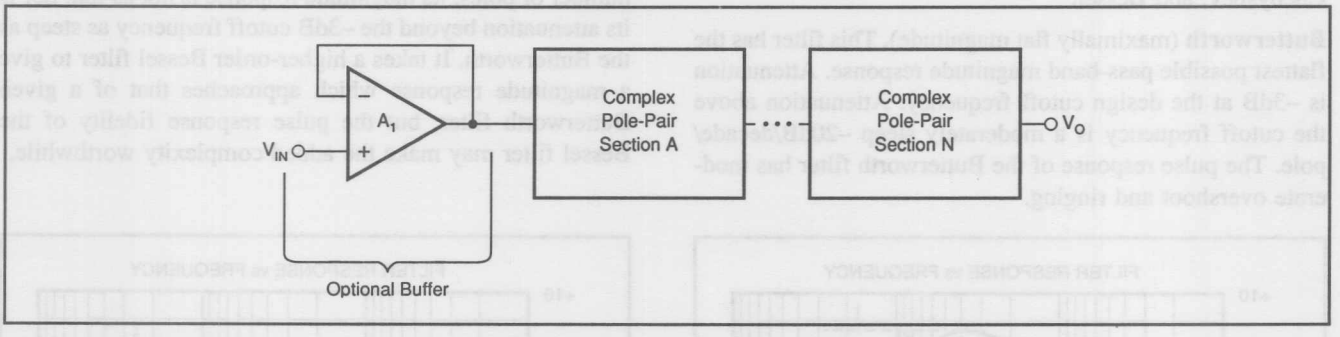

FIGURE 5. Even-Order Low-Pass Filter Using Cascaded Complex Pole-Pair Sections.

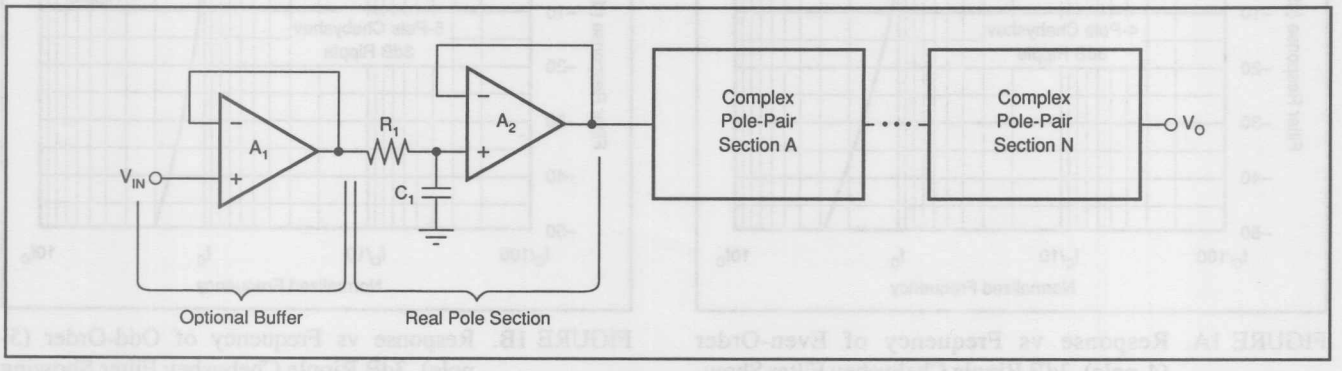

FIGURE 6. Odd-Order Low-Pass Filter Using Cascaded Complex Pole-Pair Sections Plus One Real-Pole Section.

Butterworth

Advantages — Maximally flat magnitude response in the pass-band. Good all-around performance. Pulse response better than Chebyshev. Rate of attenuation better than Bessel.

Disadvantages — Some overshoot and ringing in step response.

Chebyshev

Advantages — Better attenuation beyond the pass-band than Butterworth.

Disadvantages — Ripple in pass-band. Considerable ringing in step response.

Bessel

Advantages — Best step response—very little overshoot or ringing.

Disadvantages — Slower rate of attenuation beyond the pass-band than Butterworth.

CIRCUIT IMPLEMENTATION

Even-order filters designed with this program consist of cascaded sections of complex pole-pairs. Odd-order filters contain an additional real-pole section. Figures 2 through 6 show the recommended cascading arrangement. The program automatically places lower Q stages ahead of higher Q stages to prevent op amp output saturation due to gain peaking. The program can be used to design filters up to 8th order.

FILTER ORDER	FIGURE
1 pole	Figure 2
2 poles	Figure 3
3 poles	Figure 4
4 or more poles (even order)	Figure 5
5 or more poles (odd order)	Figure 6

TABLE I. Filter Circuit vs Filter Order.

COMPLEX POLE-PAIR CIRCUIT

The choice of a complex pole-pair circuit depends on performance requirements. FILTER2 supports the two most commonly used op amp pole-pair circuit topologies:

- Multiple Feedback (MFB)—shown in Figure 7.
- Sallen-Key—shown in Figures 8 and 9.

The MFB topology (sometimes called Infinite Gain or Rauch) is often preferred due to assured low sensitivity to component variations—see sensitivity section. There are instances, however, where the Sallen-Key topology is a better choice.

As a rule of thumb, the Sallen-Key topology is better if:

1) Gain accuracy is important, *AND*
2) A unity-gain filter is used, *AND*
3) Pole-pair Q is low (e.g. Q < 3)

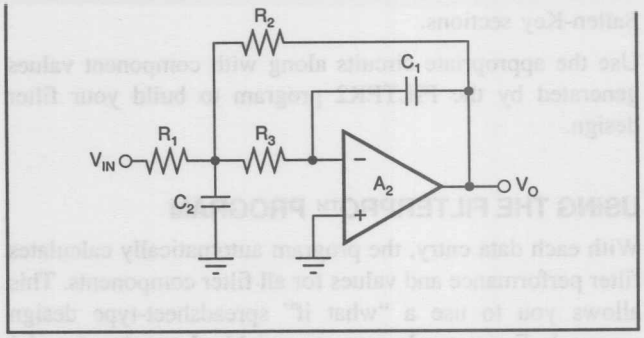

FIGURE 7. MFB Complex Pole-Pair Section. (Gain = $-R_2/R_1$)

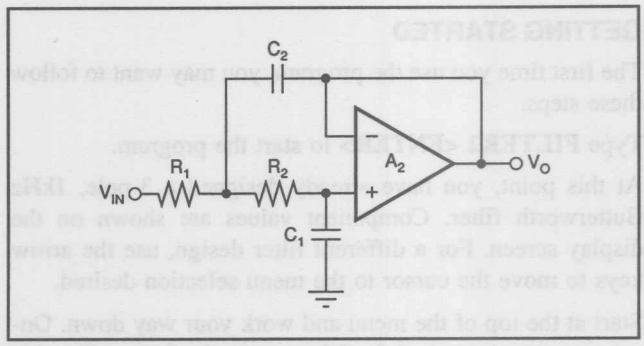

FIGURE 8. Unity-Gain Sallen-Key Complex Pole-Pair Section. (Gain = 1)

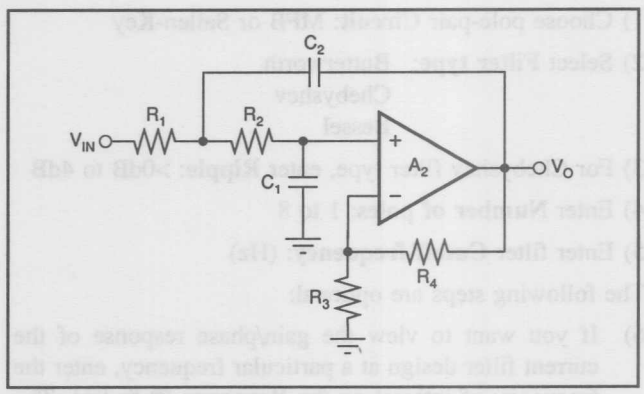

FIGURE 9. Sallen-Key Complex Pole-Pair Section. (Gain = $1 + R_4/R_3$)

At unity-gain, the Sallen-Key topology inherently has excellent gain accuracy. This is because the op amp is used as a unity-gain buffer. With the MFB topology, gain is determined by the R_2/R_1 resistor ratio. The unity-gain Sallen-Key topology also requires fewer components—two resistors vs three for MFB.

The Sallen-Key topology may also be preferable for high-Q high frequency filter sections. In these sections the value required for C_1 in a MFB design can be quite low for reasonable resistor values. Low capacitor values can result in significant errors due to parasitic capacitances.

The best filter design may be a combination of MFB and Sallen-Key sections.

Use the appropriate circuits along with component values generated by the FILTER2 program to build your filter design.

USING THE FILTERPRO™ PROGRAM

With each data entry, the program automatically calculates filter performance and values for all filter components. This allows you to use a "what if" spreadsheet-type design approach. For example, you can quickly determine, by trial and error, how many poles are needed for a given roll-off.

GETTING STARTED

The first time you use the program, you may want to follow these steps.

Type **FILTER2 <ENTER>** to start the program.

At this point, you have already designed a 3-pole, 1kHz Butterworth filter. Component values are shown on the display screen. For a different filter design, use the arrow keys to move the cursor to the menu selection desired.

Start at the top of the menu and work your way down. On-screen prompts, to the left of the menu selections, will guide you in program use. Refer to this bulletin for more detail, if needed.

1) Choose pole-pair **Circuit**: MFB or Sallen-Key
2) Select **Filter type**: Butterworth
   Chebyshev
   Bessel
3) For Chebyshev filter type, enter **Ripple**: >0dB to 4dB
4) Enter **Number of poles**: 1 to 8
5) Enter filter **Cutoff frequency**: (Hz)

The following steps are optional:

6) If you want to view the gain/phase response of the current filter design at a particular frequency, enter the frequency of interest on the **Response @ fx** line. The gain/phase information can be viewed on the **fn, Q, Response** display window—see step 11.
7) If you want to change the resistor scaling, enter a value on the **Scale Resistors** line.
8) If you want to change the gain of a section, press **<ENTER>** on the **Gain Entry** line. Default value for gain is 1.0V/V in each section.
9) If you want to enter your own capacitor values, press **<ENTER>** on the **Capacitor Menu** line.
10) If you want to design with standard 1% resistors instead of exact resistors, press **<ENTER>** on the **Resistors** line.
11) To change the display screen press **<ENTER>** on the **Display** line. Available display screens are: Component values; fn, Q, Response; Sensitivities.

TO RETURN TO DOS

To exit the program and return to DOS, press **<F1>**.

USING THE PLOT FEATURE

A Plot feature allows you to view graphical results of filter gain and phase vs frequency. This feature is useful for comparing filter types.

To view a plot of the current filter design, press **<F2>**.

GRAPHIC DISPLAY COMMANDS

While viewing the graphic display, several commands can be used to compare filter responses:

S—Saves the plot of the current design for future recall.

R—Recalls the Saved plot and plots it along with the current design.

P—Recalls the Previous plot of the last design plotted from the main program (by pressing **<F2>**) and plots it along with the current design. You can recall the Previous design and the Saved design to plot all three together.

C—Clears the display and replots only the current design.

GRAPHIC DISPLAY CURSOR CONTROL

While viewing the graphics display you can also use the left/right *arrow* keys to move a cursor and view gain and phase for plotted filter responses. The gain/phase of the current design is always displayed. In addition, the gain/phase of the Recalled or Previous design can be viewed by pressing **R** or **P**.

TO PRINT RESULTS

To print results press **<F3>**. All three display screens will automatically be printed.

SENSITIVITY

Sensitivity is the measure of the vulnerability of a filter's performance to changes in component values. The important filter parameters to consider are natural frequency (f_n) and Q.

f_n SENSITIVITY FOR BOTH MFB AND SALLEN-KEY

Sensitivity of f_n to resistor, capacitor, and amplifier gain variations is always low for both the Sallen-Key and MFB filter topologies.

$S_R^f = S_C^f = \pm 0.5\%/\%$

$S_K^f = 0$

Where:

S_R^f, S_C^f, S_K^f = Sensitivity of f_n to resistor, capacitor, and gain variations (%/%)

Q SENSITIVITY

For the MFB topology, sensitivities to Q are also always low, but sensitivities for the Sallen-Key topology can be quite high—exceeding $2 \cdot K \cdot Q^2$. At unity gain, the Sallen-Key Q sensitivity to resistor and capacitor variations will always be low. Unfortunately, however, the sensitivity of the unity-gain Sallen-Key pole-pair to op amp gain can be high.

Q Sensitivity for MFB Pole-Pair

$S_C^Q = \pm 0.5\%/\%$

$$S_R^Q = \pm \frac{R_2 - R_3 - K \cdot R_3}{2(R_2 + R_3 + K \cdot R_3)} \quad \text{(MFB complex pole-pair)}$$

$$S_K^Q = \frac{K \cdot R_3}{R_2 + R_3 + K \cdot R_3} \quad \text{(MFB complex pole-pair)}$$

Notice, by inspection: S_R^Q is always less than $\pm 0.5\%/\%$, and S_K^Q is always less than $1.0\%/\%$.

Q Sensitivity for Gain = 1 Sallen-Key Pole-Pair

$S_C^Q = \pm 0.5\%/\%$

$$S_R^Q = \pm \frac{R_1 - R_2}{2(R_1 + R_2)} \quad \text{(Sallen-Key complex pole-pair)}$$

So, S_R^Q is always less than $0.5\%/\%$.

$Q^2 < S_K^Q < 2 \cdot Q^2$ (Sallen-Key complex pole-pair)

Where:

S_R^Q, S_C^Q, S_K^Q = Sensitivity of f and Q to resistor, capacitor, and gain variations (%/%)

K = Op amp gain (V/V)

Figure 7 circuit, $K = R_2/R_1$

Figure 8 circuit, $K = 1.0$

Figure 9 circuit, $K = 1 + R_4/R_3$

NOTE: FilterPro™ always selects component values so unity-gain Sallen-Key S_K^Q will be closer to Q^2 than to $2 \cdot Q^2$.

However, FILTER2 will allow you to design Sallen-Key pole-pairs with high sensitivities (high Qs and GAIN >> 1). You must make sure that sensitivities to component variations do not make these designs impractical. A feature in the **Display** menu allows you to view the f_n and Q sensitivity of filter sections to resistor and capacitor variations.

USING THE SENSITIVITY DISPLAY FEATURE

To use the **Sensitivity** display option, move the cursor to the **Display** menu, press **<ENTER>**, move the cursor to the **Sensitivity** selection, and press **<ENTER>** again. The display shows sensitivity of f_n and Q to each component for each filter section. The format is S^f; S^Q.

Rather than displaying the derivative with respect to component variations, the program calculates f_n and Q change for a 1% change in component values. This gives a more realistic sensitivity value for real-world variations.

USING THE SCALE RESISTORS MENU OPTION

The **Scale Resistors** option allows you to scale the computer-selected resistor values to match the application. Move the cursor to the **Scale Resistors** menu selection and enter your *seed* resistor value. The default value of 10kΩ is suggested for most applications.

Higher resistor values, e.g. 100kΩ, can be used with FET-input op amps. At temperatures below about 70°C, DC errors and excess noise due to op amp input bias current will be small. Remember, however, that noise due to the resistors will be increased by $\sqrt{n}$ where n is the resistor increase multiplier.

Lower resistor values, e.g. 500Ω, are a better match for high-frequency filters using the OPA620 or OPA621 op amps.

CAPACITOR VALUES

Compared to resistors, capacitors with tight tolerances are more difficult to obtain and can be much more expensive. The **Capacitor** menu option allows you to enter actual measured capacitor values. In this way, an accurate filter response can be achieved with relatively inexpensive components.

USING THE CAPACITOR MENU OPTION

To use the **Capacitor** menu option, move the cursor to the **Capacitor** menu selection and press **<ENTER>**. Move the cursor to any capacitor and enter your value. Prompts on the left of the screen advise min/max capacitor entry limits. With each capacitor entry, the program will select exact or closest standard 1% resistor values as before.

COMPENSATE FOR OP AMP INPUT CAPACITANCE—SALLEN-KEY ONLY

If the common-mode input capacitance of the op amp used in a Sallen-Key filter section is more than approximately $C_1/400$ (0.25% of C_1), it must be considered for accurate filter response. You can use the **Capacitor** menu option to compensate for op amp input capacitance by simply adding the value of the op amp common-mode input capacitance to the actual value of C_1. The program then automatically

recalculates the exact or closest 1% resistor values for accurate filter response. No compensation for op amp input capacitance is required with MFB designs.

CAPACITOR SELECTION

Capacitor selection is very important for a high-performance filter. Capacitor behavior can vary significantly from ideal, introducing series resistance and inductance which limit Q. Also, nonlinearity of capacitance vs voltage causes distortion.

Common ceramic capacitors with high dielectric constants, such as "high-K" types, can cause errors in filter circuits. Recommended capacitor types are: NPO ceramic, silver mica, metallized polycarbonate; and, for temperatures up to 85°C, polypropylene or polystyrene.

OP AMP SELECTION

It is important to choose an op amp that can provide the necessary DC precision, noise, distortion, and speed.

OP AMP BANDWIDTH

In a low-pass filter section, maximum gain peaking is very nearly equal to Q at f_n (the section's natural frequency). So, as a rule of thumb:

For an MFB section: Op amp bandwidth should be at least $100 \cdot \text{GAIN} \cdot f_n$.

High-Q Sallen-Key sections require higher op amp bandwidth.

For a Sallen-Key section: For $Q > 1$, op amp gain-bandwidth should be at least $100 \cdot \text{GAIN} \cdot Q^3 \cdot f_n$.
For $Q \leq 1$, op amp gain-bandwidth should be at least $100 \cdot \text{GAIN} \cdot f_n$.

For a real-pole section: Op amp bandwidth should be at least $50 \cdot f_n$.

Although Q is formally defined only for complex poles, it is convenient to use a Q of 0.5 for calculating the op amp gain required in a real-pole section.

For example, a unity-gain 20kHz 5-pole, 3dB ripple Chebyshev MFB filter with a 2nd pole-pair f_n of 19.35kHz and a Q of 8.82 needs an op amp with unity gain bandwidth of at least 17MHz. On the other hand, a 5-pole Butterworth MFB filter, with a worst case Q of 1.62 needs only a 3.2MHz op amp. The same 5-pole Butterworth filter implemented with a Sallen-Key topology would require a 8.5MHz op amp in the high-Q section.

USING THE f_n AND Q DISPLAY OPTION

To aid in selection of the op amp, a feature in the **Display** menu section allows you to view pole-pair section f_n and Q.

To use this feature move the cursor to the **Display** menu, press **<ENTER>**, move the cursor to the **f_n & Q** selection, and press **<ENTER>** again. The f_n and Q information is also useful when trouble-shooting filters by comparing expected to actual response of individual filter sections.

OP AMP SLEW RATE

For adequate full-power response, the slew rate of the op amp must be greater than $\pi \cdot V_O p\text{-}p \cdot$ FILTER BANDWIDTH. For example, a 100kHz filter with 20Vp-p output requires an op amp slew rate of at least 6.3V/µs. Burr-Brown offers an excellent selection of op amps which can be used for high performance active filters. The guide on P-7 lists some good choices.

THE UAF42 UNIVERSAL ACTIVE FILTER

For other filter designs, consider the Burr-Brown UAF42 Universal Active Filter. It can easily be configured for a wide variety of low-pass, high-pass, band-pass, or band-reject (notch) filters. It uses the classical state-variable architecture with an inverting amplifier and two integrators to form a pole-pair. The integrators include on-chip 1000pF, ±0.5% capacitors. This solves one of the most difficult problems in active filter implementation—obtaining tight tolerance, low-loss capacitors at reasonable cost.

Simple design procedures for the UAF42 allow implementation of Butterworth, Chebyshev, Bessel, and other types of filters. An extra FET-input op amp in the UAF42 can be used to form additional stages or special filter types such as Inverse Chebyshev. The UAF42 is available in a standard 14-pin DIP. For more information, request the Burr-Brown Product Data Sheet PDS-1070 and Application Bulletin AB-035.

EXAMPLES OF MEASURED MFB FILTER RESPONSE

Figures 10 and 11 show actual measured magnitude response plots for 5th-order 20kHz Butterworth, 3dB Chebyshev and Bessel filters designed with the program. The op amp used in all filters was the OPA627. As can be seen in Figure 10, the initial roll-off of the Chebyshev filter is fastest and the roll-off of the Bessel filter is the slowest. However, each of the 5th-order filters ultimately rolls off at $-N \cdot 20$dB/decade, where N is the filter order (–100dB/decade for a 5-pole filter).

The oscilloscope photographs (Figures 12-14) show the step response for each filter. As expected, the Chebyshev filter has the most ringing, while the Bessel has the least. Figure 15 shows distortion plots vs frequency for the three filters.

See Application Bulletin AB-017 for measured Sallen-Key filter performance of the same three designs.

T_A = 25°C, V_S = ±15V, specifications typ, unless otherwise noted, min/max specifications are for high-grade model.

OP AMP MODEL	BW typ (MHz)	FPR [1] typ (kHz)	SR typ (V/μs)	V_{OS} max (μV)	V_{OS}/dT max (μV/°C)	NOISE at 10kHz (nV/√Hz)	C_{CM} [3] (pF)
OPA177	0.6	3	0.2	10	±0.1	8	1
OPA27	8	30	1.9	25	±0.6	2.7	1
OPA2107 dual [2]	4.5	280	18	500	±5	8	4
OPA602 [2]	6	500	35	250	±2	12	3
OPA404 quad [2]	6	500	35	1000	±3 typ	12	3
OPA627 [2]	16	875	55	100	±0.8	4.5	7
OPA620 (V_S = ±5V)	300	16MHz(5Vp-p)	250	500	±8 typ	2.3 @ 1MHz	1

NOTES: (1) Unless otherwise noted, FPR is full power response at 20Vp-p as calculated from slew rate. (2) These op amps have FET inputs. (3) Common-mode input capacitance.

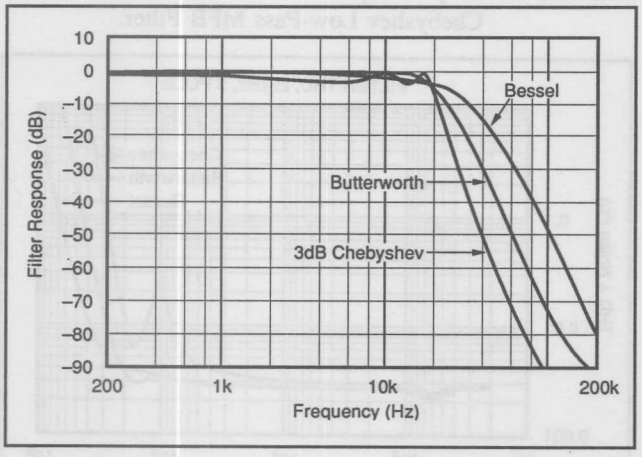

FIGURE 10. Gain vs Frequency for Fifth-Order 20kHz Butterworth, Chebyshev, and Bessel Unity-Gain MFB Low-Pass Filters, Showing Overall Filter Response.

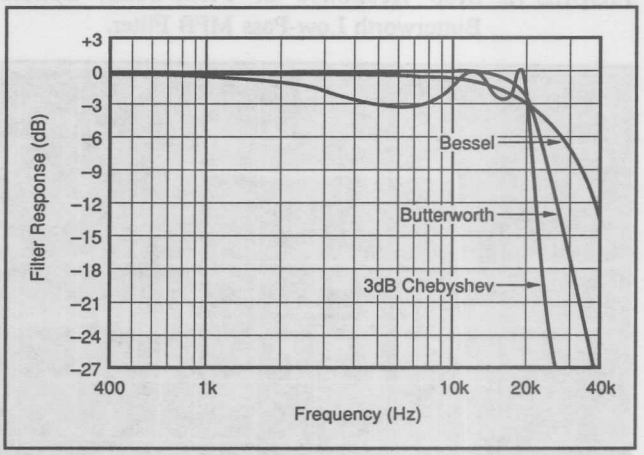

FIGURE 11. Gain vs Frequency for Fifth-Order 20kHz Butterworth, Chebyshev, and Bessel Unity-Gain MFB Low-Pass Filters, Showing Transition-Band Detail.

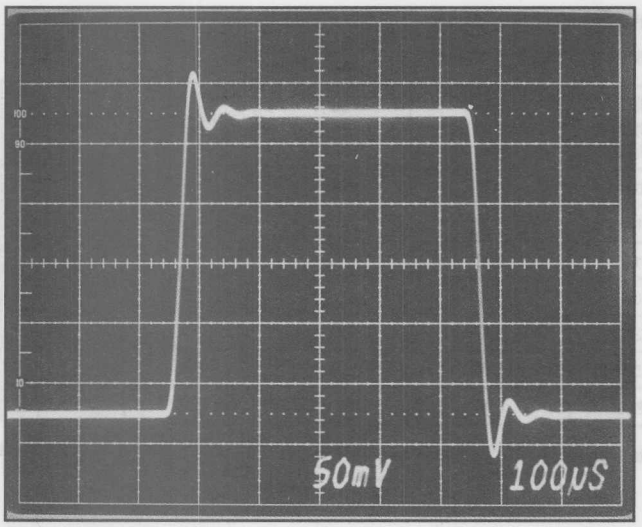

FIGURE 12. Step Response of Fifth-Order 20kHz Butterworth Low-Pass MFB Filter.

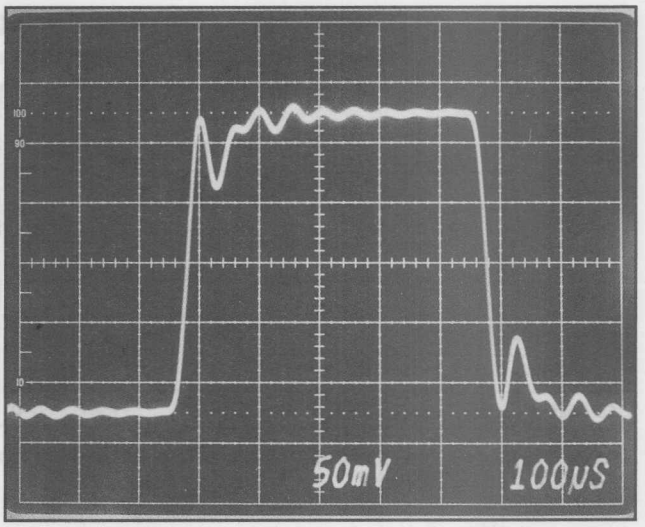

FIGURE 13. Step Response of Fifth-Order 20kHz Chebyshev Low-Pass MFB Filter.

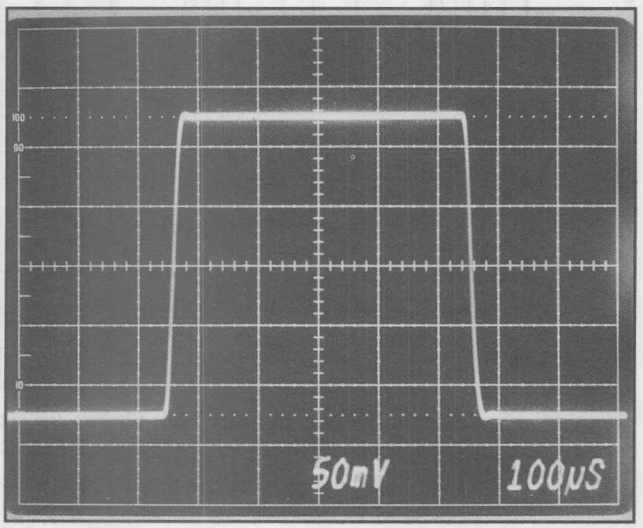

FIGURE 14. Step Response of Fifth-Order 20kHz Bessel Low-Pass MFB Filter.

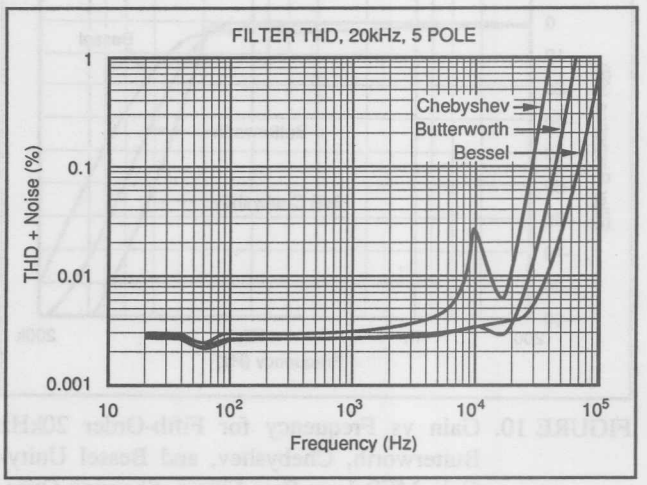

FIGURE 15. Measured Distortion for the Three 20kHz MFB Low-Pass Filters.

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FILTER DESIGN PROGRAM FOR THE UAF42 UNIVERSAL ACTIVE FILTER

By Johnnie Molina and R. Mark Stitt (602) 746-7592

Although active filters are vital in modern electronics, their design and verification can be tedious and time consuming. To aid in the design of active filters, Burr-Brown provides a series of FilterPro™ computer-aided design programs. Using the FILTER42 program and the UAF42 it is easy to design and implement all kinds of active filters. The UAF42 is a monolithic IC which contains the op amps, matched resistors, and precision capacitors needed for a state-variable filter pole-pair. A fourth, uncommitted precision op amp is also included on the die.

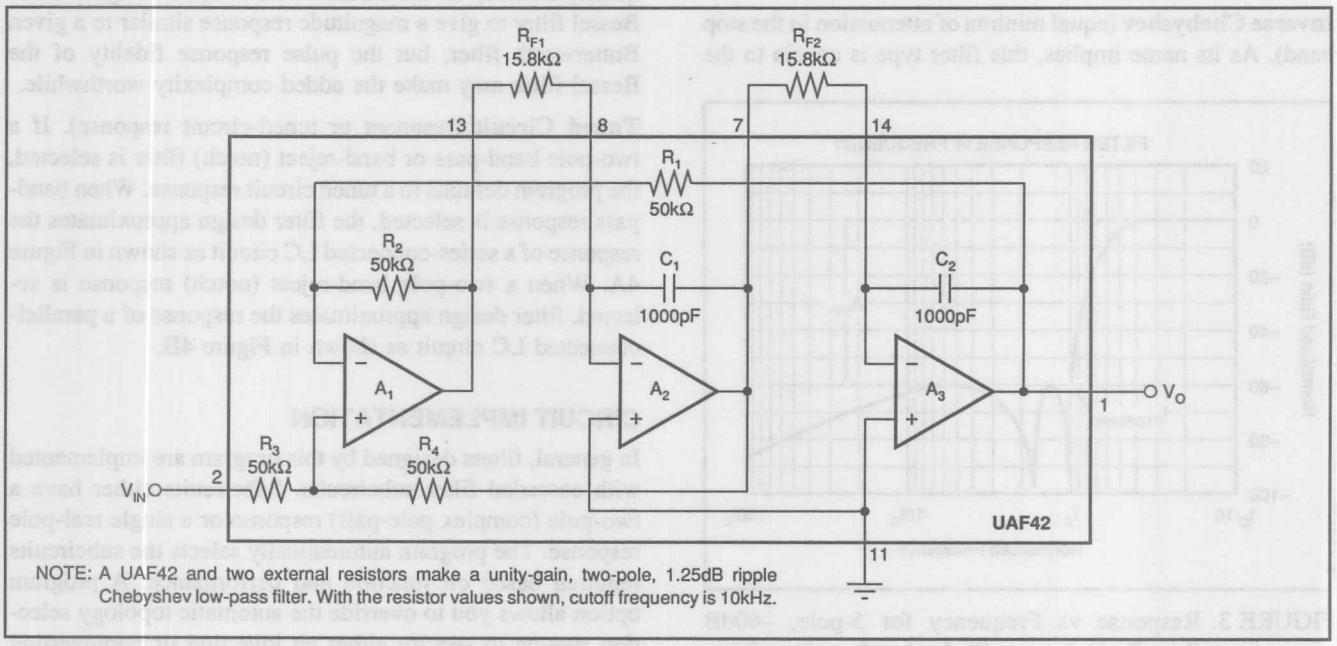
Filters implemented with the UAF42 are time-continuous, free from the switching noise and aliasing problems of switched-capacitor filters. Other advantages of the state-variable topology include low sensitivity of filter parameters to external component values and simultaneous low-pass, high-pass, and band-pass outputs. Simple two-pole filters can be made with a UAF42 and two external resistors—see Figure 1.

The DOS-compatible program guides you through the design process and automatically calculates component values. Low-pass, high-pass, band-pass, and band-reject (or notch) filters can be designed.

Active filters are designed to approximate an ideal filter response. For example, an ideal low-pass filter completely eliminates signals above the cutoff frequency (in the stop-band), and perfectly passes signals below it (in the pass-band). In real filters, various trade-offs are made in an attempt to approximate the ideal. Some filter types are optimized for gain flatness in the pass-band, some trade-off gain variation or ripple in the pass-band for a steeper rate of attenuation between the pass-band and stop-band (in the transition-band), still others trade-off both flatness and rate of roll-off in favor of pulse-response fidelity. FILTER42 supports the three most commonly used all-pole filter types: Butterworth, Chebyshev, and Bessel. The less familiar Inverse Chebyshev is also supported. If a two-pole band-pass or notch filter is selected, the program defaults to a resonant-circuit response.

Butterworth (maximally flat magnitude). This filter has the flattest possible pass-band magnitude response. Attenuation is –3dB at the design cutoff frequency. Attenuation beyond the cutoff frequency is a moderately steep –20dB/decade/pole. The pulse response of the Butterworth filter has moderate overshoot and ringing.

Chebyshev (equal ripple magnitude). (Other transliterations of the Russian Чебышев are Tschebychev, Tschebyscheff or Tchevysheff). This filter response has steeper initial rate of attenuation beyond the cutoff frequency than Butterworth.



NOTE: A UAF42 and two external resistors make a unity-gain, two-pole, 1.25dB ripple Chebyshev low-pass filter. With the resistor values shown, cutoff frequency is 10kHz.

FIGURE 1. Two-Pole Low-Pass Filter Using UAF42.

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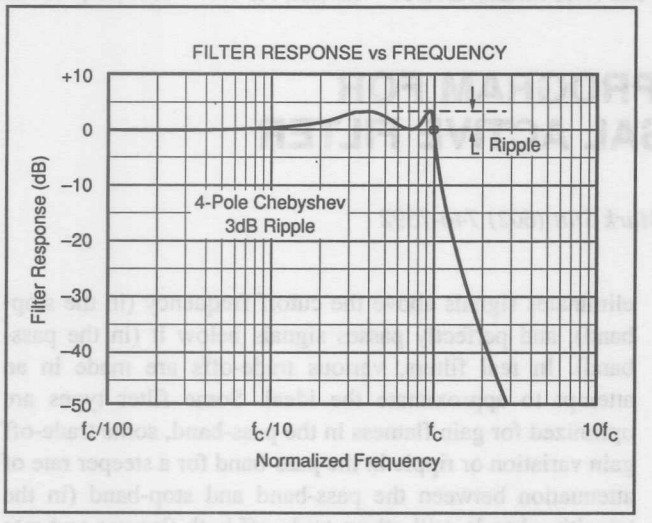


FIGURE 2A. Response vs Frequency for Even-Order (4-pole) 3dB Ripple Chebyshev Low-Pass Filter Showing Cutoff at 0dB.

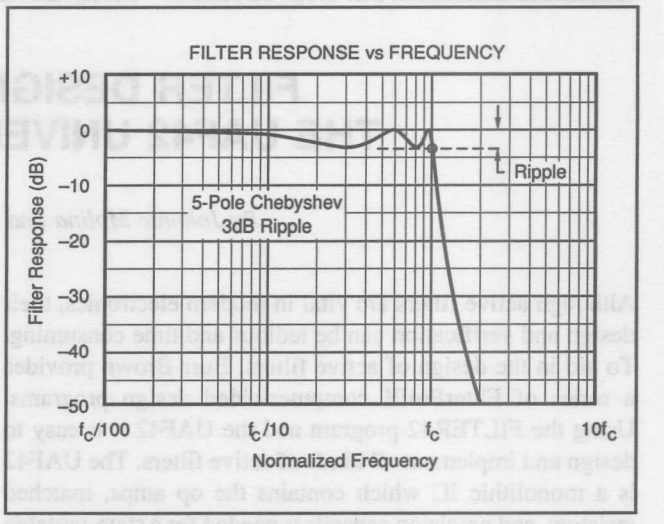


FIGURE 2B. Response vs Frequency for Odd-Order (5-pole) 3dB Ripple Chebyshev Low-Pass Filter Showing Cutoff at –3dB.

This advantage comes at the penalty of amplitude variation (ripple) in the pass-band. Unlike Butterworth and Bessel responses, which have 3dB attenuation at the cutoff frequency, Chebyshev cutoff frequency is defined as the frequency at which the response falls below the ripple band. For even-order filters, all ripple is above the 0dB-normalized passband gain response, so cutoff is at 0dB (see Figure 2A). For odd-order filters, all ripple is below the 0dB-normalized passband gain response, so cutoff is at –(ripple) dB (see Figure 2B). For a given number of poles, a steeper cutoff can be achieved by allowing more pass-band ripple. The Chebyshev has more ringing in its pulse response than the Butterworth—especially for high-ripple designs.

Inverse Chebyshev (equal minima of attenuation in the stop band). As its name implies, this filter type is cousin to the Chebyshev. The difference is that the ripple of the Inverse Chebyshev filter is confined to the stop-band. This filter type has a steep rate of roll-off and a flat magnitude response in the pass-band. Cutoff of the Inverse Chebyshev is defined as the frequency where the response first enters the specified stop-band—see Figure 3. Step response of the Inverse Chebyshev is similar to the Butterworth.

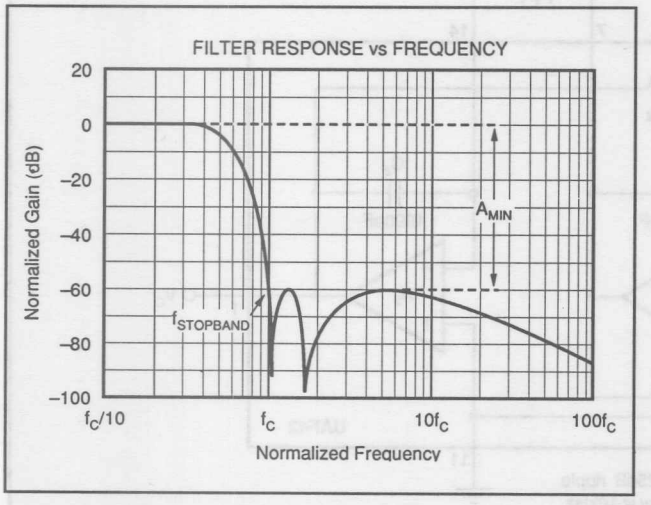


FIGURE 3. Response vs Frequency for 5-pole, –60dB Stop-Band, Inverse Chebyshev Low-Pass Filter Showing Cutoff at –60dB.

Bessel (maximally flat time delay), also called Thomson. Due to its linear phase response, this filter has excellent pulse response (minimal overshoot and ringing). For a given number of poles, its magnitude response is not as flat, nor is its initial rate of attenuation beyond the –3dB cutoff frequency as steep as the Butterworth. It takes a higher-order Bessel filter to give a magnitude response similar to a given Butterworth filter, but the pulse response fidelity of the Bessel filter may make the added complexity worthwhile.

Tuned Circuit (resonant or tuned-circuit response). If a two-pole band-pass or band-reject (notch) filter is selected, the program defaults to a tuned circuit response. When band-pass response is selected, the filter design approximates the response of a series-connected LC circuit as shown in Figure 4A. When a two-pole band-reject (notch) response is selected, filter design approximates the response of a parallel-connected LC circuit as shown in Figure 4B.

CIRCUIT IMPLEMENTATION

In general, filters designed by this program are implemented with cascaded filter subcircuits. Subcircuits either have a two-pole (complex pole-pair) response or a single real-pole response. The program automatically selects the subcircuits required based on function and performance. A program option allows you to override the automatic topology selection routine to specify either an inverting or noninverting pole-pair configuration.

subcircuit as shown in Figure 5. More complex filters consist of two or more cascaded subcircuits as shown in Figure 6. Even-order filters are implemented entirely with UAF42 pole-pair sections and normally require no external capacitors. Odd-order filters additionally require one real pole section which can be implemented with the fourth uncommitted op amp in the UAF42, an external resistor, and an external capacitor. The program can be used to design filters up to tenth order.

The program guides you through the filter design and generates component values and a block diagram describing the filter circuit. The *Filter Block Diagram* program output shows the subcircuits needed to implement the filter design labeled by type and connected in the recommended order. The *Filter Component Values* program output shows the values of all external components needed to implement the filter.

SUMMARY OF FILTER TYPES

Butterworth

Advantages: Maximally flat magnitude response in the pass-band.
Good all-around performance.
Pulse response better than Chebyshev.
Rate of attenuation better than Bessel.

Disadvantages: Some overshoot and ringing in step response.

Chebyshev

Advantages: Better attenuation beyond the pass-band than Butterworth.

Disadvantages: Ripple in pass-band.
Considerably more ringing in step response than Butterworth.

Inverse Chebyshev

Advantages: Flat magnitude response in pass-band with steep rate of attenuation in transition-band.

Disadvantages: Ripple in stop-band.
Some overshoot and ringing in step response.

Bessel

Advantages: Best step response—very little overshoot or ringing.

Disadvantages: Slower initial rate of attenuation beyond the pass-band than Butterworth.

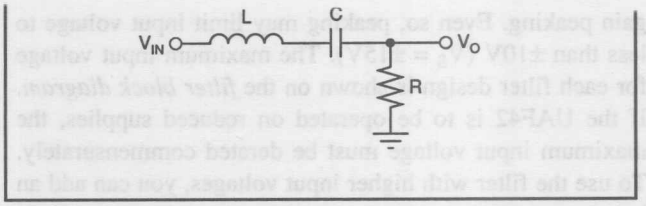


FIGURE 4A. n = 2 Band-Pass Filter Using UAF42 (approximates the response of a series-connected tuned L, C, R circuit).

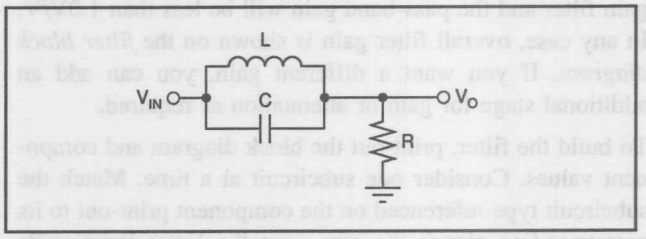


FIGURE 4B. n = 2 Band-Reject (Notch) Filter Using UAF42 (approximates the response of a parallel-connected tuned L, C, R circuit).

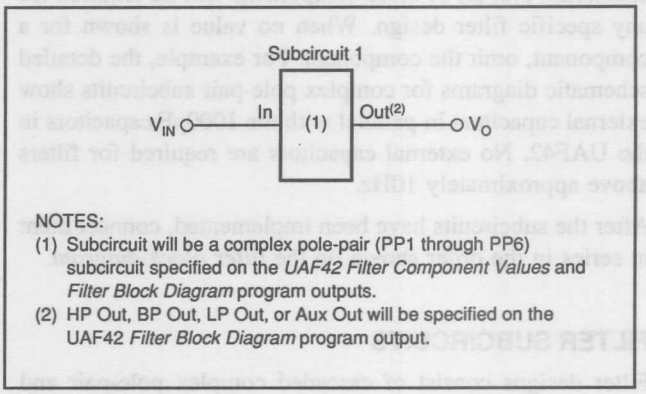


FIGURE 5. Simple Filter Made with Single Complex Pole-Pair Subcircuit.

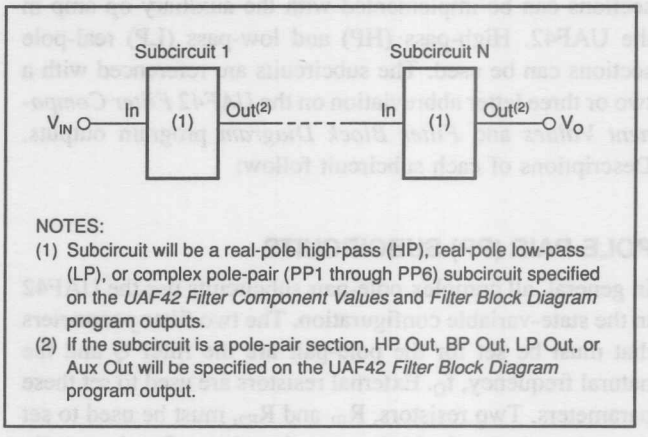


FIGURE 6. Multiple-Stage Filter Made with Two or More Subcircuits.

The program automatically places lower Q stages ahead of higher Q stages to prevent op amp output saturation due to gain peaking. Even so, peaking may limit input voltage to less than ±10V (V_S = ±15V). The maximum input voltage for each filter design is shown on the *filter block diagram.* If the UAF42 is to be operated on reduced supplies, the maximum input voltage must be derated commensurately. To use the filter with higher input voltages, you can add an input attenuator.

The program designs the simplest filter that provides the desired AC transfer function with a pass-band gain of 1.0V/V. In some cases the program cannot make a unity-gain filter and the pass-band gain will be less than 1.0V/V. In any case, overall filter gain is shown on the *filter block diagram.* If you want a different gain, you can add an additional stage for gain or attenuation as required.

To build the filter, print-out the block diagram and component values. Consider one subcircuit at a time. Match the subcircuit type referenced on the component print-out to its corresponding circuit diagram—see the Filter Subcircuits section of this bulletin.

The *UAF42 Filter Component Values* print-out has places to display every possible external component needed for any subcircuit. Not all of these components will be required for any specific filter design. When no value is shown for a component, omit the component. For example, the detailed schematic diagrams for complex pole-pair subcircuits show external capacitors in parallel with the 1000pF capacitors in the UAF42. No external capacitors are required for filters above approximately 10Hz.

After the subcircuits have been implemented, connect them in series in the order shown on the *filter block diagram.*

FILTER SUBCIRCUITS

Filter designs consist of cascaded complex pole-pair and real-pole subcircuits. Complex pole pair subcircuits are based on the UAF42 state-variable filter topology. Six variations of this circuit can be used, PP1 through PP6. Real pole sections can be implemented with the auxiliary op amp in the UAF42. High-pass (HP) and low-pass (LP) real-pole sections can be used. The subcircuits are referenced with a two or three letter abbreviation on the *UAF42 Filter Component Values* and *Filter Block Diagram* program outputs. Descriptions of each subcircuit follow:

POLE-PAIR (PP) SUBCIRCUITS

In general, all complex pole-pair subcircuits use the UAF42 in the state-variable configuration. The two filter parameters that must be set for the pole-pair are the filter Q and the natural frequency, f_O. External resistors are used to set these parameters. Two resistors, R_{F1} and R_{F2}, must be used to set the pole-pair f_O. A third external resistor, R_Q, is usually needed to set Q.

At low frequencies, the value required for the frequency-setting resistors can be excessive. Resistor values above about 5MΩ can react with parasitic capacitance causing poor filter performance. When f_O is below 10Hz, external capacitors must be added to keep the value of R_{F1} and R_{F2} below 5MΩ. When f_O is in the range of about 10Hz to 32Hz, An external 5.49kΩ resistor, R_{2A}, is added in parallel with the internal resistor, R_2, to reduce R_{F1} and R_{F2} by $\sqrt{10}$ and eliminate the need for external capacitors. At the other extreme, when f_O is above 10kHz, R_{2A}, is added in parallel with R_2 to improve stability.

External filter gain-set resistors, R_G, are always required when using an inverting pole-pair configuration or when using a noninverting configuration with Q < 0.57.

PP1 (Noninverting pole-pair subcircuit using internal gain-set resistor, R_3)—See Figure 7. In the automatic topology selection mode, this configuration is used for all band-pass filter responses. This configuration allows the combination of unity pass-band gain and high Q (up to 400). Since no external gain-set resistor is required, external parts count is minimized.

PP2 (Noninverting pole-pair subcircuit using an external gain-set resistor, R_G)—See Figure 8. This configuration is used when the pole-pair Q is less than 0.57.

PP3 (Inverting pole-pair subcircuit)—See Figure 9A. In the automatic topology selection mode, this configuration is used for the all-pole low-pass and high-pass filter responses. This configuration requires an external gain-set resistor, R_G. With R_G = 50kΩ, low-pass and high-pass gain are unity.

PP4 (Noninverting pole-pair/zero subcircuit)—See Figure 10. In addition to a complex pole-pair, this configuration produces a jω-axis zero (response null) by summing the low-pass and high-pass outputs using the auxiliary op amp, A_4, in the UAF42. In the automatic topology selection mode, this configuration is used for all band-reject (notch) filter responses and Inverse Chebyshev filter types when Q > 0.57. This subcircuit option keeps external parts count low by using the internal gain-set resistor, R_3.

PP5 (Noninverting pole-pair/zero subcircuit)—See Figure 11. In addition to a complex pole-pair, this configuration produces a jω-axis zero (response null) by summing the low-pass and high-pass outputs using the auxiliary op amp, A_4, in the UAF42. In the automatic topology selection mode, this configuration is used for all band-reject (notch) filter responses and Inverse Chebyshev filter types when Q < 0.57. This subcircuit option requires an external gain-set resistor, R_G.

PP6 (Inverting pole-pair/zero subcircuit)—See Figure 12. In addition to a complex pole-pair, this configuration produces a jω-axis zero (response null) by summing the low-pass and high-pass outputs using the auxiliary op amp, A_4, in the UAF42. This subcircuit is only used when you override the automatic topology selection algorithm and specify the inverting pole-pair topology. Then it is used for all band-reject (notch) filter responses and Inverse Chebyshev filter types.

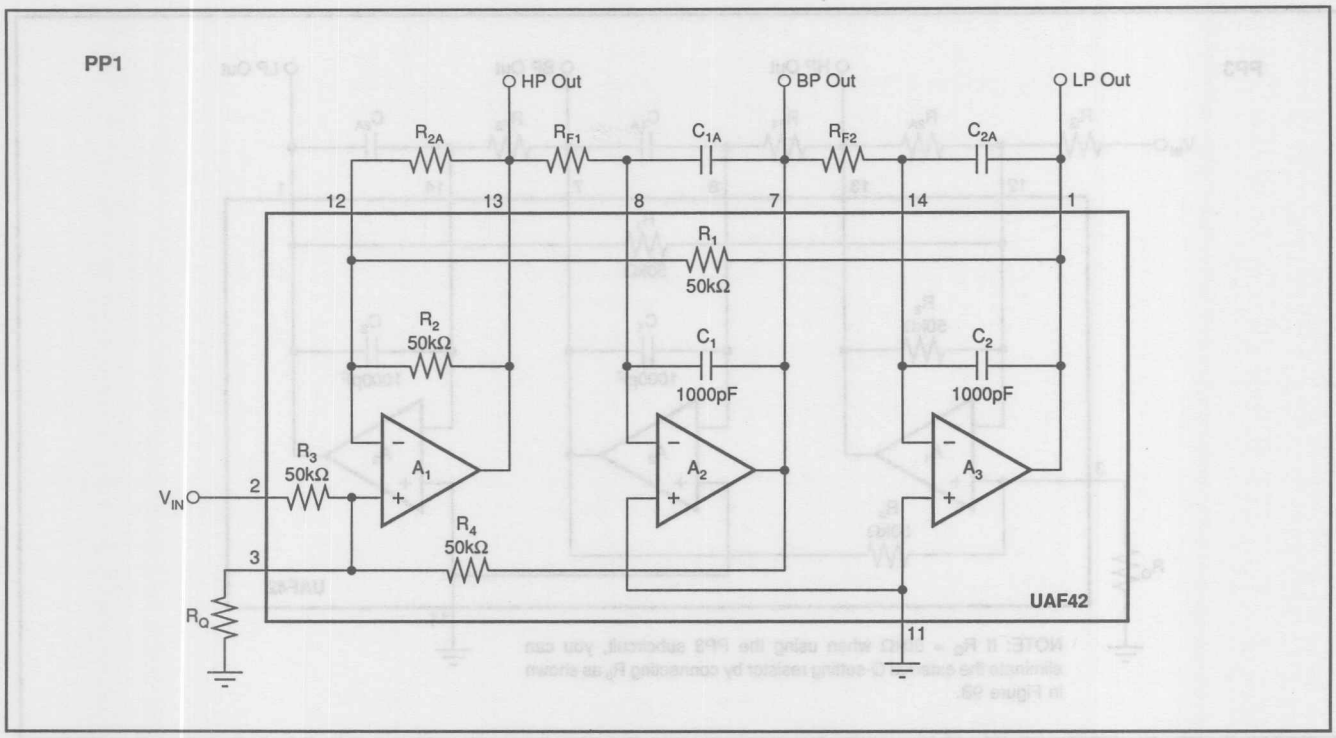


FIGURE 7. PP1 Noninverting Pole-Pair Subcircuit Using Internal Gain-Set Resistor R_3.

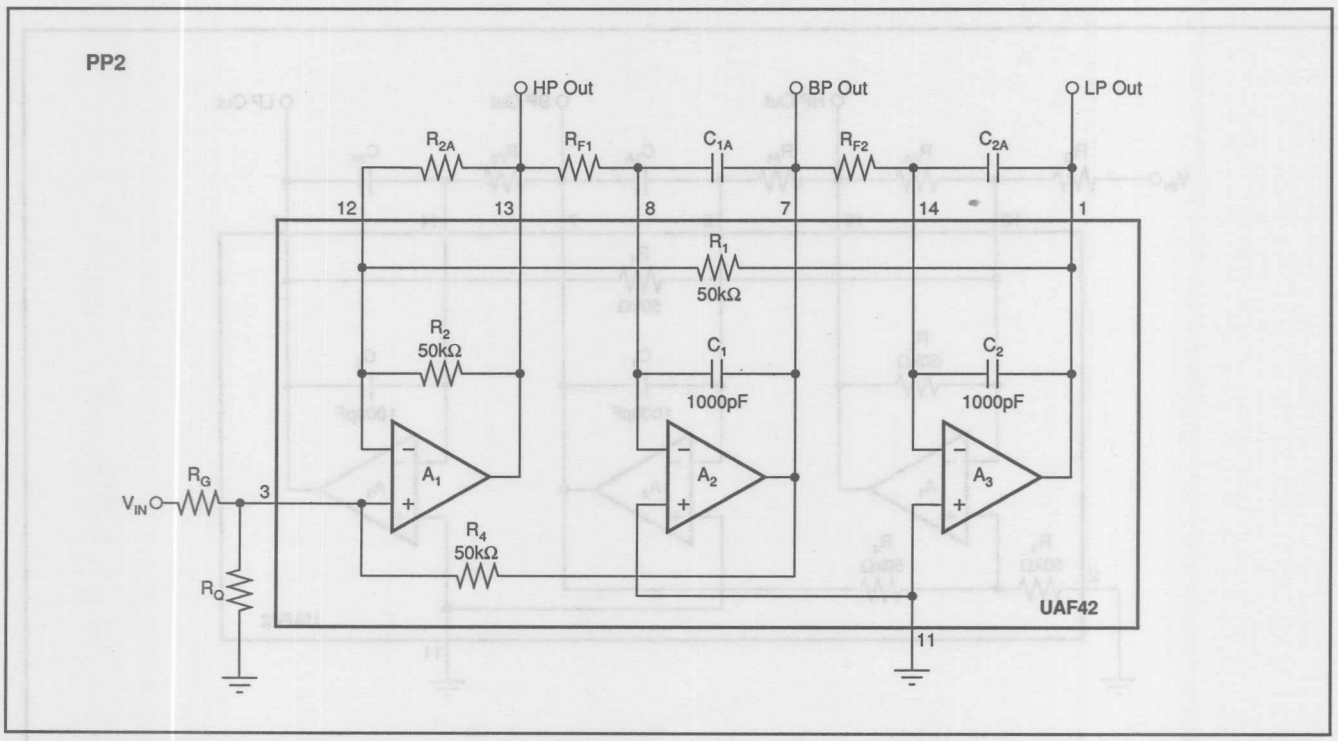


FIGURE 8. PP2 Noninverting Pole-Pair Subcircuit Using External Gain-Set Resistor R_G.

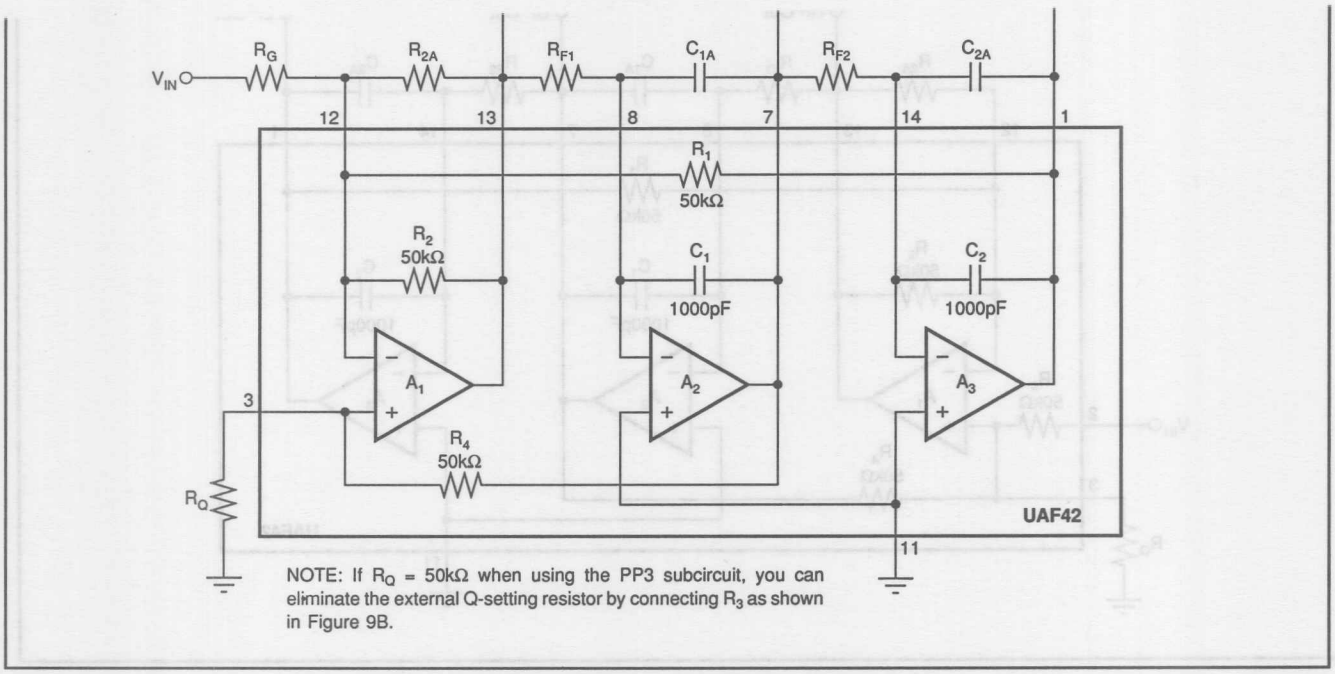


FIGURE 9A. PP3 Inverting Pole-Pair Subcircuit.

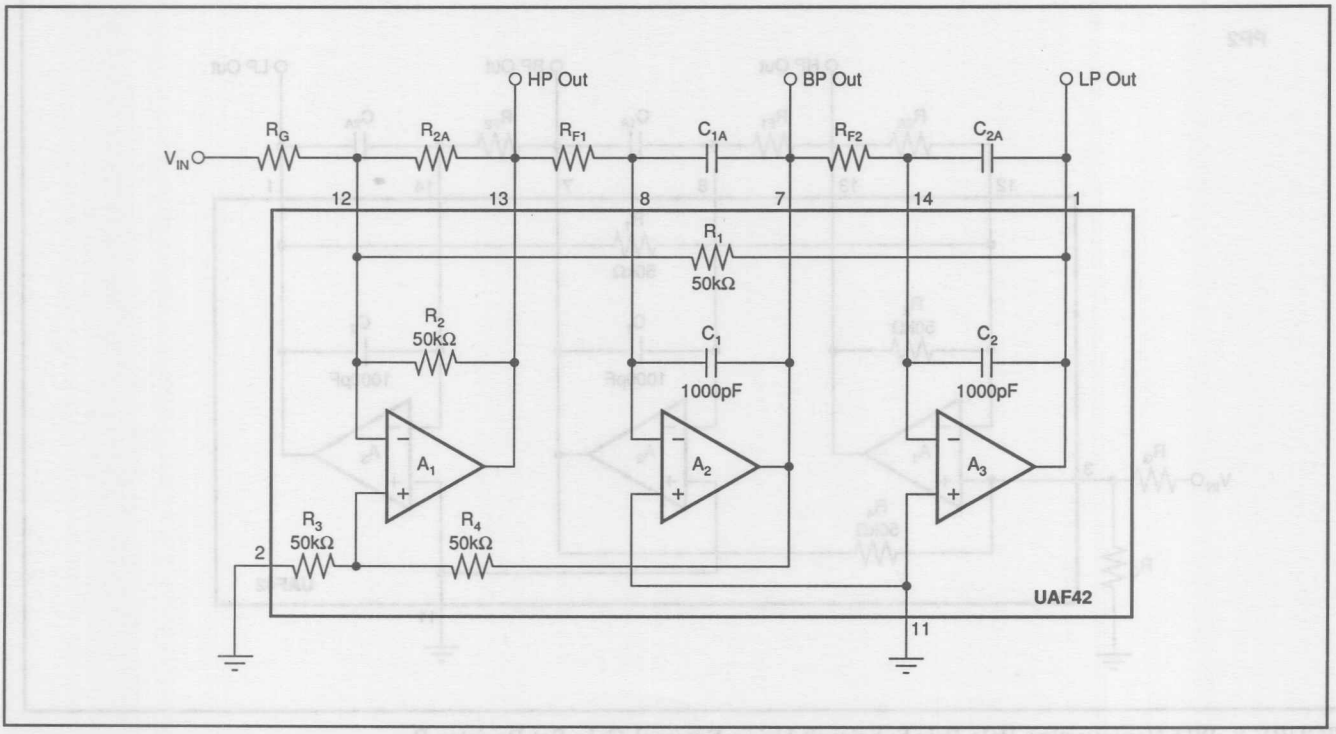


FIGURE 9B. Inverting Pole-Pair Subcircuit Using R_3 to Eliminate External Q-Setting Resistor R_G.

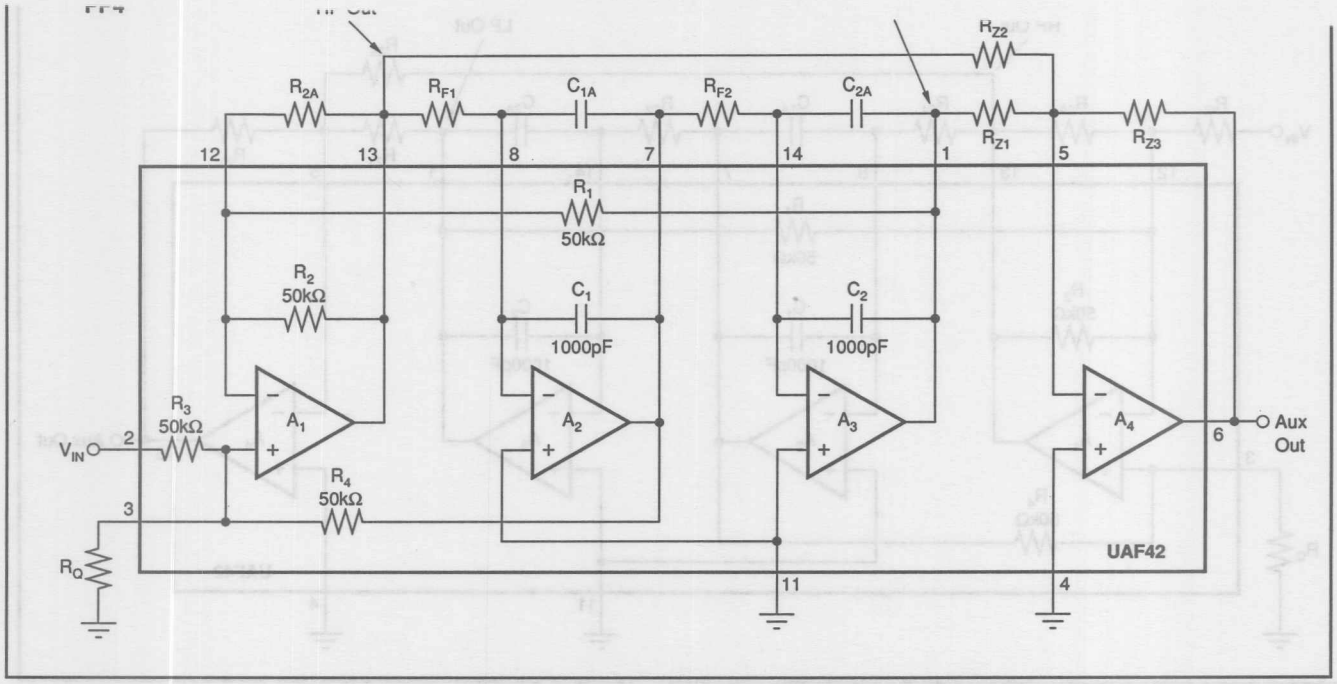


FIGURE 10. PP4 Noninverting Pole-Pair/Zero Subcircuit Using Internal Gain-Set Resistor R_3.

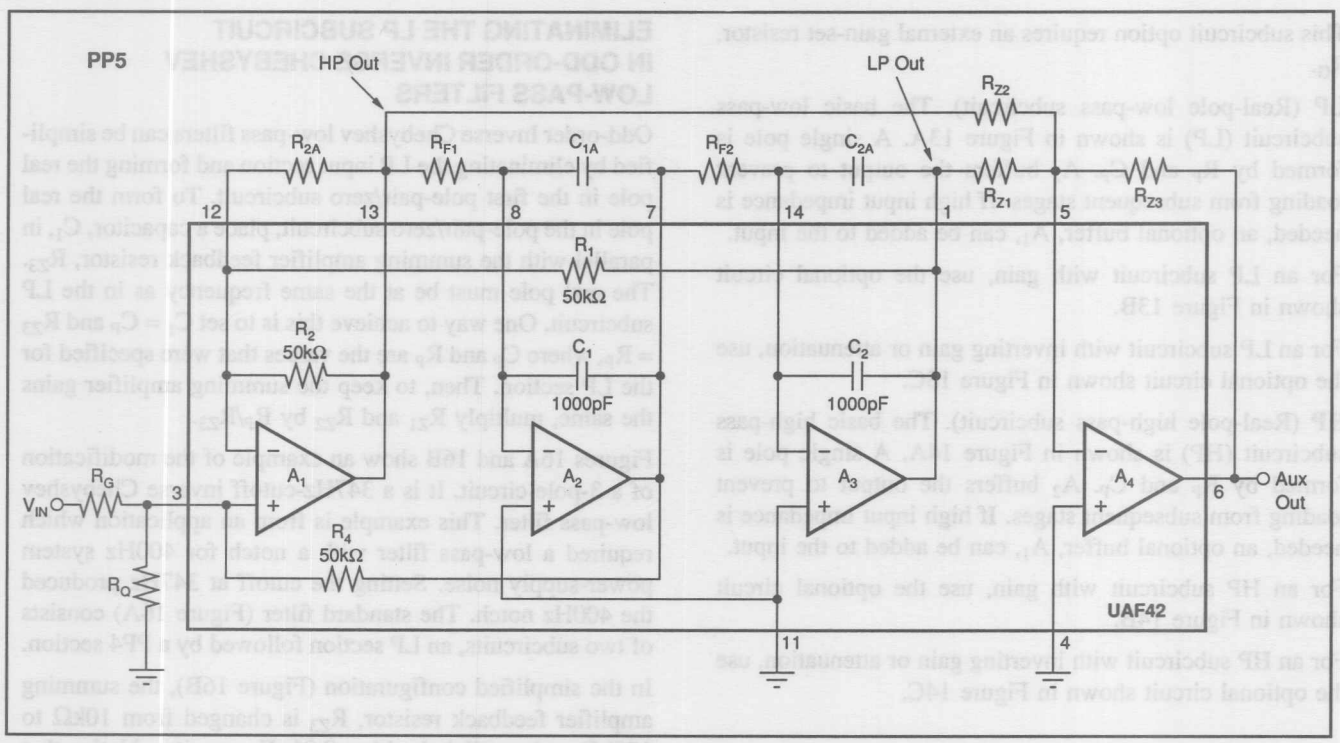


FIGURE 11. PP5 Noninverting Pole-Pair/Zero Subcircuit Using External Gain-Set Resistor R_G.

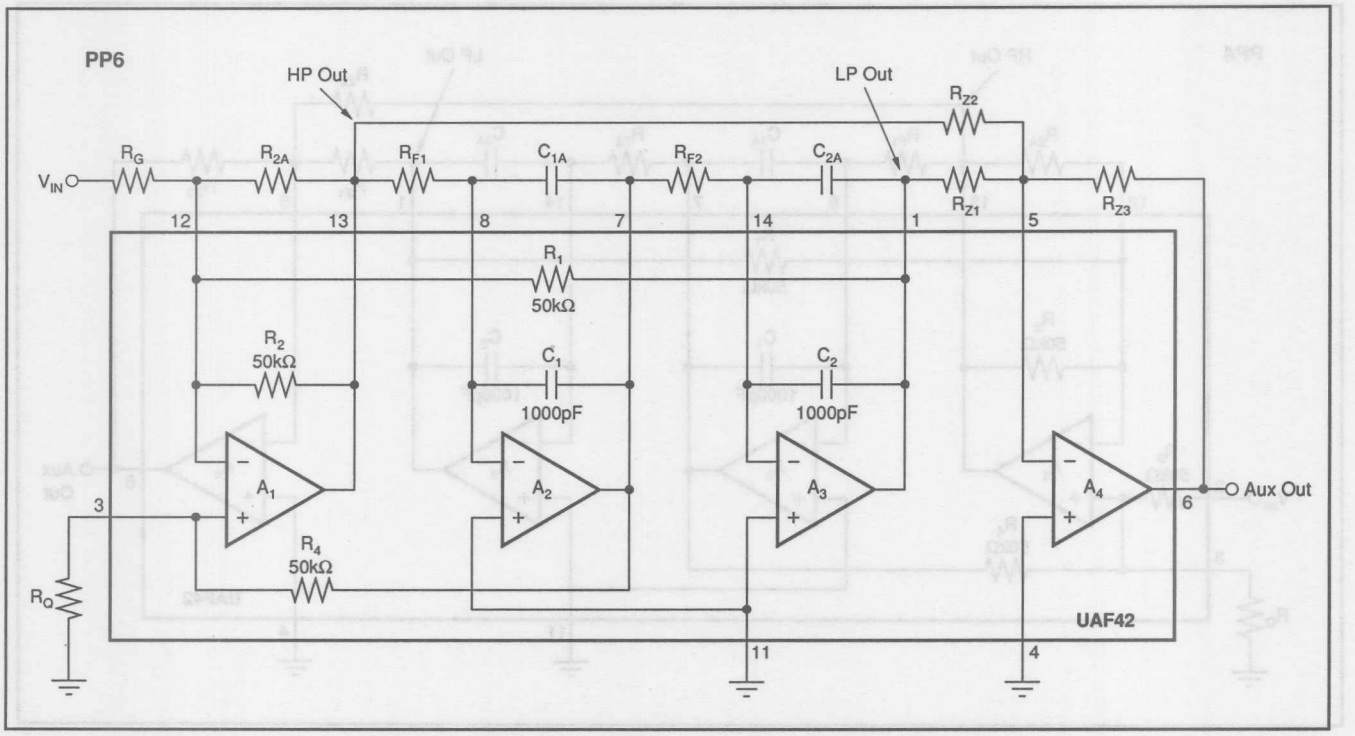


FIGURE 12. PP6 Inverting Pole-Pair/Zero Subcircuit.

This subcircuit option requires an external gain-set resistor, R_G.

LP (Real-pole low-pass subcircuit). The basic low-pass subcircuit (LP) is shown in Figure 13A. A single pole is formed by R_P and C_P. A_2 buffers the output to prevent loading from subsequent stages. If high input impedance is needed, an optional buffer, A_1, can be added to the input.

For an LP subcircuit with gain, use the optional circuit shown in Figure 13B.

For an LP subcircuit with inverting gain or attenuation, use the optional circuit shown in Figure 13C.

HP (Real-pole high-pass subcircuit). The basic high-pass subcircuit (HP) is shown in Figure 14A. A single pole is formed by R_P and C_P. A_2 buffers the output to prevent loading from subsequent stages. If high input impedance is needed, an optional buffer, A_1, can be added to the input.

For an HP subcircuit with gain, use the optional circuit shown in Figure 14B.

For an HP subcircuit with inverting gain or attenuation, use the optional circuit shown in Figure 14C.

IF THE AUXILIARY OP AMP IN A UAF42 IS NOT USED

If the auxiliary op amp in a UAF42 is not used, connect it as a grounded unity-gain follower as shown in Figure 15. This will keep its inputs and output in the linear region of operation to prevent biasing anomalies which may affect the other op amps in the UAF42.

ELIMINATING THE LP SUBCIRCUIT IN ODD-ORDER INVERSE CHEBYSHEV LOW-PASS FILTERS

Odd-order Inverse Chebyshev low-pass filters can be simplified by eliminating the LP input section and forming the real pole in the first pole-pair/zero subcircuit. To form the real pole in the pole-pair/zero subcircuit, place a capacitor, C_1, in parallel with the summing amplifier feedback resistor, R_{Z3}. The real pole must be at the same frequency as in the LP subcircuit. One way to achieve this is to set $C_1 = C_P$ and $R_{Z3} = R_P$, where C_P and R_P are the values that were specified for the LP section. Then, to keep the summing amplifier gains the same, multiply R_{Z1} and R_{Z2} by R_P/R_{Z3}.

Figures 16A and 16B show an example of the modification of a 3-pole circuit. It is a 347Hz-cutoff inverse Chebyshev low-pass filter. This example is from an application which required a low-pass filter with a notch for 400Hz system power-supply noise. Setting the cutoff at 347Hz produced the 400Hz notch. The standard filter (Figure 16A) consists of two subcircuits, an LP section followed by a PP4 section.

In the simplified configuration (Figure 16B), the summing amplifier feedback resistor, R_{Z3} is changed from 10kΩ to 130kΩ and paralleled with a 0.01µF capacitor. Notice that these are the same values used for R_P and C_P in the LP section of Figure 16A. To set correct the summing amplifier gain, resistors, R_{Z1} and R_{Z2} are multiplied by R_P/R_{Z3} (130kΩ/10kΩ). R_{Z1} and R_{Z2} must be greater than 2kΩ to prevent op amp output overloading. If necessary, increase R_{Z1}, R_{Z2}, and R_{Z3} by decreasing C_P.

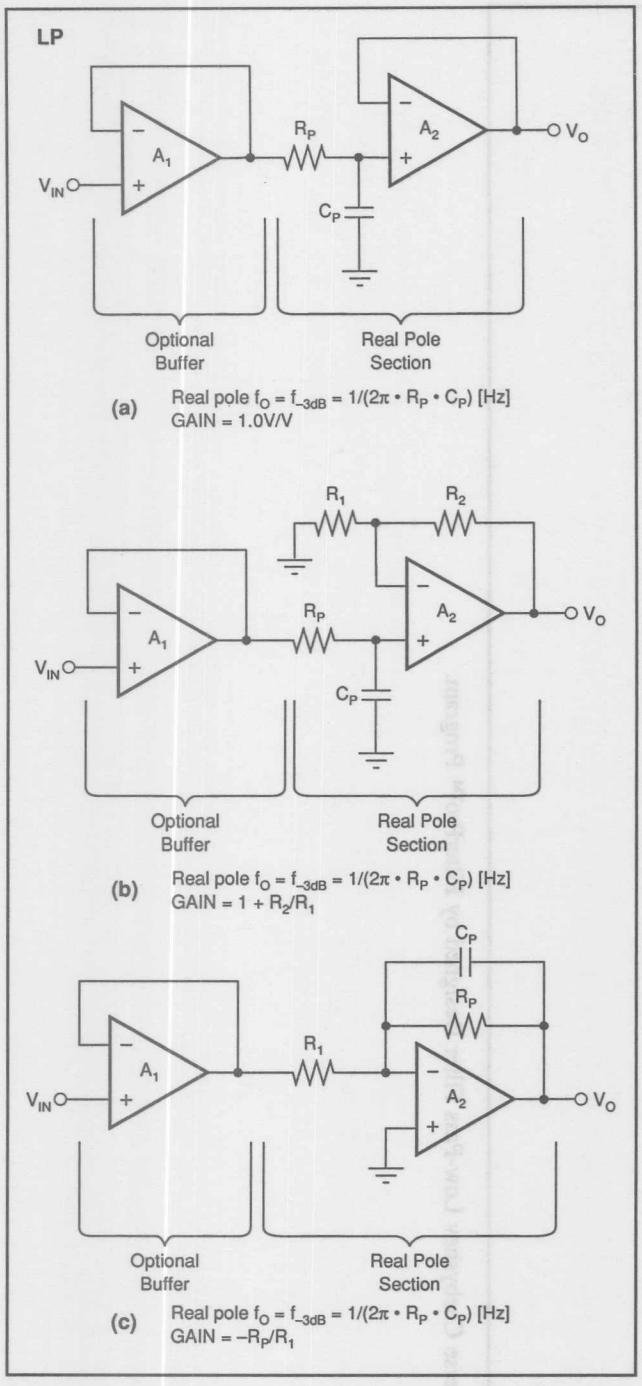


FIGURE 13. Low-Pass (LP) Subcircuit: (a) Basic; (b) with Noninverting Gain; (c) with Inverting Gain.

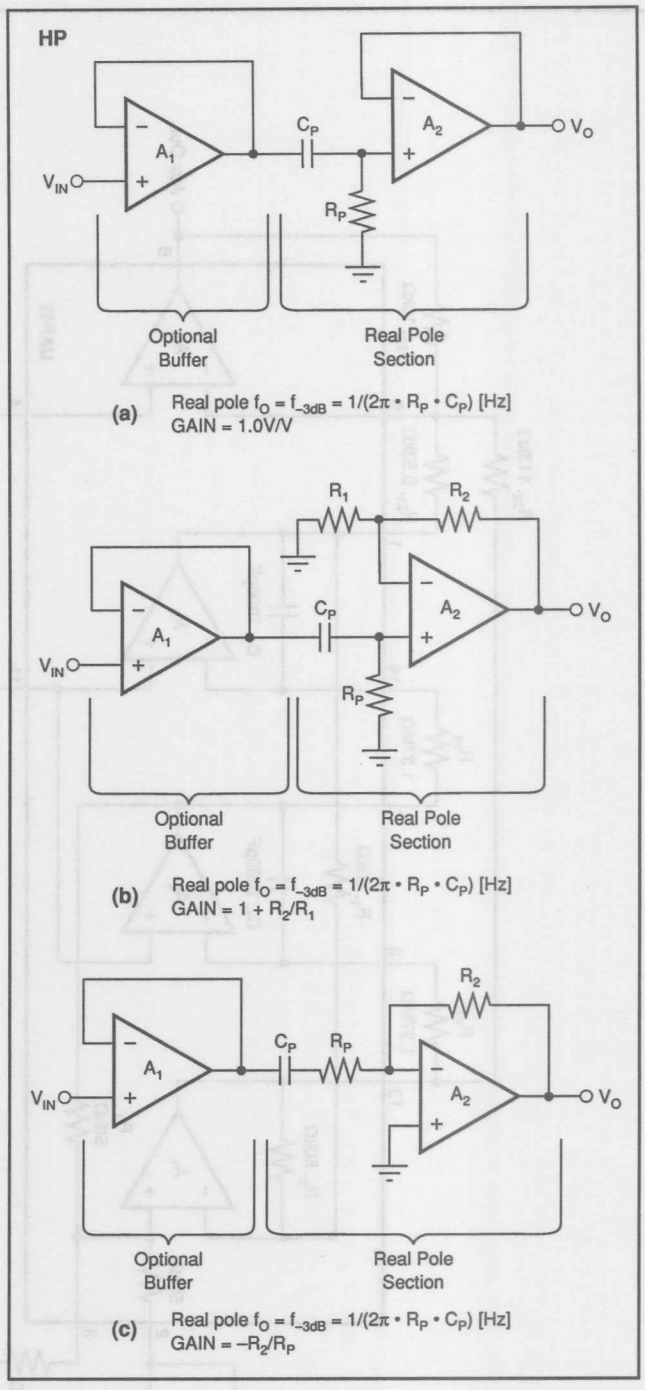


FIGURE 14. High-Pass (HP) Subcircuit: (a) Basic; (b) with Noninverting Gain; (c) with Inverting Gain.

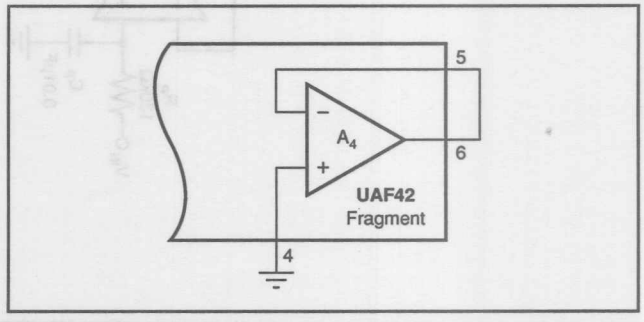


FIGURE 15. Connect Unused Auxiliary Op Amps as Grounded-Input Unity-Gain Followers.

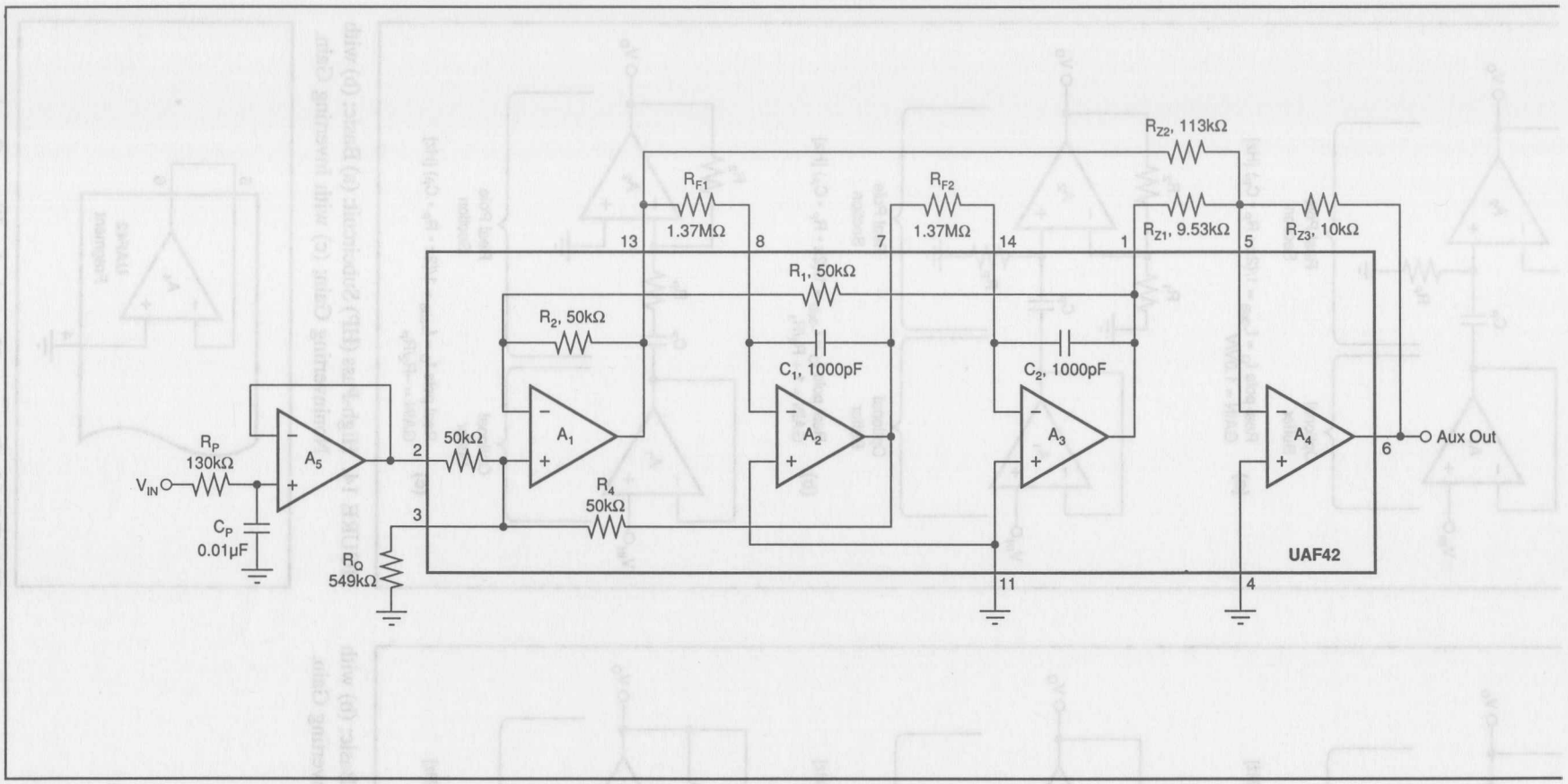
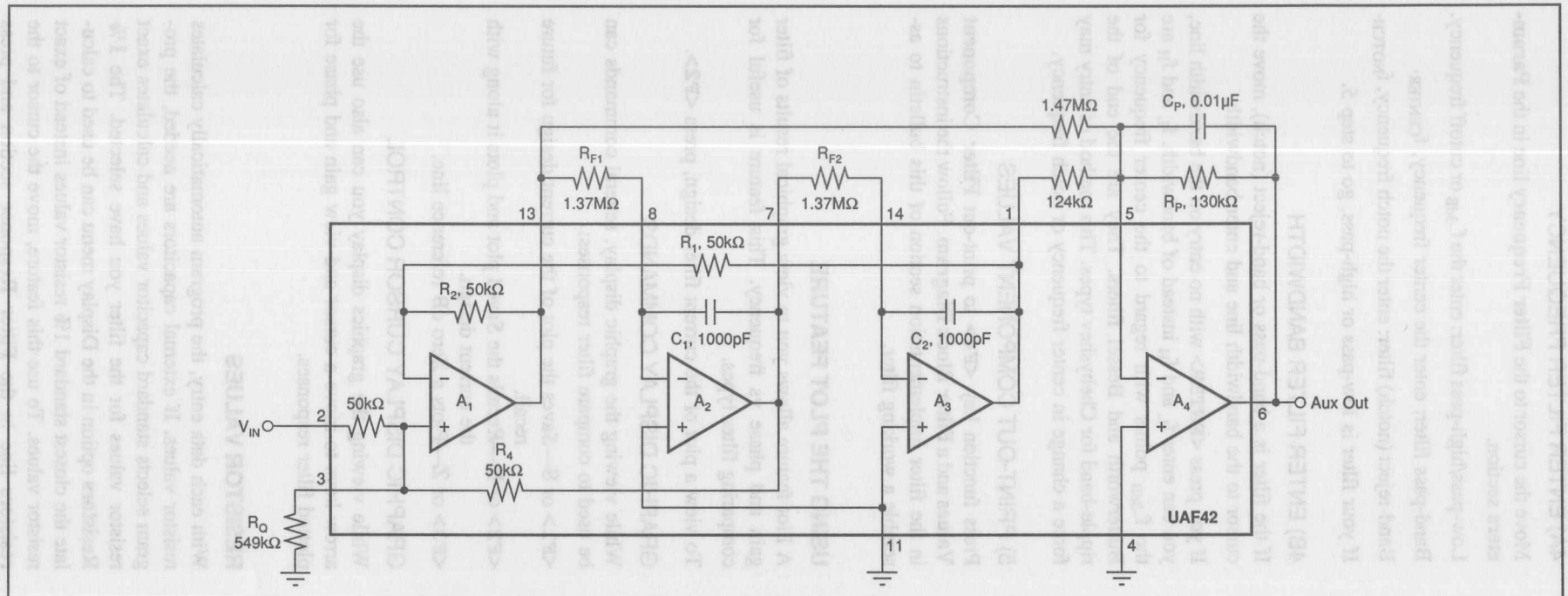


FIGURE 16A. Three-Pole 347Hz Inverse Chebyshev Low-Pass Filter Designed by FilterPro™ Program.



NOTE: To establish a real pole at the proper frequency and set the proper summing amplifier gain, the following changes were made to the pole-pair subcircuit:

R_{Z3} changed to R_P.

C_P added in parallel with R_{Z3}.

R_{Z1} and R_{Z2} multiplied by R_P/R_{Z3}.

FIGURE 16B. Simplified Three-Pole 347Hz Inverse Chebyshev Low-Pass Filter (created by moving real pole to feedback of A_4 and eliminating LP input section).

Q ENHANCEMENT

When the f_O • Q product required for a pole-pair section is above ≈100kHz at frequencies above ≈3kHz, op amp gain-bandwidth limitations can cause Q errors and gain peaking. To mitigate this effect, the program automatically compensates for the expected error by decreasing the design-Q according to a Q-compensation algorithm[1]. When this occurs, the value under the Q heading on the *UAF42 Filter Component Values* print-out will be marked with an asterisk indicating that it is the theoretical Q, not the actual design Q. The actual design Q will be shown under an added heading labeled Q_{COMP}.

USING THE FilterPro™ PROGRAM

With each data entry, the program automatically calculates filter performance. This allows you to use a "what if" spreadsheet-type design approach. For example; you can quickly determine, by trial and error, how many poles are needed for a desired roll-off.

GETTING STARTED

The first time you use the program, you may want to follow these suggested steps.

Type **FILTER42 <ENTER>** to start the program.

Use the arrow keys to move the cursor to the **Filter Response** section.

1) SELECT FILTER RESPONSE

Press **<ENTER>** to toggle through four response choices:

Low-pass
High-pass
Band-pass
Notch (band-reject)

When the desired response appears, move the cursor to the **Filter Type** section.

2) SELECT FILTER TYPE

Move the cursor to the desired filter type and press **<ENTER>**. The selected filter type is highlighted and marked with an asterisk. There are four filter-type choices:

Butterworth	Bessel
Chebyshev	Inverse Chebyshev

If you choose Chebyshev, you must also enter ripple (i.e. pass-band ripple—see Chebyshev filter description).

If you choose Inverse Chebyshev, you must also enter A_{MIN} (i.e. min attenuation or max gain in stop-band—see Inverse Chebyshev filter description).

3) ENTER FILTER ORDER

Move the cursor to the **Filter Order** line in the **Parameters** section. Enter filter order **n** (from 2 to 10).

4A) ENTER FILTER FREQUENCY

Move the cursor to the **Filter Frequency** line in the **Parameters** section.

Low-pass/high-pass filter: enter the f_{-3dB} or cutoff frequency.

Band-pass filter: enter the center frequency, f_{CENTER}.

Band-reject (notch) filter: enter the notch frequency, f_{NOTCH}.

If your filter is low-pass or high-pass, go to step 5.

4B) ENTER FILTER BANDWIDTH

If the filter is a band-pass or band-reject (notch), move the cursor to the bandwidth line and enter bandwidth.

If you press **<ENTER>** with no entry on the bandwidth line, you can enter f_L and f_H instead of bandwidth. f_L and f_H are the f_{-3dB} points with regard to the center frequency for Butterworth and Bessel filters. They are the end of the ripple-band for Chebyshev types. This method of entry may force a change in center frequency or notch frequency.

5) PRINT-OUT COMPONENT VALUES

Press function key **<F4>** to print-out **Filter Component Values** and a **Filter Block Diagram**. Follow the instructions in the filter implementation section of this bulletin to assemble a working filter.

USING THE PLOT FEATURE

A Plot feature allows you to view graphical results of filter gain and phase vs frequency. This feature is useful for comparing filter types.

To view a plot of the current filter design, press **<F2>**.

GRAPHIC DISPLAY COMMANDS

While viewing the graphic display, several commands can be used to compare filter responses:

<F1> or **S**—***S**aves* the plot of the current design for future recall.

<F2> or **R**—***R**ecalls* the ***S**aved* plot and plots it along with the current design.

<F3> or **Z**—Plots a **Z**ero dB reference line.

GRAPHIC DISPLAY CURSOR CONTROL

While viewing the graphics display you can also use the arrow keys to move a cursor and view gain and phase for plotted filter responses.

RESISTOR VALUES

With each data entry, the program automatically calculates resistor values. If external capacitors are needed, the program selects standard capacitor values and calculates exact resistor values for the filter you have selected. The **1% Resistors** option in the Display menu can be used to calculate the closest standard 1% resistor values instead of exact resistor values. To use this feature, move the cursor to the **resistors** line in the **Filter Response** section and press

---

(1) L.P. Huelsman and P. E. Allen, *Theory and Design of Active Filters*, p. 241.

OP AMP SELECTION GUIDE (In Order of Increasing Slew Rate)

T_A = 25°C, V_S = ±15V, specifications typ, unless otherwise noted, min/max specifications are for high-grade model.

OP AMP MODEL	BW typ (MHz)	FPR (1) typ (kHz)	SR typ (V/µs)	V_{OS} max (µV)	V_{OS}/dT max (µV/°C)	NOISE at 10kHz (nV/√Hz)	C_{CM} (3) (pF)
OPA177	0.6	3	0.2	10	±0.1	8	1
OPA27	8	30	1.9	25	±0.6	2.7	1
OPA2107 dual (2)	4.5	280	18	500	±5	8	4
OPA602 (2)	6	500	35	250	±2	12	3
OPA404 quad (2)	6	500	35	1000	±3 typ	12	3
OPA627 (2)	16	875	55	100	±0.8	4.5	7
UAF42 aux amp (2)	4	160	10	5000	±3 typ	10	4

NOTES: (1) FPR is full power response at 20Vp-p as calculated from slew rate. (2) These op amps have FET inputs. (3) Common-mode input capacitance.

<ENTER>. The program will toggle between **exact resistors** and **standard 1% resistors**.

CAPACITOR SELECTION

Even-order filters above 10Hz normally will not require external capacitors. Odd order filters require one external capacitor to set the real pole in the LP or HP section. Capacitor selection is very important for a high-performance filter. Capacitor behavior can vary significantly from ideal, introducing series resistance and inductance which limit Q. Also, nonlinearity of capacitance vs voltage causes distortion. The 1000pF capacitors in the UAF42 are high performance types laser trimmed to 0.5%.

If external capacitors are required, the recommended capacitor types are: NPO ceramic, silver mica, metallized polycarbonate; and, for temperatures up to 85°C, polypropylene or polystyrene. Common ceramic capacitors with high dielectric constants, such as "high-K" types should be avoided—they can cause errors in filter circuits.

OP AMP SELECTION

Normally you can use the uncommitted fourth op amp in the UAF42 to implement any necessary LP, HP, or gain stages. If you must use additional op amps, it is important to choose an op amp that can provide the necessary DC precision, noise, distortion, and speed.

OP AMP SLEW RATE

The slew rate of the op amp must be greater than $\pi \cdot V_{OPP} \cdot$ BANDWIDTH for adequate full-power response. For example, operating at 100kHz with 20Vp-p output requires an op amp slew rate of at least 6.3V/µs. Burr-Brown offers an excellent selection of op amps which can be used for high performance active filter sections. The guide above lists some good choices.

OP AMP BANDWIDTH

As a rule of thumb, in low-pass and band-pass applications, op amp bandwidth should be at least 50 • GAIN • f_O, where GAIN = noise gain of the op amp configuration and f_O = filter f_{-3dB} or f_{CENTER} frequency.

In high-pass and band-reject (notch) applications, the required op amp bandwidth depends on the upper frequency of interest. As with most active filters, high-pass filters designed with the UAF42 turn into band-pass filters with an upper roll-off determined by the op amp bandwidth. Error due to op amp roll-off can be calculated as follows:

$$\% = 100\left(1 - \frac{1}{\sqrt{(1 + f^2 \cdot (NGAIN)^2/(UGBW)^2)}}\right)$$

or

$$f = \frac{\sqrt{200 - \%} \cdot \sqrt{\%} \cdot UGBW}{NGAIN \cdot (\% - 100)}$$

Where:

% = Percent gain error f = Frequency of interest (Hz)

NGAIN = Noise gain of op amp (V/V)

= GAIN of noninverting configuration

= 1 + |GAIN| of inverting configuration

UGBW = Unity-gain bandwidth of the op amp (Hz):

GAIN ACCURACY (%)	f (NGAIN)/(UGBW)
–29.29	1.000
–10.00	0.484
–1.00	0.142
–0.10	0.045
–0.01	0.014

EXAMPLES OF MEASURED UAF42 FILTER RESPONSE

Figures 17 and 18 show actual measured magnitude response plots for 5th-order 5kHz Butterworth, 3dB Chebyshev, –60dB Inverse Chebyshev and Bessel low-pass filters designed with the program and implemented with UAF42s. As can be seen, the initial roll-off of the Chebyshev filter is the fastest and the roll-off of the Bessel filter is the slowest. However, each of the 5th-order all-pole filters ultimately rolls off at –N • 20dB/decade, where N is the filter order (–100dB/decade for a 5-pole filter).

The oscilloscope photographs (Figures 19-22) show the step response for each filter. As expected, the Chebyshev filter has the most ringing, while the Bessel has the least.

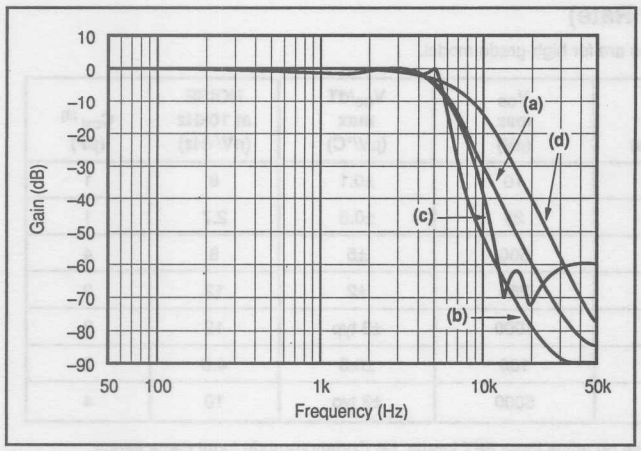


FIGURE 17. Gain vs Frequency for Fifth-Order 5kHz (a) Butterworth, (b) 3dB Chebyshev, (c) –60dB Inverse Chebyshev, and (d) Bessel Unity-Gain Low-Pass Filters, Showing Overall Filter Response.

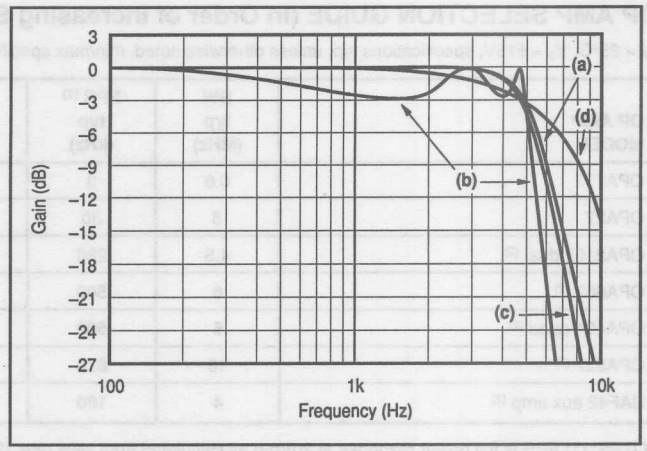


FIGURE 18. Gain vs Frequency for Fifth-Order 5kHz (a) Butterworth, (b) 3dB Chebyshev, (c) –60dB Inverse Chebyshev, and (d) Bessel Unity-Gain Low-Pass Filters, Showing Transition-Band Detail.

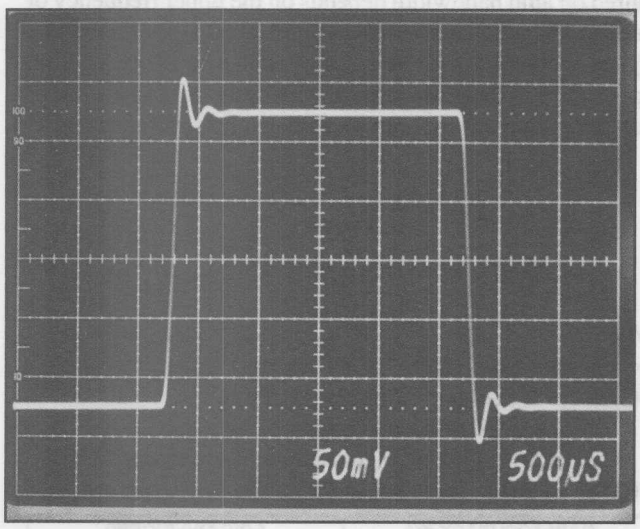


FIGURE 19. Step Response of Fifth-Order 5kHz Butterworth Low-Pass Filter.

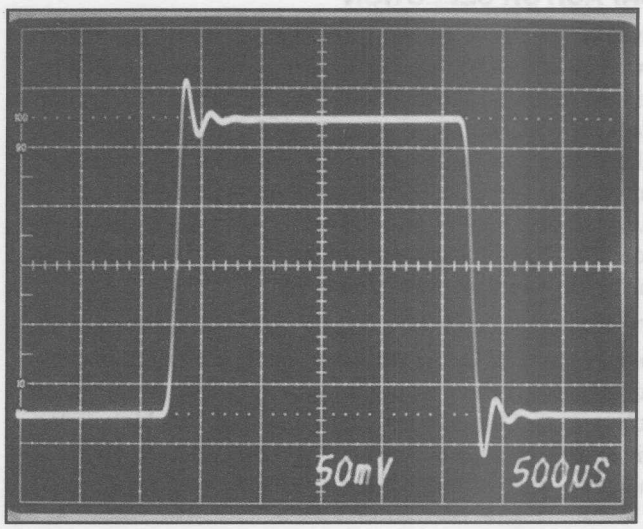


FIGURE 21. Step Response of Fifth-Order 5kHz, –60dB Inverse Chebyshev Low-Pass Filter.

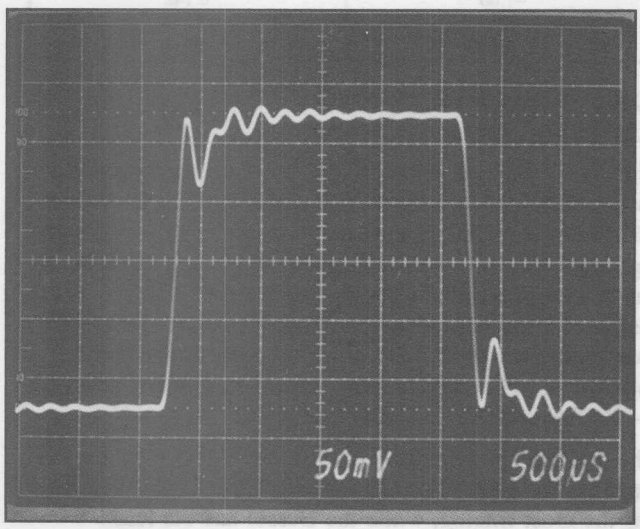


FIGURE 20. Step Response of Fifth-Order 5kHz, 3dB Ripple Chebyshev Low-Pass Filter.

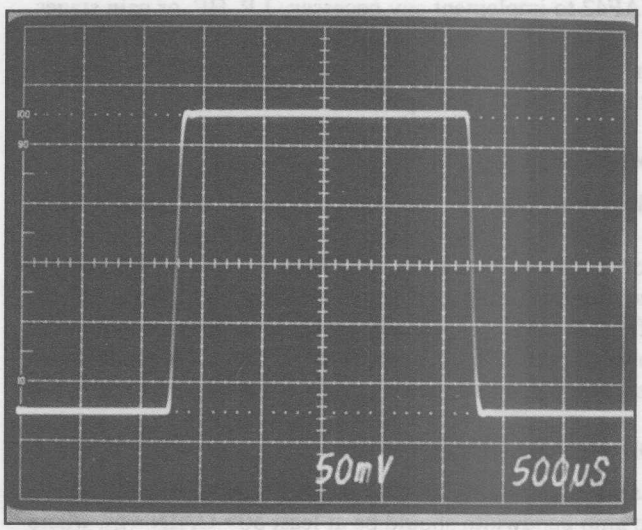


FIGURE 22. Step Response of Fifth-Order 5kHz Bessel Low-Pass Filter.

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INCREASING ADC603 INPUT RANGE

By Gordon Gleason (602) 746-7494, and R. Mark Stitt

The ADC603 is a 10MHz, 12-bit analog-to-digital converter with a ±1.25V input range. Many applications call for a higher input range such as ±2.5V. A resistor divider can be used as an input attenuator to increase the input range. The OPA620 can be used to buffer the input attenuator for high-source-impedance applications. Suggested component values and measured performance results are shown in this bulletin.

Since the ADC603 has a high-impedance input, a simple voltage divider as shown in Figure 1 can be used to increase its voltage input range. The source impedance of the divider as seen by the ADC603 is $R_1 \parallel R_2$ (the parallel combination of R_1 and R_2). A divider source impedance of 50Ω is recommended since it has been shown to give consistently good results. If a higher divider input impedance is needed and adding a buffer is not viable, source impedances up to 500Ω should give satisfactory results. If hardware gain trim is needed, select the next higher 1% resistor value for R_1 and use a 10kΩ multi-turn trim pot in parallel with R_1 for gain trim.

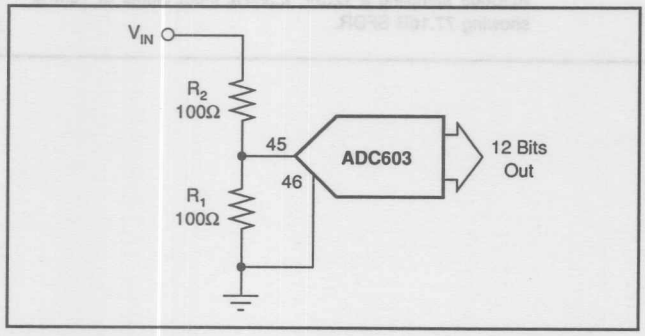

FIGURE 1. ADC603 12-Bit ADC with 2/1 Input Attenuator to Provide ±2.5V Input Range.

If an input impedance of 50Ω to the circuit is needed as a termination, add a third resistor as shown in Figure 2. The three-resistor approach improves accuracy by placing the majority of the termination power dissipation in the third resistor. This minimizes error-producing self heating in the precision divider network. Pay attention to the power rating for R_3. For a ±10V input, R_3 must be rated 2W.

If a high input impedance is needed, drive the divider with a unity-gain-connected OPA620 buffer amp as shown in Figure 3. The OPA620 can be used for inputs as high as ±3V.

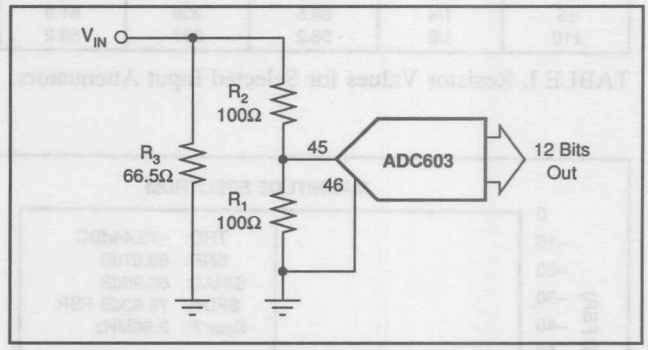

FIGURE 2. ADC603 12-Bit ADC with Three-Resistor 2/1 Input Attenuator to Provide ±2.5V Input Range and 50Ω Termination Impedance.

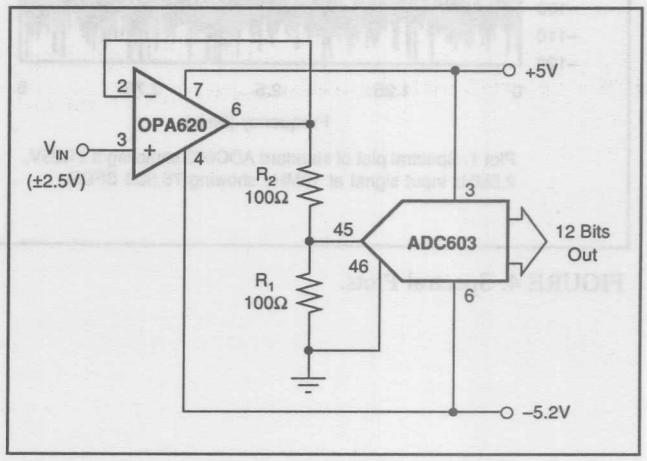

FIGURE 3. ADC603 12-Bit ADC with 2/1 Input Attenuator to Provide High Input Impedance ±2.5V Input Range.

Equations for determining recommended resistor values are:

$R_1 = 50\Omega \cdot N/(N - 1)$

$R_2 = (N - 1) \cdot R_1$

$R_3 = 50\Omega \cdot (R_1 + R_2)/(R_1 + R_2 - 50\Omega)$

Where:

R_1, R_2, R_3 are in Ω

N = input divider ratio

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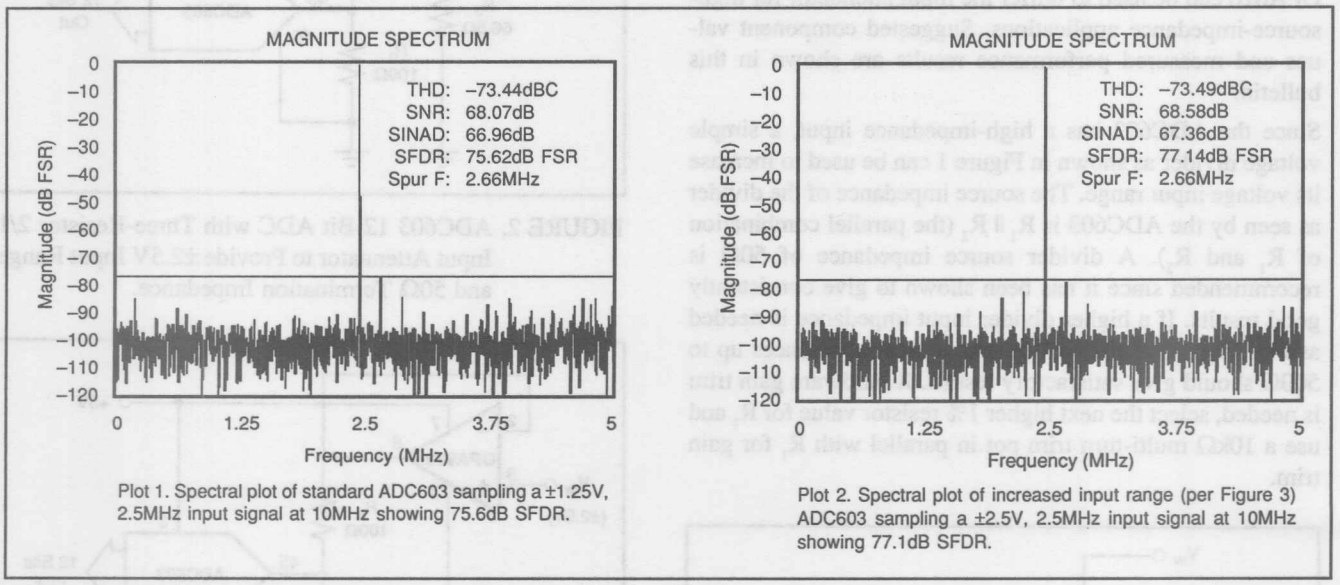
The table below shows recommend resistor values for selected input ranges.

INPUT RANGE (V)	DIVIDER (1/N)	R_1 (Ω)	R_2 (Ω)	R_3 (Ω)
±2	1/1.6	133	80.6	64.9
±2.5	1/2	100	100	68.1
±3	1/2.4	86.6	121	66.5
±5	1/4	66.5	200	61.9
±10	1/8	56.2	397	56.2

TABLE I. Resistor Values for Selected Input Attenuators.

The spectral plots compare a standard ±1.25V input ADC603 to a ±2.5V input, OPA620 buffered ADC603 per Figure 3. In both cases, the circuit is sampling a 2.5MHz signal at 10MHz. The results show that the spurious-free dynamic range of the boosted circuit is as good as for the standard circuit. If anything, the boosted circuit has better performance (77dB vs 76dB). The ADC603 seems to perform slightly better when driven by the purely resistive 50Ω divider impedance instead of the complex impedance of the cable and signal generator.



Plot 1. Spectral plot of standard ADC603 sampling a ±1.25V, 2.5MHz input signal at 10MHz showing 75.6dB SFDR.

Plot 2. Spectral plot of increased input range (per Figure 3) ADC603 sampling a ±2.5V, 2.5MHz input signal at 10MHz showing 77.1dB SFDR.

FIGURE 4. Spectral Plots.

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USING THE ADS7800 12 BIT ADC WITH UNIPOLAR INPUT SIGNALS

By R. Mark Stitt and Dave Thomas (602) 746-7445

The ADS7800 12 bit Sampling analog-to-digital-converter is designed to operate with bipolar inputs of ±5V or ±10V. With the addition of an external amplifier, the ADS7800 can be used for 10V or 20V unipolar inputs. Four unipolar input options are shown in this Bulletin.

ADS7800 UNIPOLAR VOLTAGE INPUT RANGES

INPUT	SEE FIGURE
0 to +10V	2
0 to –10V	3
0 to +20V	4
0 to –20V	5

To understand how the circuits work, consider the ADS7800 input voltage divider network shown in Figure 1. Since the input resistor divider network drives a high impedance at V_O, the transfer function is:

$$V_O = \frac{R_3 (R_2 V_1 + R_1 V_2)}{R_1 R_2 + R_1 R_3 + R_2 R_3}$$

since $R_2 = R_3$ and $R_1 = 2 R_2$,

$$V_O = \frac{V_1 + 2 V_2}{5}$$

Where:
V_1 = voltage at pin 1 (V)
V_2 = voltage at pin 2 (V)
V_O = voltage into ADC cell (V)

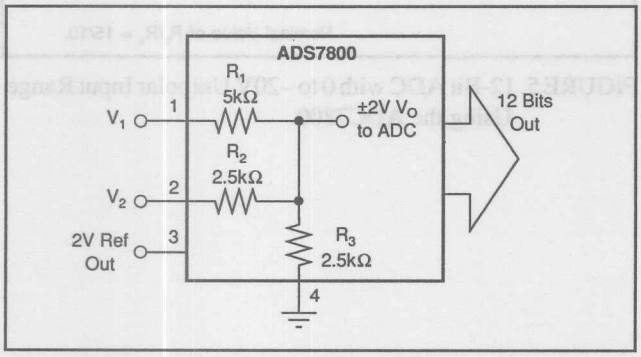

FIGURE 1. ADS7800 Input-Voltage Scaling Resistor Network.

The internal ADC gives a zero to full-scale digital output with ±2V at V_O (the internal ADC node voltage shown in Figure 1). When used in the standard bipolar voltage input mode, with $V_2 = 0$ (i.e. V_2 connected to analog ground), ±10V input at pin 1 of the ADS7800 produces ±2V output at V_O. Similarly, ±5V input at pin 2 produces ±2V V_O with V_1 grounded. There are four unipolar input range connections to the ADS7800 that will produce ±2V V_O when V_1 or V_2 is connected to an appropriate offsetting voltage instead of ground. A summary of the four cases is shown in Table I.

INPUT RANGE	V_1	V_2	V_O
±5V	0 (Ground)	INPUT	±2V
±10V	INPUT	0 (Ground)	±2V
0 to +10V	-10.000V	INPUT	±2V
0 to –10V	+10.000V	INPUT	±2V
0 to +20V	INPUT	–5.000V	±2V
0 to –20V	INPUT	+5.000V	±2V

TABLE I. ADS7800 Input Ranges (see Figure 1).

The +2.0V reference output from the ADS7800 can be amplified to provide the ±5V or ±10V offsetting voltage needed. The circuits in Figures 2 to 5 show how to connect inverting or noninverting amplifiers for the various input ranges.

Adjustment of the offsetting voltage is required because the absolute accuracy of the 2.0V ADS7800 reference output may vary by a few percent. Adjust the 1kΩ pot for an accurate offsetting voltage (e.g. V_2 = 5.000V or V_1 = 10.000V). Even though the reference output of the ADS7800 does not have absolute accuracy, the gain of the ADC is scaled to its value. Scaling the internal reference to generate the offsetting voltage preserves gain accuracy with temperature and supply variation so long as the R_4/R_5 resistor ratio tracks with temperature and a low drift op amp, such as the OPA177, is used.

If desired, the ADC zero (negative full-scale) can be adjusted by fine trimming the offsetting voltage with the 1kΩ pot. To adjust the ADC zero, apply a 1/2 LSB voltage to the input of the ADC and adjust the gain adjust pot so the LSB output, pin 17, toggles between 1 and 0.

The 1/2 LSB zero-adjust voltage can be derived from a resistor divider connected to a voltage source (See Application Bulletin AB-003, 004, and 005 for ±10V references). Remember to consider the input impedance of the ADC when using a resistor divider. In the 10V range, the input impedance is 2.5kΩ + (2.5kΩ || 5kΩ) = 4.17kΩ, in the 20V range the input impedance is 5kΩ + (2.5kΩ || 2.5kΩ) = 6.25kΩ. Recommended values for a zero-adjust divider are:

INPUT RANGE (V)	1/2 LSB (V)	V_{REF} (V)	R_{D1} (kΩ)	R_{D2} (Ω)
0 to +10	0.012	+10.00	8.25	10.0
0 to –10	–0.012	–10.00	8.25	10.0
0 to +20	0.024	+10.00	4.12	10.0
0 to –20	–0.024	–10.00	4.12	10.0

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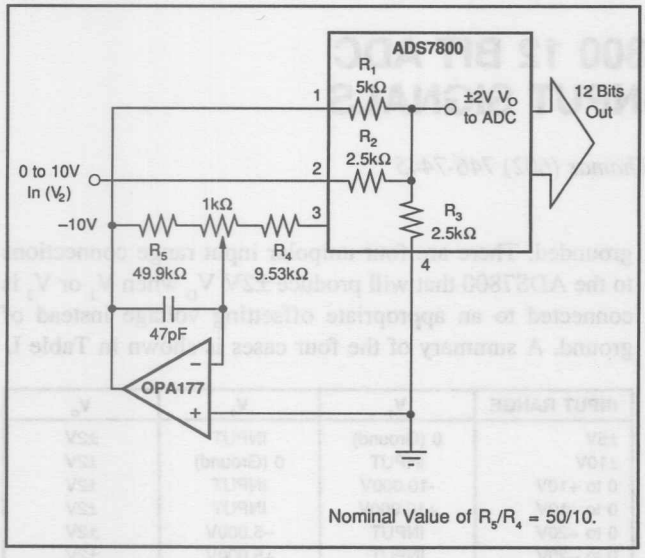

FIGURE 2. 12-Bit ADC with 0 to 10V Unipolar Input Range Using the ADC7800.

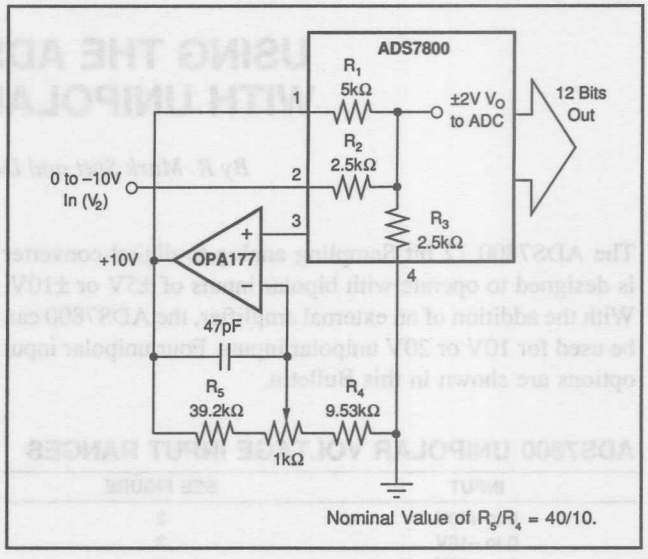

FIGURE 3. 12-Bit ADC with 0 to –10V Unipolar Input Range Using the ADC7800.

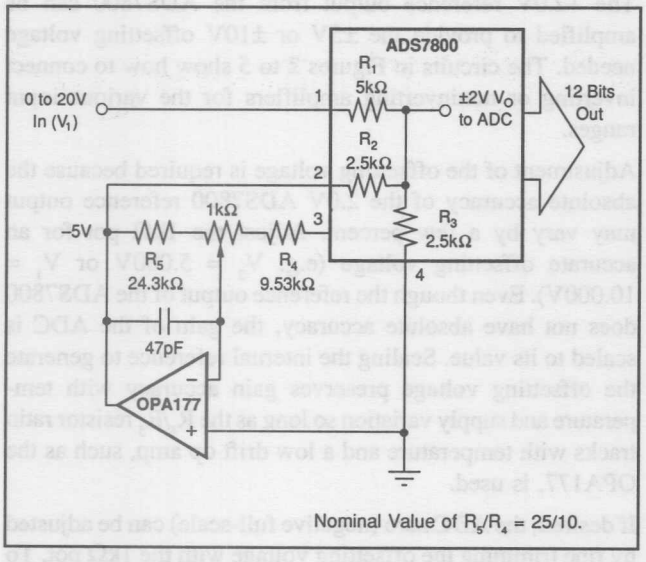

FIGURE 4. 12-Bit ADC with 0 to 20V Unipolar Input Range Using the ADC7800.

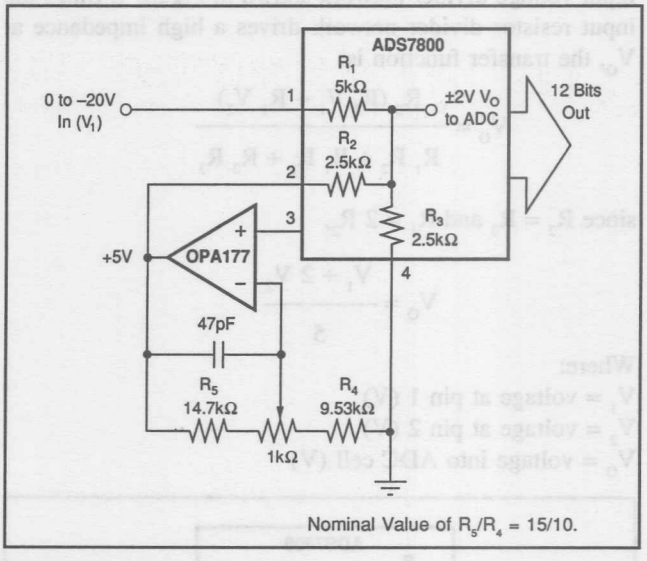

FIGURE 5. 12-Bit ADC with 0 to –20V Unipolar Input Range Using the ADC7800.

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FREQUENCY-TO-VOLTAGE CONVERSION

By R. Mark Stitt and Rod Burt (602) 746-7445

Precision frequency-to-voltage converters (FVC)s can be made using voltage-to-frequency converters (VFCs). Burr-Brown offers a complete line of precision free-running VFCs.

VFC110 High frequency, low jitter VFC
4MHz max full-scale, ±0.02% typ linearity at 2MHz

VFC121 Precision single-supply VFC (+4.5V to +36V)
1.5MHz max full-scale, 0.03% max nonlinearity at 100kHz

VFC320 Precision VFC
1MHz max full-scale, 0.005% max nonlinearity at 10kHz

This bulletin describes three techniques for making a precision FVC using a VFC. The standard technique has high precision, but high ripple or slow settling. Adding an output filter can improve the settling-time, ripple trade-off, but adds error. A third new technique can eliminate ripple from the FVC output and improve settling time by more than 1000/1 as compared to the conventional FVC. Moreover, the DC precision is unaffected.

FVC APPLICATIONS

A rapidly-growing application for frequency-to-voltage converters is high-voltage analog signal isolation. High-voltage analog isolation amplifiers (ISO Amps), such as the Burr-Brown ISO121, are available for isolating signals up to 8000V. Higher voltage isolation of tens-of-thousands or even millions of volts as in utility-power-transmission line monitoring, nuclear event monitoring, and protection from lightning strikes calls for other techniques. You can get virtually unlimited isolation by using a voltage-to-frequency converter (VFC) to digitize an analog signal and transmit it over a fiber-optic data link to a FVC where the signal is reconstructed.

Many times VFCs are favored for analog-to-digital conversion because of their integrating input characteristic and high resolution (modern Sigma-delta analog-to-digital converters are really a variation of a VFC with digital filtering and encoding). An analog signal digitized by a VFC can be transmitted to a remote receiver serially over a single twisted pair wire cable or isolated with a single optical isolator. At the other end, the digital signal can be

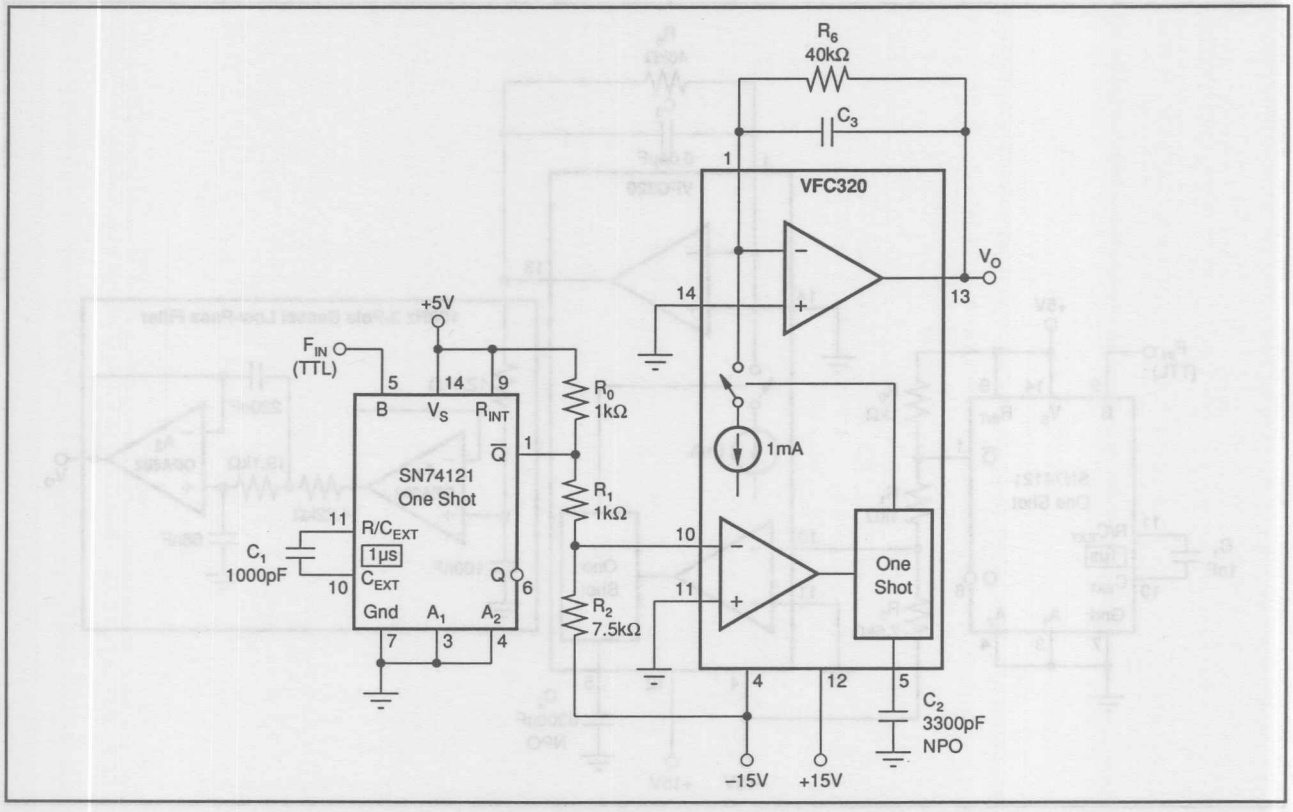

FIGURE 1. A Conventional Frequency-to-Voltage Converter. This FVC can be made by connecting a Burr-Brown VFC320 voltage-to-frequency converter in the FVC Mode. Select C_3 for ripple/settling-time trade off.

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both digitally processed and reconstructed to analog. An analog signal is often required, as in medical applications, for bedside monitoring on a CRT or LCD display. The fast-settling, ripple-free characteristics of the FVC described here makes it ideal for this application too.

THE CONVENTIONAL FVC

In an conventional FVC, a one-shot-controlled current reference is averaged. A serious problem with the conventional FVC results from a trade-off between ripple and settling time. Improved resolution from the FVC demands low ripple, but decreasing the ripple increases settling time.

An example of a conventional FVC circuit is shown in Figure 1. It uses a Burr-Brown VFC320 voltage to frequency converter connected in the FVC mode. The SN74121 one shot along with input resistors, R_1, R_2, and pull-up resistor R_0 convert a TTL-logic-level input into a 1µs negative-going pulse to trip the ground-referenced comparator in the VFC320. When tripped, the comparator triggers a precision one shot in the VFC320. When triggered, a 1mA current reference in the VFC320 is switched to the input of an averaging transimpedance amplifier for the period of the one shot.

The transimpedance amplifier can be thought of as an integrator consisting of an op amp in the VFC320 with an external integrating capacitor, C_3. A current proportional to the integrator output voltage is summed in through feedback resistor, R_6. Both the periodic 1mA current pulse and the current through R_6 are integrated in C_3. The average voltage at the output of the integrator is proportional to the input frequency, the precision one-shot period, the current reference, and the external feedback resistor, R_6.

The duration of the one-shot period is determined by the external one-shot capacitor, C_2. In this example, the one-shot pulse-width is set at 25µs for a full-scale FVC input range of 10kHz. It has been empirically determined that best VFC or FVC linearity is obtained when the one shot pulse width is approximately 25% of the full-scale input period.

The integrator output ramps up during the one-shot period, integrating the sum of the 1mA current source and the current through the feedback resistor. Then, the one-shot output ramps down during the balance of the input frequency period, integrating only the current through the feedback resistor. The peak-to-peak value of this ramp appears at the FVC output as ripple.

The value of the integrator capacitor affects the FVC output ripple, but does not affect the average DC output voltage. Increasing the value of the integrator capacitor decreases the voltage ripple, and increases the time for the integrator output to settle for a change in input frequency. Settling time follows a single pole response. The following relationships apply for the conventional FVC:

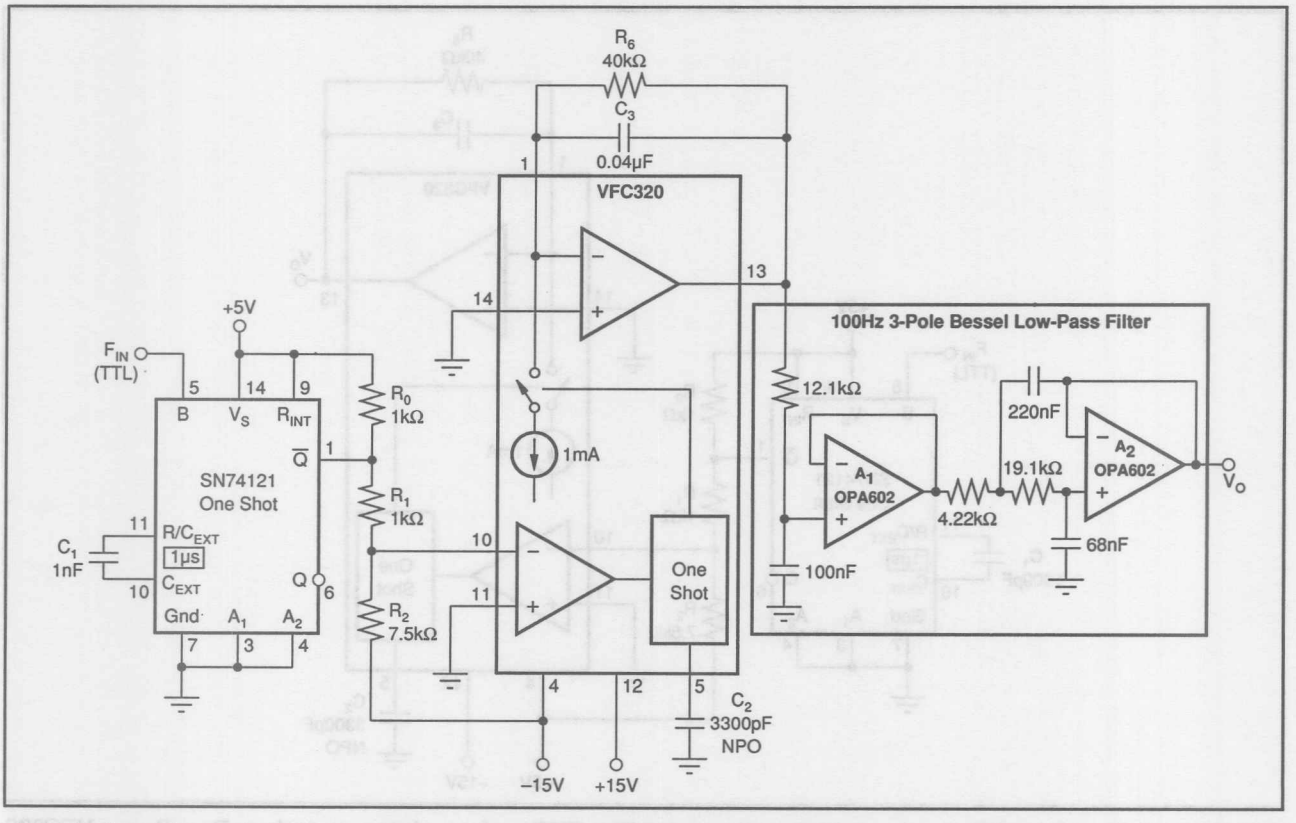


FIGURE 2. A Conventional Frequency-to-Voltage Converter. This converter with a 3-pole low-pass Bessel filter added to the output has less than 1mV ripple at 1.2kHz and can settle to 0.01% in 18ms.

$V_O = F_{IN} \cdot T_{OS} \cdot I_R \cdot R_6$
(same for conventional and fast-settling FVC)

$RIPPLE \approx T_{OS} \cdot I_R / C_3$

$t_S = R_6 \cdot C_3 \cdot \ln\left(\frac{100\%}{P\%}\right)$

Where:

V_O = Average output voltage [V]

F_{IN} = Input frequency [Hz]
(10kHz full-scale in this example)

I_R = Current reference [A]
(1mA for the VFC320)

T_{OS} = One-shot period [s]
(25µs in this example)

t_S = time for the output to settle to desired tolerance [s]

R_6 = Integrator feedback resistor [Ω]
(40kΩ for 10V full scale output with 10kHz input)

RIPPLE = Variation in V_O [Vp-p]

C_3 = Value of integrator capacitor [F]

P = Desired precision of the output signal
[% of full-scale]

CONVENTIONAL FVC PERFORMANCE

The conventional FVC has excellent DC performance, but poor dynamic performance. For example, consider an FVC with 10V full-scale output for 10kHz input. Using the VFC320 voltage-to-frequency converter with I_R = 1mA and T_{OS} = 25µs, R_6 must be 40kΩ. In the conventional FVC, for 0.01% resolution (1mV ripple), C_3 must be set to 25µF and settling time is an astoundingly long 9.2s.

FILTERING THE CONVENTIONAL FVC

In practice, the settling-time/ripple trade-off of the conventional FVC can be improved substantially by filtering the FVC output with a higher-order low-pass filter as shown in Figure 2. In this approach, a conventional FVC is designed with relatively high output ripple to give fast settling time. Then a high-order low-pass filter is added in series with the FVC output to reduce the ripple.

In the Figure 2 example, a value of 40kΩ was used for R_6 to set a 10V full-scale output for a 10kHz input. A value of 0.04µF is used for C_3 giving approximately 625mV max ripple. This is an arbitrary but adequate value to give excellent linearity and a 10V full-scale output. Higher ripple would reduce the linear output range of the FVC because, at full-scale output, the FVC must swing 10V plus approximately one half the ripple voltage.

There are many output filter possibilities for a filtered FVC. Because of its excellent pulse response a Bessel filter gives the fastest settling of any standard filter type. The tables below show examples of FVC performance for Bessel filters of order 2 through 5. The 3-pole Bessel filter gives a good settling-time complexity trade-off. Figure 2 shows the conventional FVC with a 3-pole Sallen-Key Bessel filter. With the filter f_{-3dB} frequency set to 100Hz, ripple at 1.2kHz is below 1mV and settling time to 0.01% is 18ms. Notice that ripple increases dramatically below 1.2kHz when higher-order filters are used.

FILTERED FVC PERFORMANCE WITH BESSEL FILTER

FILTER ORDER	f-3dB (Hz)	SETTLING (0.01%) (ms)	RIPPLE (at 1.2kHz) (mV)	RIPPLE (at 400Hz) (mV)
2	35	38	1	8
3	100	18	1	25
4	155	17	1	59
5	205	17	1	134

The Sallen-Key filter architecture, used for the low-pass filter, was selected for low gain error. You can't include the filter in the feedback loop because the excessive phase-shift would cause instability. Since the filter must be added outside the integrator feedback loop, DC errors such as gain offset and offset drift add to the transfer function of the FVC. In the unity-gain Sallen-Key architecture, the op amps are connected as voltage-followers so gain error is negligible. You still must use low-drift precision op amps to reduce offset and offset drift errors. Other active filters can be designed with easy-to-use DOS-compatible programs available free of charge from Burr-Brown—request the FilterPro™ filter design software. These programs make it easy to design a wide variety of practical Sallen-Key, Multiple Feedback (MFB), and State-Variable active filters up to tenth order. State-Variable active filters use the UAF42 monolithic Universal Active Filter which contains on-chip precision capacitors so that external capacitors are not required.

The filtered FVC gives a good improvement in settling time. However, even with the complexity of a 3-pole filter, its performance pales in comparison to the fast-settling FVC. Filtering, with a 3-pole filter, can give 18ms settling to 0.01% with less than 1mV ripple at 1.2kHz, but ripple increases at lower frequencies. For comparison, the new fast-settling FVC, using the same R_6, C_3 values, settles to 0.01% in 7.4ms with less than 1mV ripple at any frequency.

THE NEW FAST-SETTLING FVC

Instead of using a filter in series with the output, the fast-settling FVC uses a sample/hold amplifier inside the integrator feedback loop of the conventional FVC. One way to think of the fast-settling FVC is as a conventional FVC with an adaptive N-pole filter in its feedback. The order, N, of the adaptive filter approaches a very high value so that all integrator output ripple is removed regardless of input frequency. By comparison, the output ripple of the filtered FVC increases with decreasing frequency. Also, delay of the adaptive filter is low so that it can be included in the feedback loop to the integrator without adversely affecting stability. This is not possible with a conventional filter. With the filter included in the feedback loop, DC filter errors (sample/hold errors) such as gain, offset, and offset drift are divided-down by the loop gain of the integrator amplifier to negligible levels.

and C_3. In theory, a smaller value could be used for C_3 in the fast-settling FVC for better settling time. Ripple at the output is eliminated by using a sample/hold to sample the VFC320 integrator output. The only constraint on ripple voltage is that it must be within the linear output-swing range of integrator amplifier. Gain can be added in the sample/hold circuit to reduce the peak amplitude needed from the integrator output. In the filtered approach, added gain would also gain-up the ripple.

In the fast-settling FVC, the sample/hold acquires a feedback signal from the integrator output ramp in approximately 1µs so that the ripple of the ramp is translated to a higher frequency and substantially eliminated by a simple single-pole high-frequency filter, R_5, C_5. The delay through the high-frequency filter is low enough so that it can also be included in the feedback loop.

Since the sample/hold is in the feedback loop of the integrator, trigger timing is unimportant. The feedback loop automatically adjusts the relative level of the integrator output signal for proper alignment with the trigger pulse.

verter connected as a level shifter. Pull-down resistor R_8 is added at the output of the integrator amplifier to boost output drive to the sample/hold capacitor, C_4.

Design of the sample/hold is greatly simplified because DC accuracy is unimportant. The complete sample/hold circuit consists of a common DMOS FET, Q_1, hold capacitor, C_4, and FET-input op amp, A_1. High frequency sampling glitches are also filtered out by the R_5, C_5 output filter. Since the glitch filter is also in the integrator feedback loop, associated DC errors are eliminated, and low DC output impedance is maintained.

Sample/hold gain is set to 2.0V/V by R_3 and R_4. The sample/hold gain attenuates (by two) the maximum output excursion necessary from the VFC320 integrator output, allowing both a comfortable +10V full-scale output from the FVC and a large ripple signal at the integrator output.

Gain in the feedback loop of the integrator also increases slew rate and bandwidth. With a high slew-rate op amp used for A_1, FVC slew rate is limited by the integrator op amp. Adding a gain of two in the feedback loop doubles

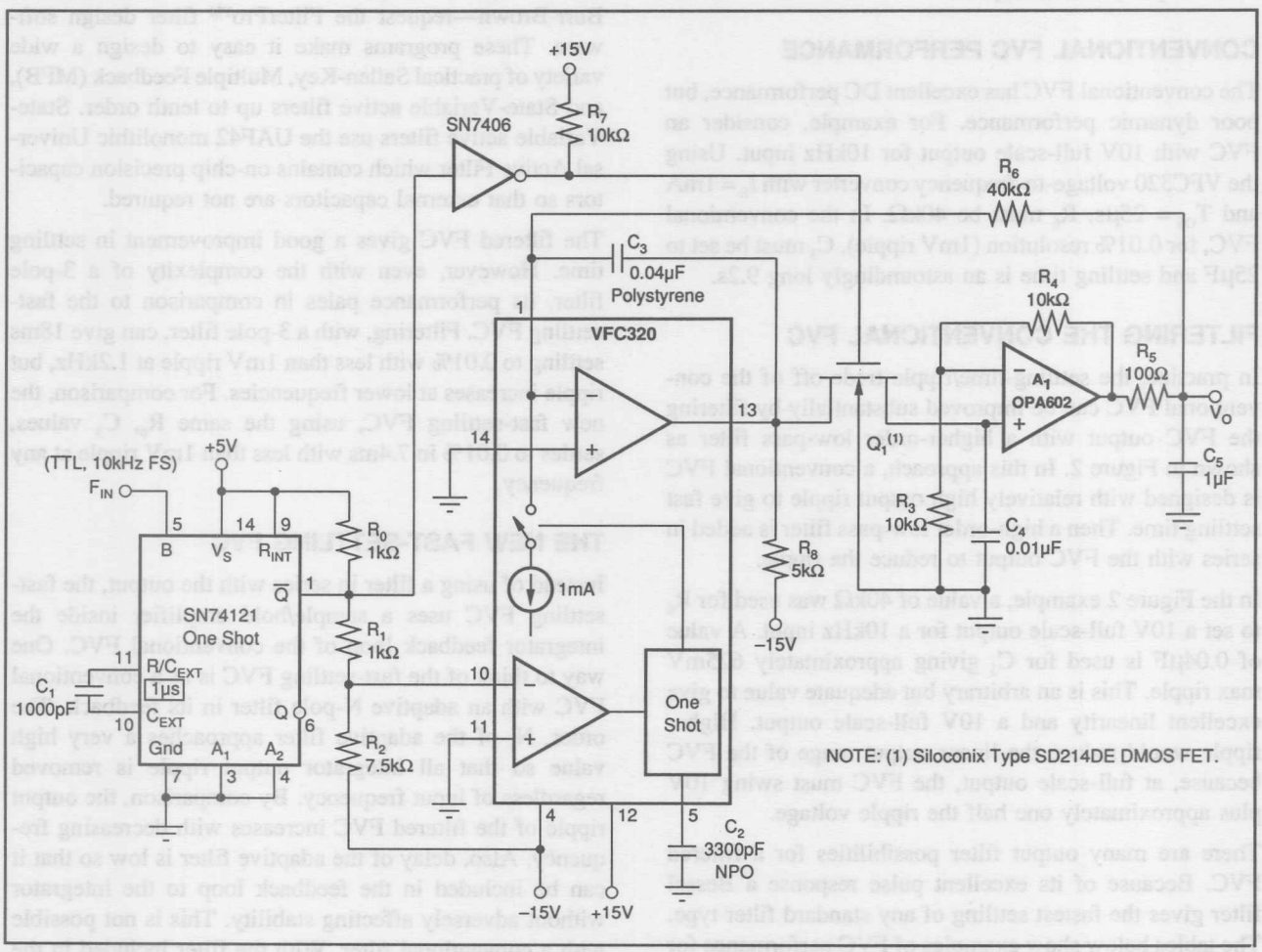


FIGURE 3. Fast-Settling Frequency-to-Voltage Converter. This converter is formed by adding a sample/hold in the feedback loop of the conventional FVC. It can settle to 0.01% in 7.4µs without ripple. Because the sample/hold is in the feedback loop, FVC precision is unaffected.

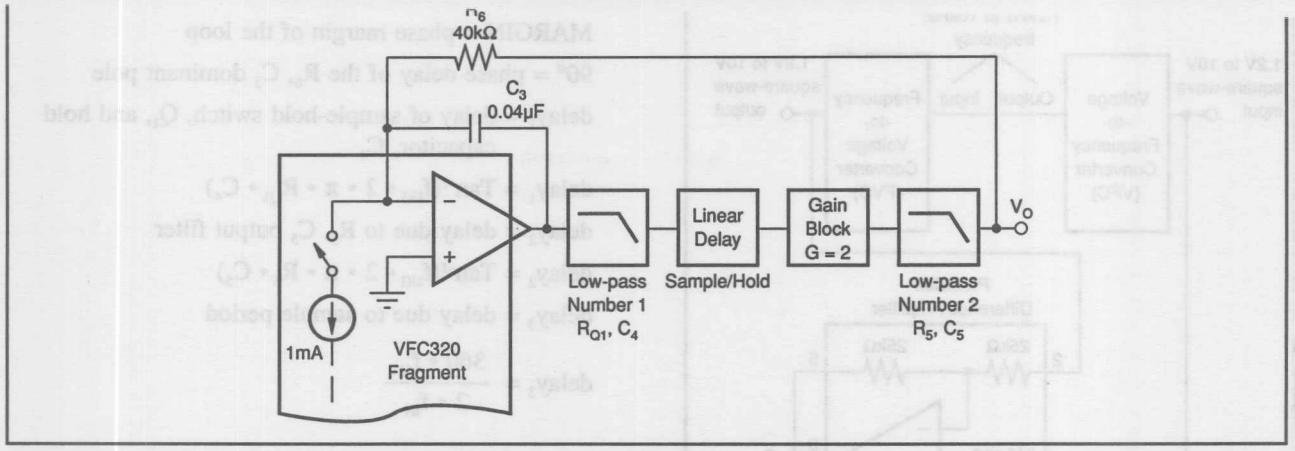


FIGURE 6. This Integrator Feedback-Loop Block Diagram can be Used for Stability Analysis of the Fast-Settling FVC.

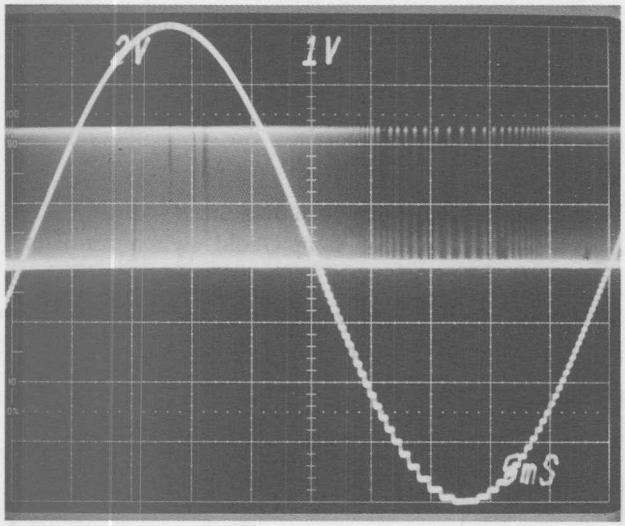


FIGURE 7. Dual-Trace Scope Photo Showing Frequency-to-Voltage Converter 1V to 9V Output for a 1kHz to 9kHz TTL-Level Frequency Input.

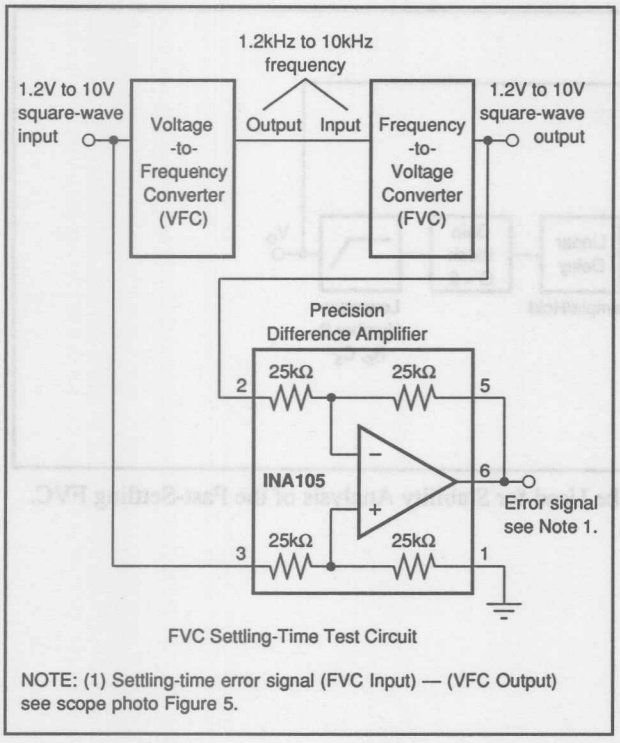


FIGURE 5A. FVC Settling-Time Measurement Circuit Used for Figure 5.

DISCUSSING STABILITY OF THE FAST-SETTLING FVC

Stability in sampled systems depends on sampling frequency. Since the sample/hold in the feedback loop of the fast-settling FVC is controlled by the input frequency, there is a minimum input frequency required to assure loop stability. As input frequency decreases, delay through the sample/hold increases thereby decreasing phase margin of the integrator loop. The feedback loop block diagram shown in Figure 6 gives a fairly accurate stability-criteria analysis. Phase margin of the loop is as follows:

$$MARGIN = 180° - 90° - delay_1 - delay_2 - delay_3$$

Where:

MARGIN = phase margin of the loop

90° = phase delay of the R_6, C_3 dominant pole

$delay_1$ = delay of sample-hold switch, Q_1, and hold capacitor, C_4

$delay_1 = Tan^{-1}(f_{UG} \cdot 2 \cdot \pi \cdot R_{Q1} \cdot C_4)$

$delay_2$ = delay due to R_5, C_5 output filter

$delay_2 = Tan^{-1}(f_{UG} \cdot 2 \cdot \pi \cdot R_5 \cdot C_5)$

$delay_3$ = delay due to sample period

$$delay_3 = \frac{360 \cdot f_{UG}}{2 \cdot f_{IN}}$$

f_{UG} = unity-gain frequency of the overall integrator loop

$f_{UG} = GAIN/(2 \cdot \pi \cdot R_6 \cdot C_3)$

GAIN = gain of the sample/hold circuit in the feedback loop

Solving for f_{IN},

(See Equation Below)

Where, in addition to previous definitions:

R_{Q1} = On-resistance of sample/hold switch-transistor, Q_1 [Ω]

Substituting the values from Figure 3, and using 25Ω for R_{Q1}, gives the following results:

MARGIN (°)	F_{IN} (Hz)
60	1200
45	780
30	600
0	400

For best pulse response and settling time the minimum input frequency should be 1.2kHz for the Figure 3 circuit example. At input frequencies below 400Hz, the loop will be unstable and the output will oscillate or lock-up.

$$f_{IN} = \frac{-90° \cdot Gain}{\pi \cdot C_3 \cdot R_6 \left(Margin \ -90° + \tan^{-1}\left(\frac{Gain \cdot R_5 \cdot C_5}{R_6 \cdot C_3} \right) + \tan^{-1}\left(\frac{Gain \cdot R_{Q1} \cdot C_4}{R_6 \cdot C_3} \right) \right)}$$

the FVC slew rate. The actual sample/hold gain is not critical. Because it is in the feedback loop, gain errors in the sample/hold circuit do not affect the gain of the FVC or degrade its accuracy.

FAST-SETTLING FVC PERFORMANCE

The fast-settling FVC has the same DC transfer function as the simple FVC, but with neglegable ripple at the output. Measured DC performance of the Figure 3 FVC circuit gave nonlinearity better than 10ppm (better than 16 bits).

The scope photo in Figure 4 shows the excellent small signal ±1V (actually +6V to +8V) output step response for the FVC with a 6kHz to 8kHz input frequency change. If phase margin were low, this signal would exhibit overshoot and ringing.

Settling time of the fast-settling time FVC approximates that predicted by a single-pole system boosted by the gain in the feedback loop:

$$T_S = \ln\left(\frac{100\%}{P\%}\right) \cdot R_6 \cdot C_3/GAIN$$

Where:

GAIN = Gain of sample/hold circuit in feedback loop of integrator [V/V]

With R_6 = 40kΩ, C_3 = 0.04µF, and GAIN = 2.0V/V as shown in Figure 3, 7.4ms settling to 0.01% is predicted. The scope photo in Figure 5 shows good agreement between theoretical and measured settling time for a large signal +1.2V to +10V output step due to a 1.2kHz to 10kHz input frequency change. The scope photo shows the residual error signal superimposed on the theoretical output signal. Each graticule division is approximately 0.01%.

The circuit used to measure settling time is shown in Figure 5A. A +1.2V to +10V square wave is applied to the input of both a VFC and to a precision difference amplifier. This square-wave input is the theoretical output signal—shown as one of the two traces on the scope photo Figure 5. The VFC converts the input voltage square wave into a modulated TTL-level 1.2kHz to 10kHz frequency signal. The frequency signal feeds directly into the FVC under test. The output of the FVC, ideally a delayed reproduction of the input square wave, feeds into the inverting input of the difference amplifier. The difference amplifier subtracts the FVC output from the VFC input. The output of the difference amplifier, (FVC output)-(VFC input) is the residual error signal—shown as the second trace on scope photo Figure 5. For this method to work, the VFC must have small dynamic error compared to the FVC. The VFC used in these measurements was the Burr-Brown VFC320.

Scope photo Figure 7 is a picture of a sine-wave modulated 1kHz to 9kHz TTL-level (0V to 5V) FVC input signal superimposed on the 1V to 9V FVC output. This photo was taken by driving a 1V to 9V sine-wave signal into the Figure 5A test circuit and looking at the FVC input and output. At the lower 1kHz frequency input, the steps between frequency input pulses can be seen on the sine-wave output showing excellent settling between pulses.

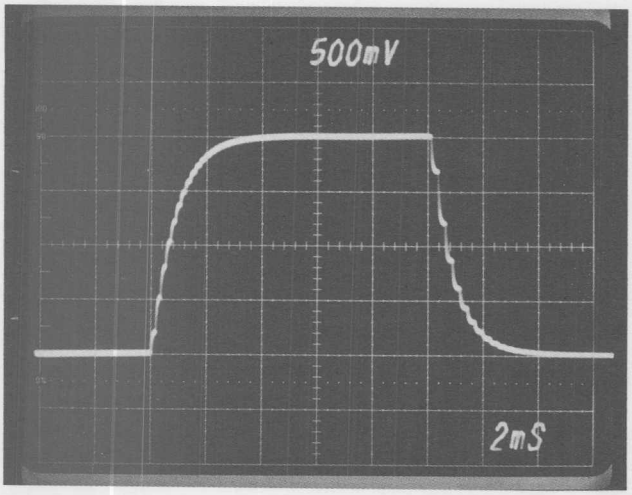


FIGURE 4. Small-Signal Step Response of the Fast-Settling FVC Shows Excellent Stability.

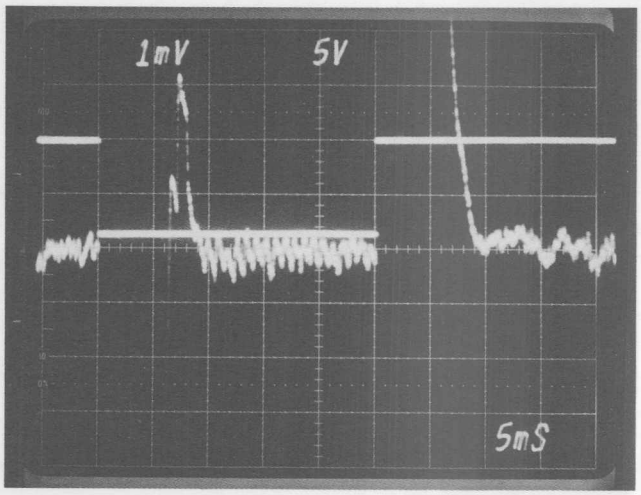
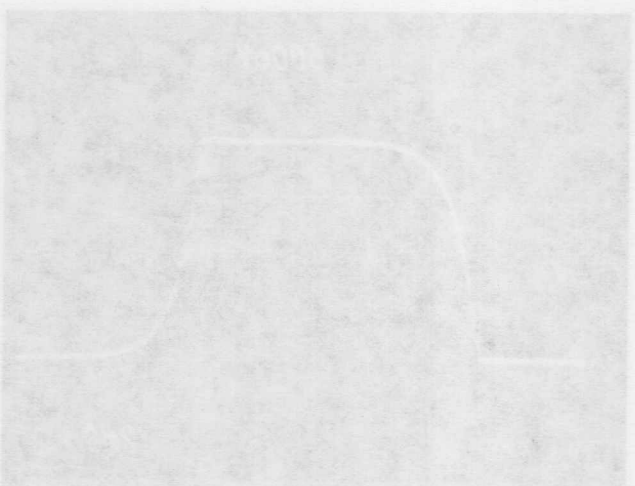


FIGURE 5. Settling Residue of the Fast-Settling FVC Confirms 0.01% Settling is Approximately 7.4ms.



HIGH SPEED DATA CONVERSION

By Mike Koen (602) 746-7337

INTRODUCTION

The design considerations for high-speed data conversion are, in many ways, similar to those for data conversion in general. High speed circuits may sometimes seem different because device types can be limited and only certain design techniques and architectures can be used with success. But the basics are the same. High speed circuits or systems are really those that tend to press the limits of state-of-the-art dynamic performance.

This bulletin focuses on the more fundamental building blocks such as op amps, sample/holds, digital to analog and analog to digital converters (DACs and ADCs). It concludes with test techniques. Op amps, which tend to be the basic building blocks of systems, are be considered first. Sample/holds which play an important role in data conversion are considered next followed by DACs and finally ADCs. ADCs are really a combination of the other three circuits. Emphasis is given to hybrid and monolithic design techniques since, in practice, the highest levels of performance are achieved using these processes. The material is presented from a design perspective. Theory and practical examples are offered so both the data conversion component designer and user will find the material useful. The concepts presented do not require extensive experience with data conversion. Fundamental concepts are discussed allowing the subject to be understood easily. The material emphasizes high speed circuit considerations—circuit theory is not treated in depth.

Topics Covered in this Bulletin

A. Amplifier Architectures
   1. Buffer
   2. Operational
   3. Open Loop
   4. Comparator

B. Amplifier Applications
   1. Sample/Hold
   2. Peak Detector

C. Digital to Analog Converters
   1. Bipolar
   2. Deglitched DAC

D. Analog to Digital Converters
   1. Successive Approximation
   2. Flash
   3. Sub-ranging

E. Test Techniques
   1. Settling Time
   2. Aperture Jitter
   3. Beat Frequency Testing
   4. Servo Loop Test

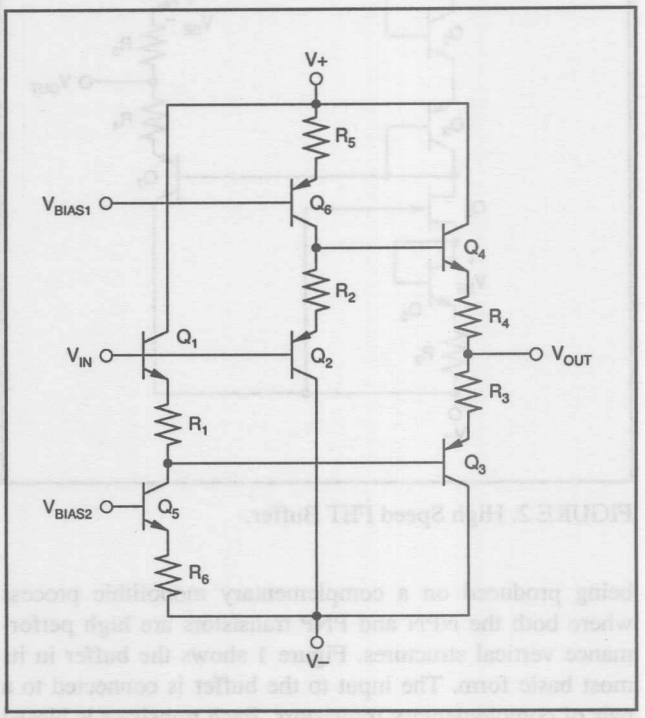


FIGURE 1. High Speed Bipolar Buffer.

AMPLIFIER ARCHITECTURES

Amplifiers of all types play an important role in data conversion systems. Since high speed amplifiers are both useful and difficult to design, an understanding of their operation is important. Four different types of amplifier architectures will be discussed. Buffers, op amps, open loop amplifiers, and comparators can be found in just about any signal processing application.

THE BUFFER

The open loop buffer is the ubiquitous modern form of the emitter follower. This circuit is popular because it is simple, low cost, wide band, and easy to apply. The open loop buffer is important in high speed systems. It serves the same purpose as the voltage follower in lower speed systems. It is often used as the output stage of wideband op amps and other types of broadband amplifiers. Consider the two buffer circuit diagrams, Figures 1 and 2. The output impedance of each buffer is about 5Ω and bandwidths of several hundred megahertz can be achieved. The FET buffer is usually implemented in hybrid form as very wideband FETs and transistors are usually not available on the same monolithic process. The all-bipolar form of the buffer is capable of

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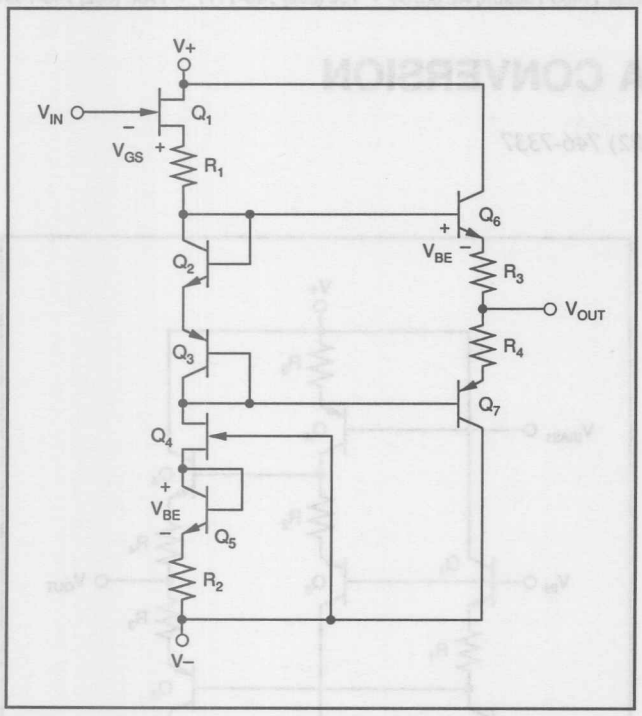


FIGURE 2. High Speed FET Buffer.

being produced on a complementary monolithic process where both the NPN and PNP transistors are high performance vertical structures. Figure 1 shows the buffer in its most basic form. The input to the buffer is connected to a pair of complementary transistors. Each transistor is biased by a separate current source. The input transistors Q_1 and Q_2 through resistors R_1 and R_2 are connected to the bases of output transistors Q_3 and Q_4 so that offset will be zero if the base to emitter voltage of the NPN and PNP are equal. Zero offset requires that transistor geometries are designed for equal V_{BE}s at the same bias current—achievable in a complementary process. This circuit is very useful as it has a moderately high input impedance and the ability to supply high current outputs. One important use of this buffer circuit is to amplify the output current of a monolithic op amp. Monolithic op amps usually do not have output currents that exceed 10mA to 50mA, while the buffer shown in Figure 1 is capable of putting out more than 100mA. Typically this type of a buffer has a bandwidth of 250MHz, allowing it to be used in the feedback loop of most monolithic op amps with minimal effect on stability. Figure 3 shows how the loop is closed around the buffer so that the DC performance of the amplifier is determined by the unbuffered amplifier and not the output buffer. An advantage of the connection shown in Figure 3 is that load-driving heat dissipating is in the buffer so that thermally induced distortion and offset drift is removed from the sensitive input op amp.

Figure 2 shows the FET version of the previously mentioned circuit. The FET buffer achieves zero offset by the mirror action of the NPN transistor Q_5 that is reflected as the gate

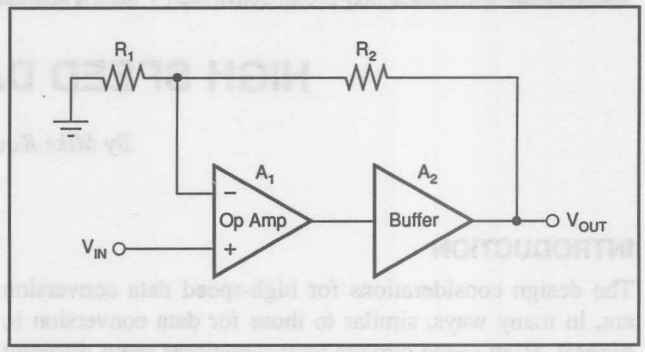


FIGURE 3. High Current Op Amp.

to source voltage of the input FET Q_1. The V_{BE} of Q_5 determines the gate to source voltage of the FET current source Q_4. Since the identical current flows in Q_4 and Q_1 the gate to source voltage of Q_1 will also be equal to V_{BE}. Since Q_5 and Q_6 are identical transistors the offset of the FET buffer circuit will be nominally zero. The circuit shown in Figure 2 is usually constructed in hybrid form so that it is usually necessary to adjust resistors R_1 and R_2 to set the offset of this circuit to zero. Setting the offset to zero is accomplished by laser-trimming resistors R_1 and R_2 with the buffer under power. (This is known as active trimming.) A common application of this circuit is to buffer the hold capacitor in a sample/hold. (See the section on sample/holds.) The high impedance of the FET buffer allows the capacitor to retain the sample voltage for a comparatively long time as the room temperature input current of a typical FET is in the vicinity of 50pA.

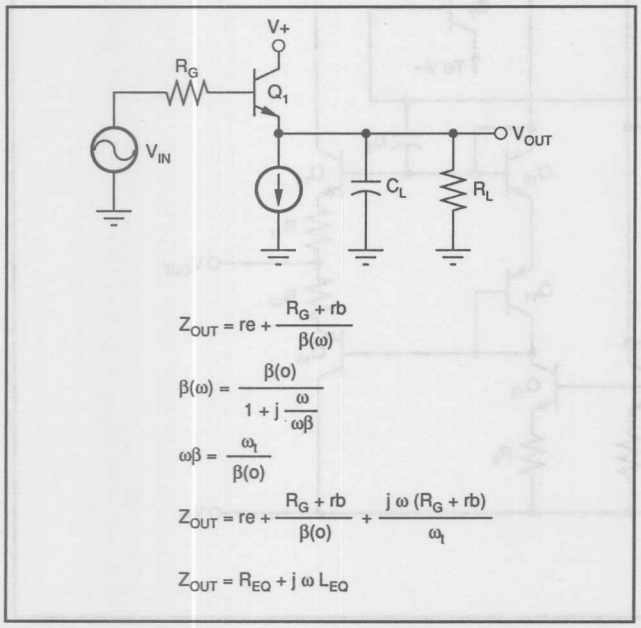
Another common application of either type of buffer circuit is to drive high capacitive loads without reducing the overall system bandwidth. Op amps, even though they have closed loop output impedances that are very low, can become unstable in the presence of high capacitive loads. The open loop buffer is usually more stable when driving capacitive loads, but this circuit will also develop a tendency to ring if the capacitive load becomes excessive. Figure 4 shows how the emitter follower can oscillate due to reactive output impedance. Figures 5 through 7 show calculated results for different conditions when a simple emitter follower is driving a capacitive load which illustrates this oscillatory tendency.

One very important application of the open loop buffer is to drive a "back matched" transmission cable. Back matching a cable is just as effective in preventing reflections as the more conventional method of terminating the cable at the receiving end. The advantage of the back matched cable is that the generating circuit does not have to supply steady-state current and there is no loss of accuracy due to the temperature dependent copper loss of the cable. Figure 8 shows circuit diagrams and explanations that describe the operation of the open loop buffer driving a "back matched" cable.

THE OPERATIONAL AMPLIFIER

Several examples will be shown that depict the architecture of wideband op amps. These amplifiers have settling times to ±0.01% in under 100ns and closed loop bandwidths in excess of 100MHz. The question is often asked, "How much loop gain is enough?" Wideband amplifiers generally do not achieve as much open loop gain as lower frequency amplifiers. This is the result of optimization of bandwidth and phase margin. If open loop gain is stable over temperature and linearity with signal adequate, the requirement for high open loop gain is reduced. This is important since it is difficult to achieve high open loop gain for wideband amplifiers.

There are several ways to shape the open-loop-gain/phase characteristics, or Bode Plot, of an amplifier. The method chosen depends on whether high slew rate or fast settling is to be emphasized. The methods of stabilizing the closed-loop gain of these amplifiers will also result in different settling time characteristics. The benefits of each of these methods will be explained. The first amplifier has a FET input and the other has a bipolar input. High speed amplifiers should be designed to drive 50Ω loads to be most useful. 50Ω cable is commonly used in high speed systems to interconnect signals.



$$Z_{OUT} = re + \frac{R_G + rb}{\beta(\omega)}$$

$$\beta(\omega) = \frac{\beta(o)}{1 + j\frac{\omega}{\omega\beta}}$$

$$\omega\beta = \frac{\omega_t}{\beta(o)}$$

$$Z_{OUT} = re + \frac{R_G + rb}{\beta(o)} + \frac{j\,\omega\,(R_G + rb)}{\omega_t}$$

$$Z_{OUT} = R_{EQ} + j\,\omega\,L_{EQ}$$

FIGURE 4. Output Impedance of Emitter Follower.

$$\frac{V_{OUT}}{V_{IN}} = 1 - \left[\frac{k}{(1-k^2)^{1/2}} \sin 2\pi\,(1-k^2)^{\frac{1}{2}}\frac{t}{T} + \cos 2\pi\,(1-k^2)^{\frac{1}{2}}\frac{t}{T}\right] e^{-2\pi k(t/T)}$$

where: $T = 2\pi\,(L_{EQ} \cdot C_L)^{\frac{1}{2}}$

$$k = \left[\frac{R_{EQ}}{L_{EQ}} + \frac{1}{R_L C_L}\right]\frac{T}{4\pi}$$

$$R_{EQ} = re + \frac{R_G + rb}{\beta(o)}$$

$$L_{EQ} = \frac{R_G + rb}{\omega T}$$

FIGURE 5. Time Response.

f_T = 1GHz	f_T = 5GHz	f_T = 5GHz
R_G = 50Ω	R_G = 50Ω	R_G = 50Ω
rb = 50	rb = 50	rb = 50
re = 5	re = 5	re = 5
C_L = 50pF	C_L = 50pF	C_L = 50pF
β(o) = 100	β(o) = 100	β(o) = 100
k = 0.35	k = 0.44	k = 0.51
T = 5.6ns	T = 4.7ns	T = 1.9ns

FIGURE 6. Different Conditions.

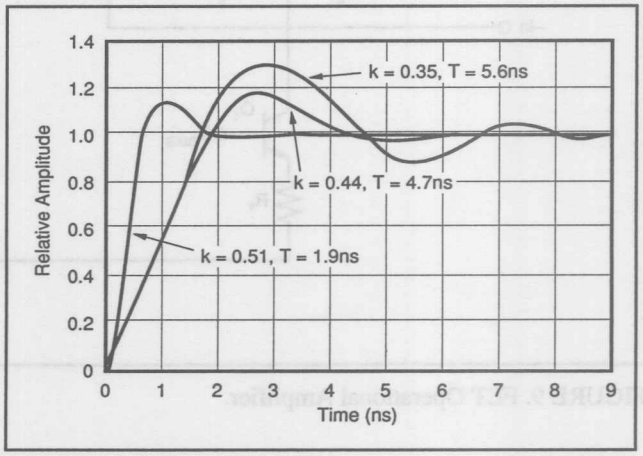


FIGURE 7. Results.

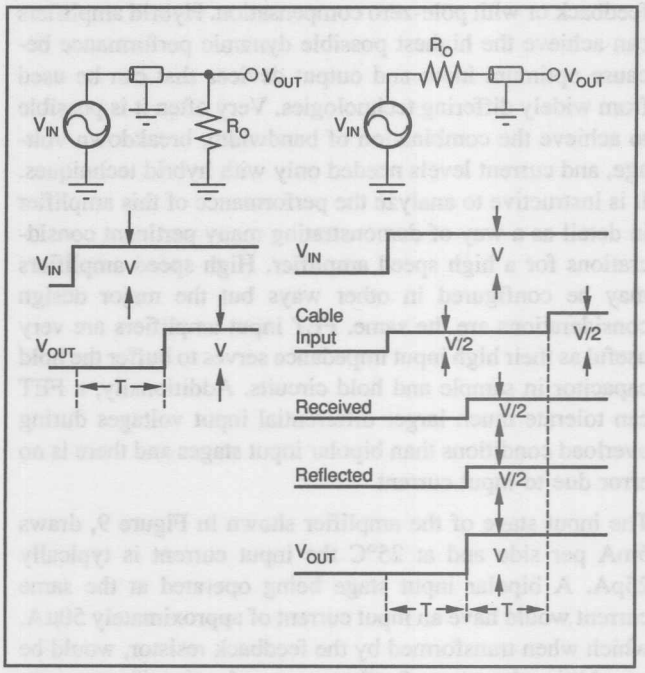


FIGURE 8. Back Matched Cable.

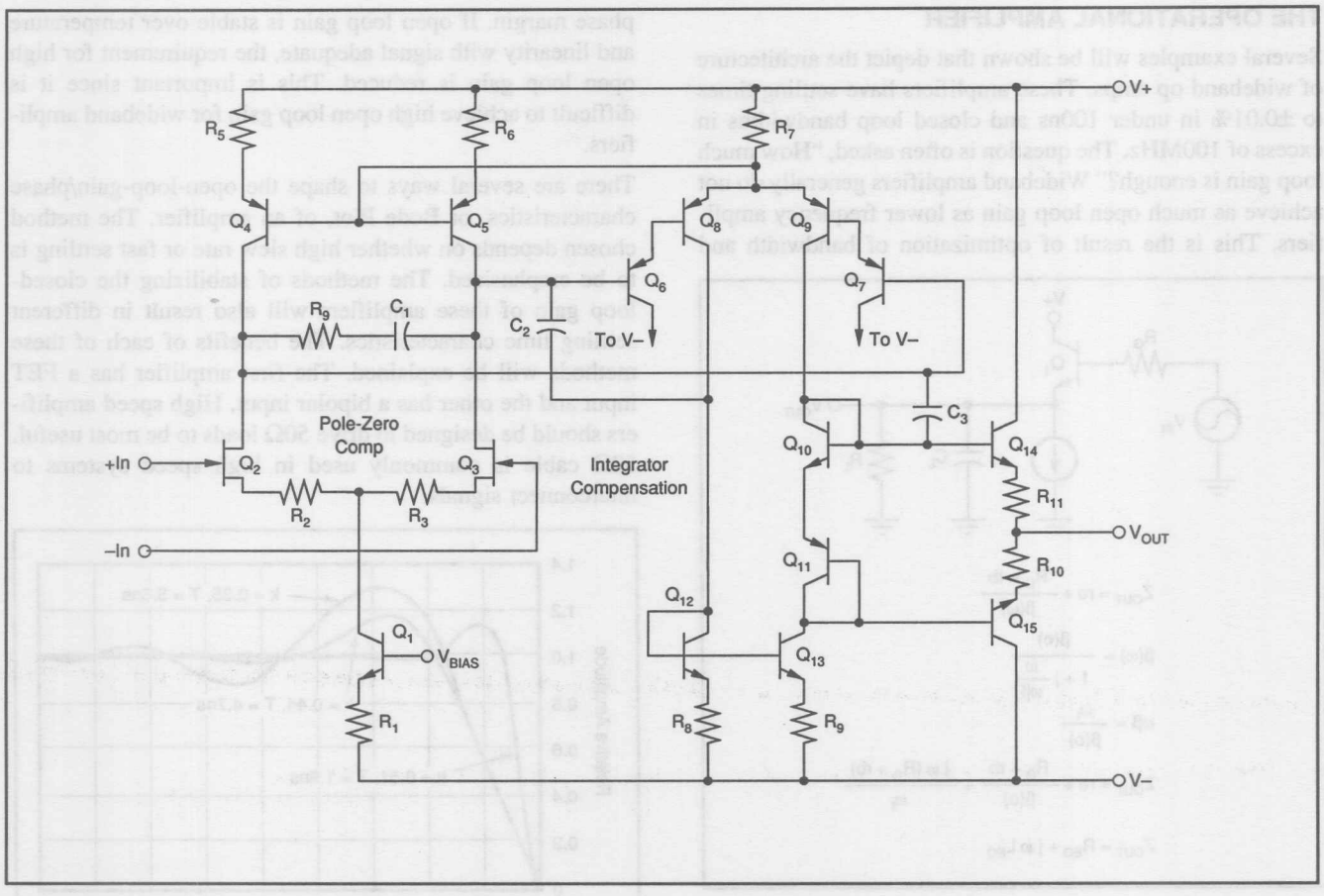


FIGURE 9. FET Operational Amplifier.

Consider a classic two stage hybrid amplifier as shown in Figure 9. It can be compensated either with integrator feedback or with pole-zero compensation. Hybrid amplifiers can achieve the highest possible dynamic performance because optimum input and output devices that can be used from widely differing technologies. Very often it is possible to achieve the combination of bandwidth, breakdown voltage, and current levels needed only with hybrid techniques. It is instructive to analyze the performance of this amplifier in detail as a way of demonstrating many pertinent considerations for a high speed amplifier. High speed amplifiers may be configured in other ways but the major design considerations are the same. FET input amplifiers are very useful as their high input impedance serves to buffer the hold capacitor in sample and hold circuits. Additionally, a FET can tolerate much larger differential input voltages during overload conditions than bipolar input stages and there is no error due to input current.

The input stage of the amplifier shown in Figure 9, draws 5mA per side and at 25°C the input current is typically 25pA. A bipolar input stage being operated at the same current would have an input current of approximately 50μA, which when transformed by the feedback resistor, would be an additional source of offset error and noise. To compensate for the low gain of the input stage (G = 25) it is desirable to maintain a differential connection between the first and second stages. When a connection of this type is made it is necessary to establish the operating point of the input stage using "common mode" feedback. Assuming that FET pair Q_2 and Q_3 are well-matched, the current is split evenly and emerges as equal collector current for transistors Q_4 and Q_5. The bases of Q_4 and Q_5 are connected together and applied to the common connection of the emitters of PNP transistors Q_8 and Q_9. Therefore, in order to establish balance in the loop, a voltage is created across R_7 of such a magnitude to allow the current in transistors and Q_4 to be a value that will exactly balance the current needed by FETs Q_2 and Q_3. Transistors Q_8 and Q_9 a driven from a pair of emitter followers to increase the overall loop gain. Emitter follower transistors Q_6 and Q_7 increase the gain of the first stage by preventing transistors Q_8 and Q_9 from loading the drains of the input FET pair. The differential output of transistors Q_8 and Q_9 are then connected to the output emitter followers directly and through the mirroring action of transistors Q_{12} and Q_{13}. The overall DC gain of this amplifier is 94dB. The current through the output emitter follower is established by the biasing action of the diode connected transistors Q_{10} and Q_{11}. The offset voltage of this amplifier is trimmed to under 1mV and the amplifier has a voltage offset drift coefficient of less than 10μV/°C.

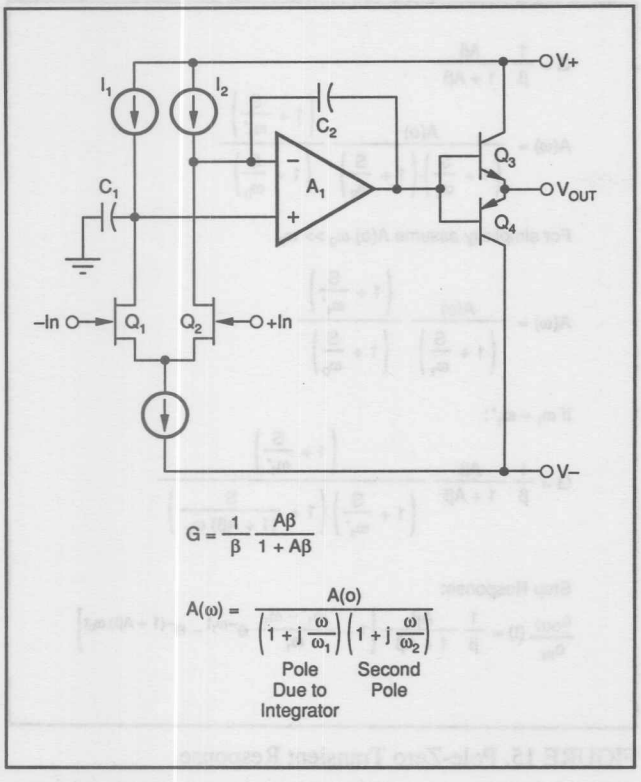


FIGURE 10. Integrator Compensation.

As previously mentioned, there are two methods for compensating the open loop frequency response of this amplifier. The first method to be discussed is called integrator feedback as a capacitor is connected from the output stage to the drain of the input stage. Figure 10 shows a block diagram of this connection which more clearly demonstrates why it is called integrator compensation as an integrator is formed around the output gain stage of the amplifier. The advantage of integrator feedback is that the closed loop frequency response has all the poles in the denominator which means that the transient response is tolerant to parameter variation. As will be shown, another type of frequency compensation is called "doublet" or "pole-zero cancellation" which can have poor transient response due to small parameter variations. Another benefit of integrator feedback is lower noise output as the integrator forms an output filter as contrasted to pole-zero cancellation which only forms an incomplete filter of the input stage. Figures 11 and 12 show the relationship between the frequency and time or transient response of a feedback amplifier that employs integrator feedback.

Figures 13 through 16 illustrate the effect of a pole-zero mismatch. A pole-zero mismatch creates a "tail" or a long time constant settling term in the transient response. Pole-zero compensation is not as effective as integrator feedback in stabilizing an amplifier but should be considered as there are times when the integrator itself can become unstable. Pole-zero compensated amplifiers often have higher slew rates.

The second architecture that will be discussed is known as

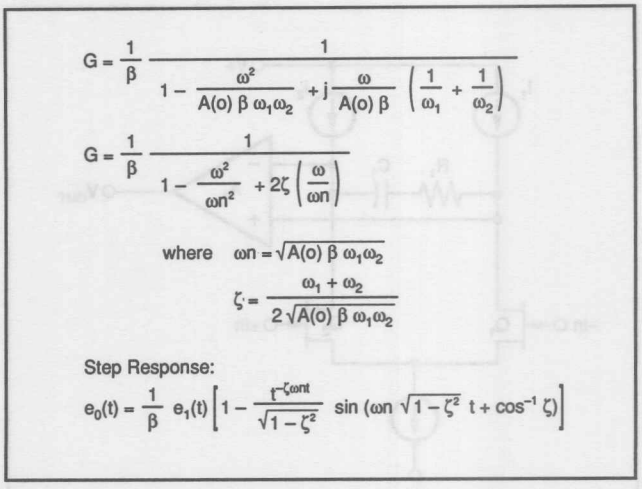


FIGURE 11. Transient Response Integrator Compensation.

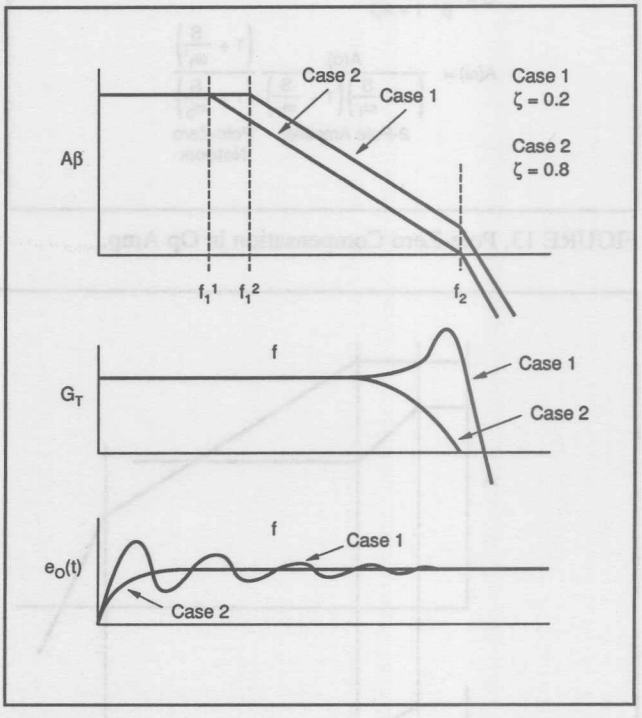
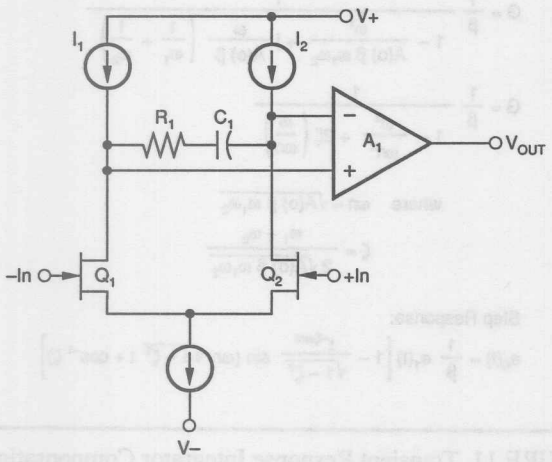


FIGURE 12. Open Loop Gain, Closed Loop Gain, and Transient Response Integrator Compensation.

the folded cascode operational amplifier. This circuit arrangement is very useful as all the open loop gain is achieved in a single stage. Since all of the gain is developed in a single stage, higher usable gain bandwidth product will result as the Bode Plot will tend to look more like a single pole response which implies greater stability.

Figure 17 shows a simplified schematic of this type of amplifier. The input terminals of this amplifier are the bases of transistors Q_1 and Q_2. The output of transistors Q_1 and Q_2 are taken from their respective collectors and applied to the emitters of the common base PNPs Q_4 and Q_5. Transistors Q_4 and Q_5 act as cascode devices reducing the impedance at



$$G = \frac{1}{\beta}\,\frac{A\beta}{1 + A\beta}$$

$$A(\omega) = \frac{A(o)}{\left(1 + \frac{S}{\omega_1}\right)\left(1 + \frac{S}{\omega_1}\right)}\,\frac{\left(1 + \frac{S}{\omega_1'}\right)}{\left(1 + \frac{S}{\omega_0}\right)}$$

2-Pole Amplifier — Pole-Zero Network

FIGURE 13. Pole-Zero Compensation in Op Amp.

$$G = \frac{1}{\beta}\,\frac{A\beta}{1 + A\beta}$$

$$A(\omega) = \frac{A(o)}{\left(1 + \frac{S}{\omega_1}\right)\left(1 + \frac{S}{\omega_2}\right)}\,\frac{\left(1 + \frac{S}{\omega_1'}\right)}{\left(1 + \frac{S}{\omega_0}\right)}$$

For simplicity assume $A(o)\ \omega_0 >> \omega_2$.

$$A(\omega) = \frac{A(o)}{\left(1 + \frac{S}{\omega_1}\right)}\,\frac{\left(1 + \frac{S}{\omega_1'}\right)}{\left(1 + \frac{S}{\omega_0}\right)}$$

If $\omega_1 \approx \omega_1'$:

$$G = \frac{1}{\beta}\,\frac{A\beta}{1 + A\beta}\,\frac{\left(1 + \frac{S}{\omega_1'}\right)}{\left(1 + \frac{S}{\omega_1'}\right)\left(1 + \frac{S}{(1 + A\beta)\,\omega_0}\right)}$$

Step Response:

$$\frac{e_{OUT}}{e_{IN}}(t) = \frac{1}{\beta}\,\frac{A\beta}{1 + A\beta}\left[1 - \frac{\omega_1' - \omega_1}{\omega_1}\,e^{-\omega_1 t} - e^{-(1 + A\beta)\,\omega_0 t}\right]$$

FIGURE 15. Pole-Zero Transient Response.

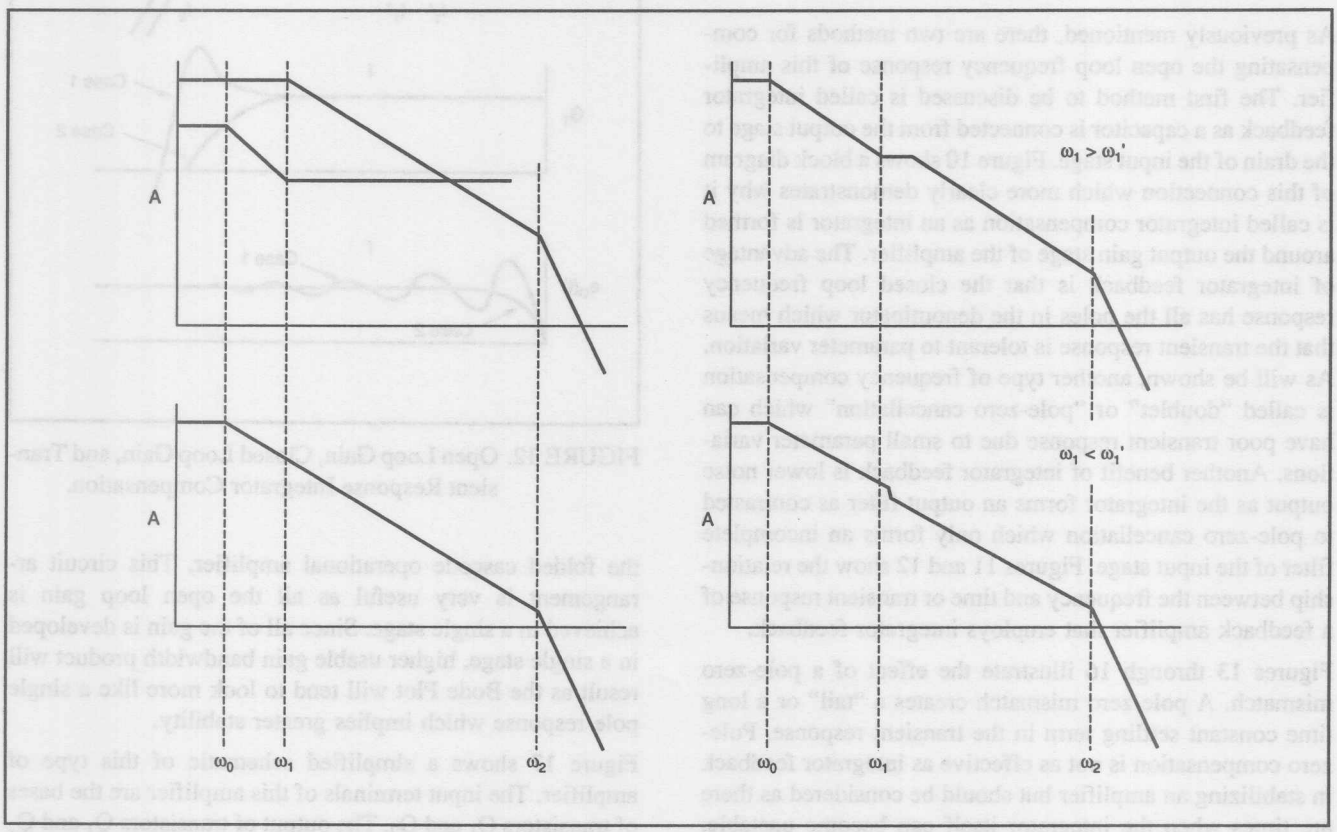


FIGURE 14. Pole-Zero Compensation Bode Plots.

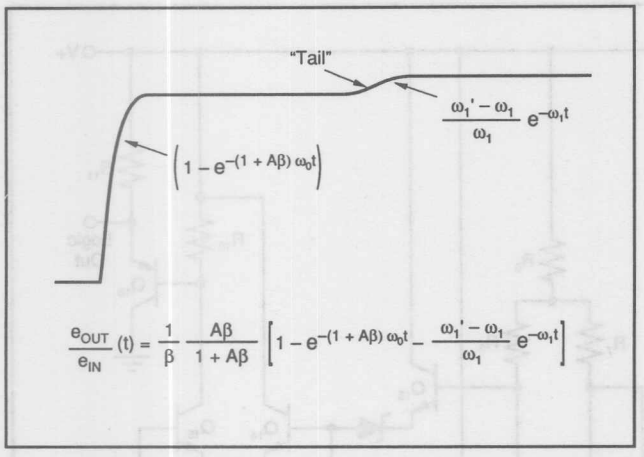


FIGURE 16. Pole-Zero Transient Response and Pole-Zero Mismatch.

the collectors of Q_1 and Q_2 while allowing the signal current to pass through transistors Q_4 and Q_5 with little attenuation. The term "folded cascode" refers to the fact that the PNP transistors not only serve as cascoding devices but also "fold" the signal down to a load connected to the negative power supply. Transistors Q_8 and Q_9 act as current source loads for transistors Q_4 and Q_5 thereby enabling the amplifier to achieve gains of up to 80 in a single stage. Emitter followers drive the output load in a similar manner to the method described for the FET operational amplifier. An additional benefit of this architecture is that the amplifier can be stabilized with a single capacitor thereby approximating a single pole response without a settling "tail."

COMPARATOR

The comparator is a common element in a signal processing system and it is used to sense a level and then generate a digital signal, either a "1" or a "0," to report the result of that comparison to the rest of the system. Comparators can be implemented two different ways, either using a high gain amplifier or by using the latching type approach. Each type of comparator has advantages as will now be explained.

When a high gain amplifier is used as a comparator, many low gain stages are cascoded to achieve high gain bandwidth product. A simplified example of a 20ns comparator is shown in Figure 18. This is in contrast to the way a wideband operational amplifier would be designed. A design objective for a wideband operational amplifier would be to achieve high gain in a single stage to avoid accumulating an excessive amount of phase shift. Feedback will be applied around an operational amplifier. It is important to achieve a phase characteristic approaching single pole response. Phase shift through a comparator is usually not important although high bandwidth and low propagation delay is desirable. The design of an open loop amplifier and a comparator are similar. The main differences are that comparators do not have to have stable, or linear, gain characteristics and the output is designed to be logic compatible such as TTL or ECL. Unlike a linear open loop amplifier, a comparator is

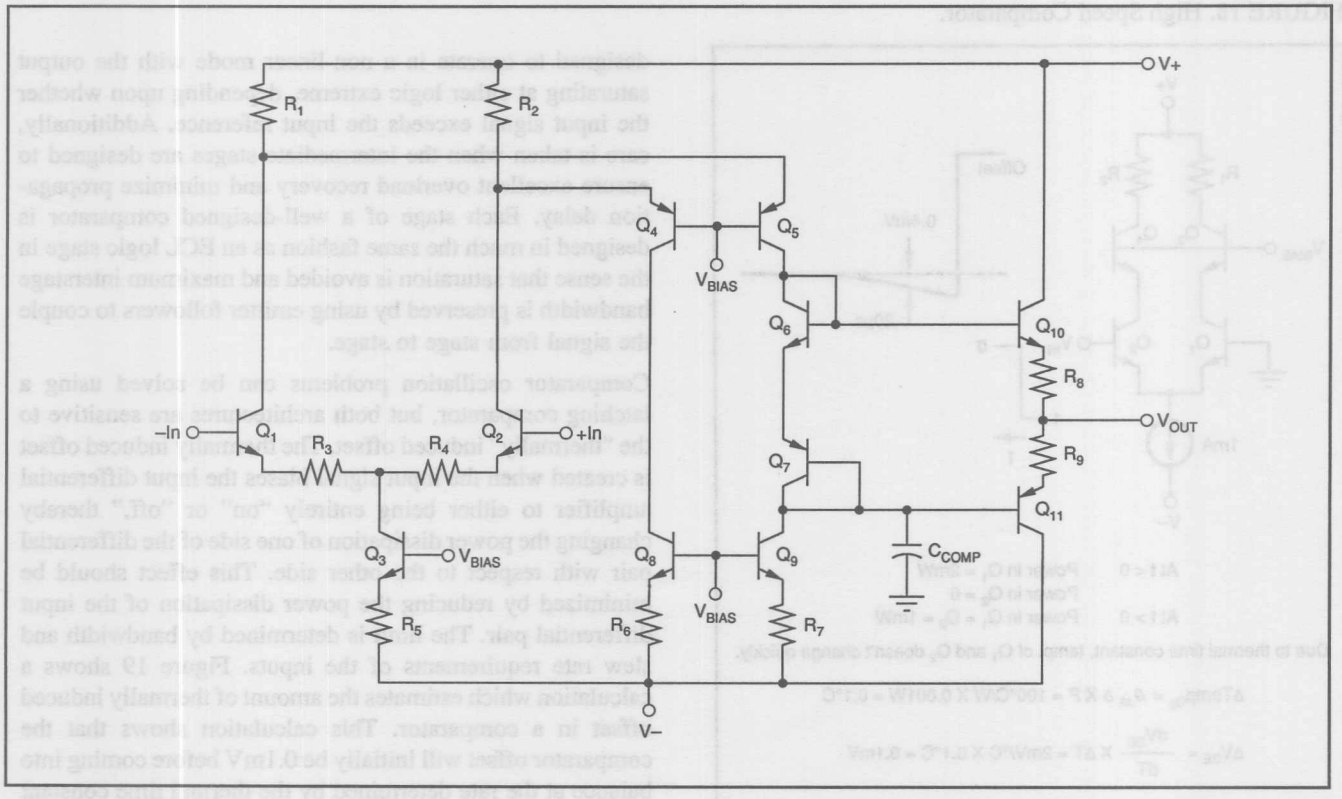


FIGURE 17. Folded Cascode.

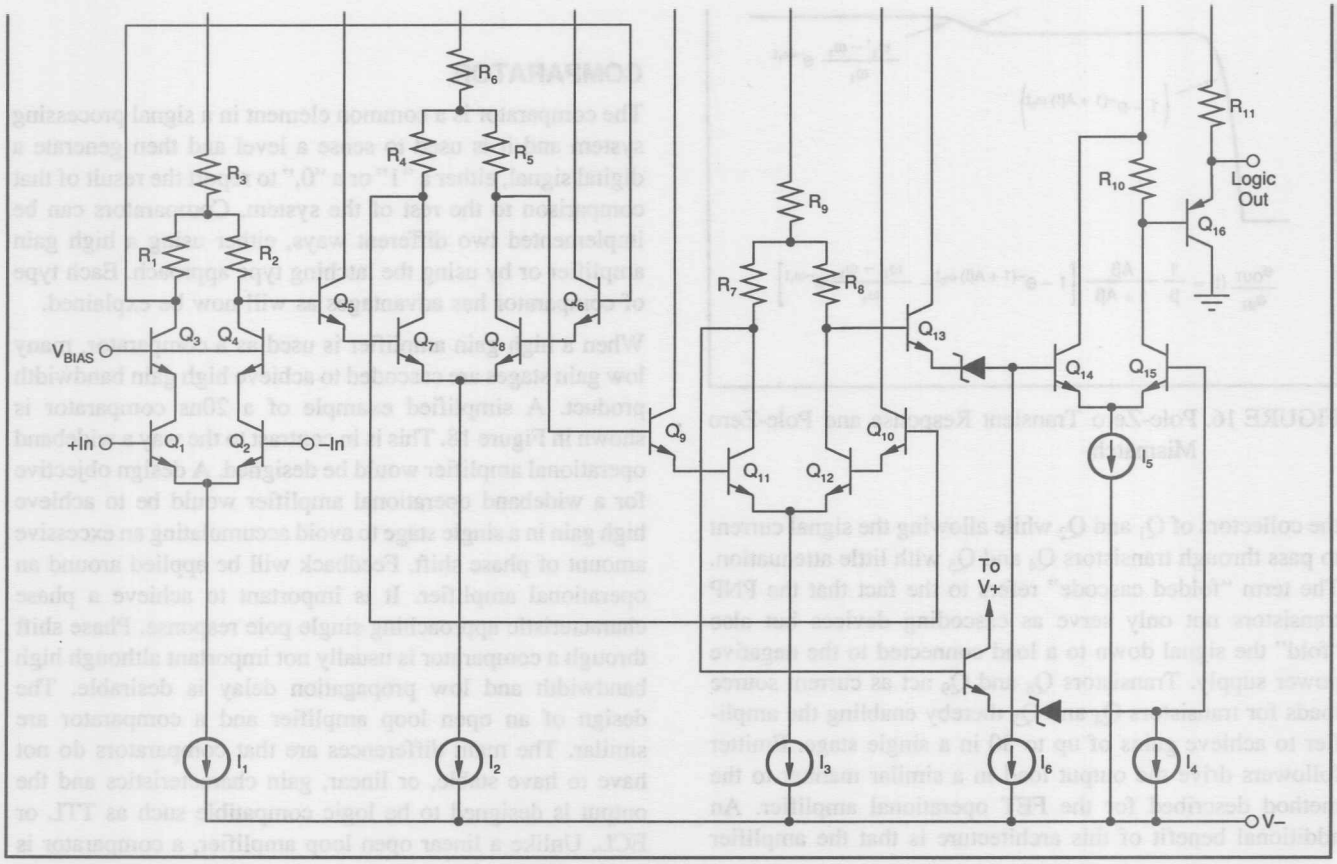


FIGURE 18. High Speed Comparator.

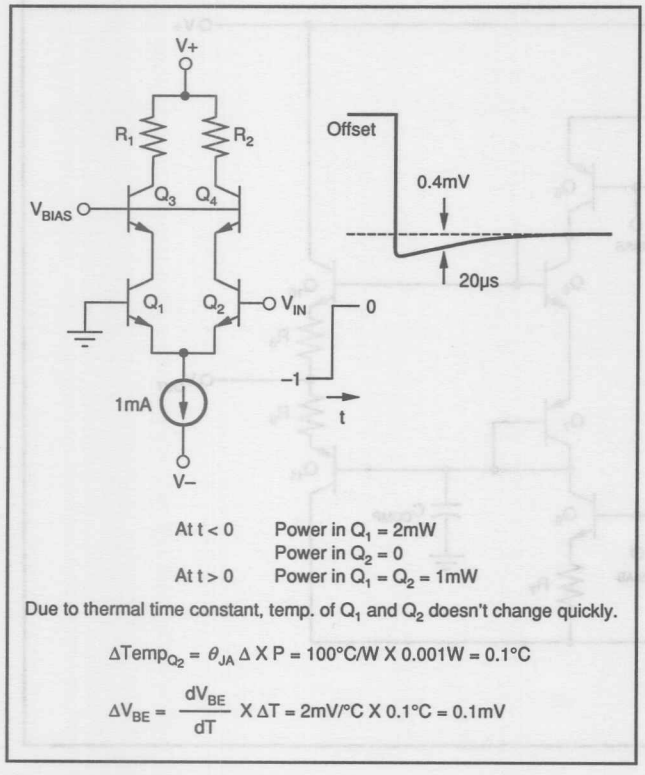


FIGURE 19. Thermal Offset.

designed to operate in a non-linear mode with the output saturating at either logic extreme, depending upon whether the input signal exceeds the input reference. Additionally, care is taken when the intermediate stages are designed to ensure excellent overload recovery and minimize propagation delay. Each stage of a well-designed comparator is designed in much the same fashion as an ECL logic stage in the sense that saturation is avoided and maximum interstage bandwidth is preserved by using emitter followers to couple the signal from stage to stage.

Comparator oscillation problems can be solved using a latching comparator, but both architectures are sensitive to the "thermally" induced offset. The thermally induced offset is created when the input signal biases the input differential amplifier to either being entirely "on" or "off," thereby changing the power dissipation of one side of the differential pair with respect to the other side. This effect should be minimized by reducing the power dissipation of the input differential pair. The limit is determined by bandwidth and slew rate requirements of the inputs. Figure 19 shows a calculation which estimates the amount of thermally induced offset in a comparator. This calculation shows that the comparator offset will initially be 0.1mV before coming into balance at the rate determined by the thermal time constant of the system. The thermal time constant of the system is in

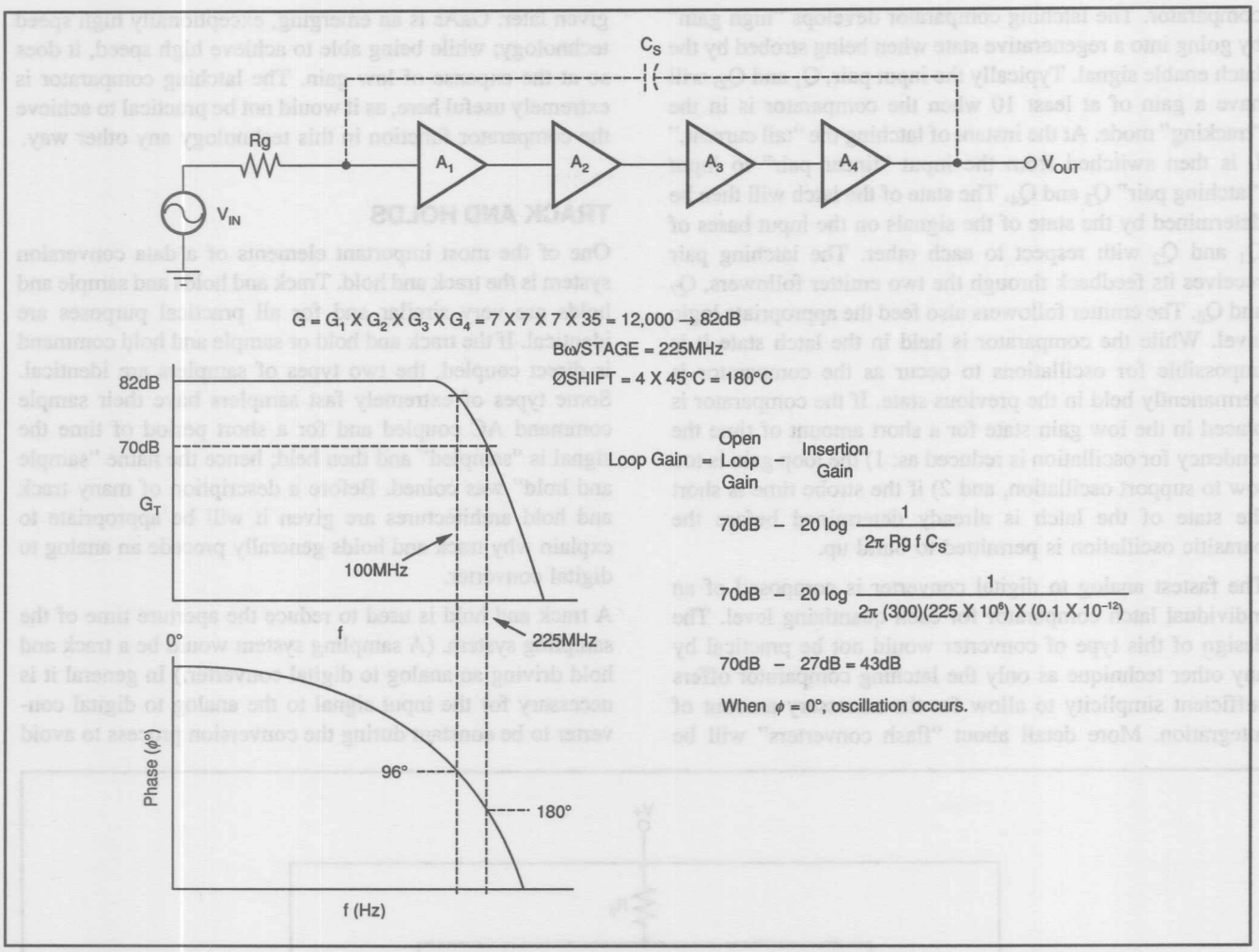


FIGURE 20. Comparator Oscillation.

the order of 10µs to 100µs and is affected by factors such as the physical size of the transistor as well as the method by which the transistor die is attached to the header. Thermally induced offset can become a serious problem in high speed, high accuracy systems and can often be the limiting factor that determines performance.

The other effect that limits the accuracy of the non-latched comparator is the tendency for oscillations. Comparator oscillations are usually due to parasitic feedback from the output signal being capacitively coupled back to the comparator's input. In discrete form this problem is very difficult to solve while still trying to maintain high sensitivity and low propagation delay. Figures 20 and 21 show a diagram which describes how the parasitic feedback between the pins of the package comparator can create enough feedback to stimulate an oscillation. Even in hybrid form, comparator oscillation is a serious problem. Integrating the comparator onto a monolithic chip is beneficial as the planar nature of this means of construction will reduce the amount of parasitic capacitance.

As previously mentioned, the other type of comparator that is employed is known as the "latching type." Figure 22 shows a simplified schematic of the front end of this type of

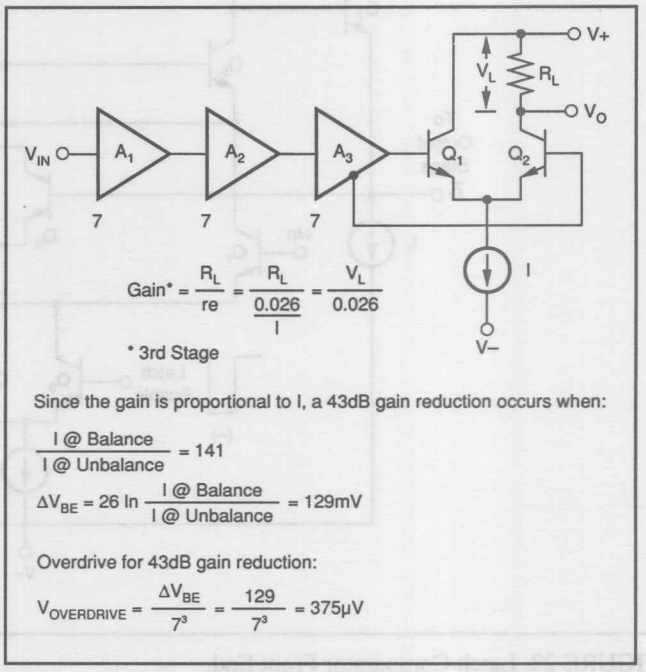


FIGURE 21. Gain Reduction to Stop Comparator Oscillation.

comparator. The latching comparator develops "high gain" by going into a regenerative state when being strobed by the latch enable signal. Typically the input pair, Q_1 and Q_2, will have a gain of at least 10 when the comparator is in the "tracking" mode. At the instant of latching the "tail current," I, is then switched from the input "linear pair" to input "latching pair" Q_3 and Q_4. The state of the latch will then be determined by the state of the signals on the input bases of Q_1 and Q_2 with respect to each other. The latching pair receives its feedback through the two emitter followers, Q_7 and Q_8. The emitter followers also feed the appropriate logic level. While the comparator is held in the latch state it is impossible for oscillations to occur as the comparator is permanently held in the previous state. If the comparator is placed in the low gain state for a short amount of time the tendency for oscillation is reduced as: 1) the loop gain is too low to support oscillation, and 2) if the strobe time is short the state of the latch is already determined before the parasitic oscillation is permitted to build up.

The fastest analog to digital converter is composed of an individual latch comparator for each quantizing level. The design of this type of converter would not be practical by any other technique as only the latching comparator offers sufficient simplicity to allow for the necessary amount of integration. More detail about "flash converters" will be given later. GaAs is an emerging, exceptionally high speed technology; while being able to achieve high speed, it does so at the expense of low gain. The latching comparator is extremely useful here, as it would not be practical to achieve the comparator function in this technology any other way.

TRACK AND HOLDS

One of the most important elements of a data conversion system is the track and hold. Track and holds and sample and holds are very similar and for all practical purposes are identical. If the track and hold or sample and hold command is direct coupled, the two types of samplers are identical. Some types of extremely fast samplers have their sample command AC coupled and for a short period of time the signal is "sampled" and then held; hence the name "sample and hold" was coined. Before a description of many track and hold architectures are given it will be appropriate to explain why track and holds generally precede an analog to digital converter.

A track and hold is used to reduce the aperture time of the sampling system. (A sampling system would be a track and hold driving an analog to digital converter.) In general it is necessary for the input signal to the analog to digital converter to be constant during the conversion process to avoid

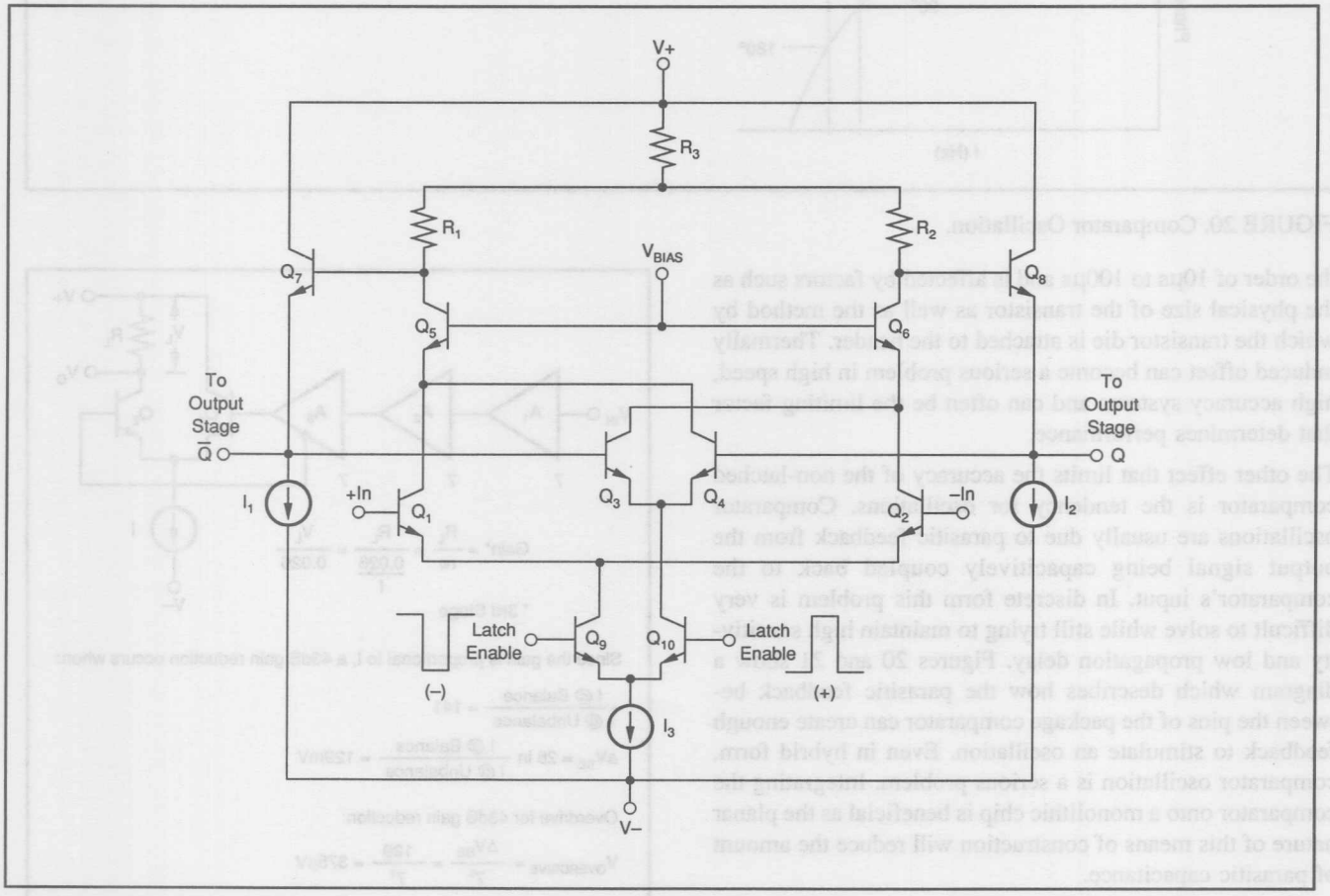


FIGURE 22. Latch Comparator Front End.

$$e(t) = \frac{EFS}{2} \sin 2\pi ft$$

EFS = Full Scale ADC Range

$$\frac{d\,e(t)}{dt} = f\,EFS\,\pi \cos 2\pi ft, \quad \frac{d\,e(t)}{dt} = f\,EFS\,\pi$$

$$f = \frac{\frac{d\,e(t)}{dt}}{EFS\,\pi}$$

Assume maximum allowable change during ADC conversion time.

T = 1/2LSB and EFS = 2^NLSB where N is the number of bit ADC.

$$f = \frac{1/2LSB}{T\,2^N LSB\,\pi} = \frac{1}{\pi\,2^{(N+1)}\,T}$$

As an example, let N = 12 and T = 1µs:

$$f_{MAX} = \frac{1/2LSB}{T\,2^N LSB\,\pi} = 38.9Hz$$

With a sample/hold, the maximum frequency would be 500kHz.

FIGURE 23. Maximum Input Frequency for ADC Without a Sample/Hold.

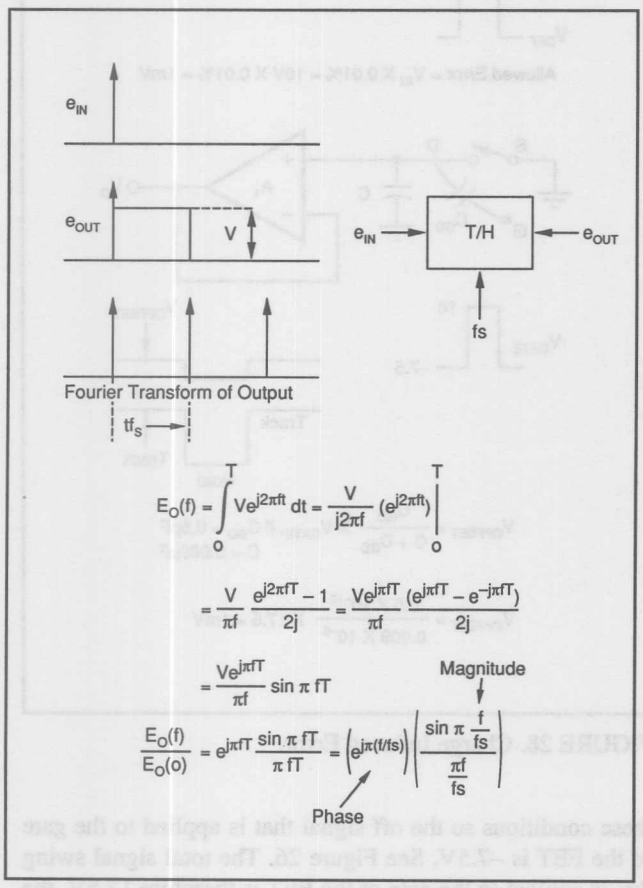


FIGURE 24. Track/Hold Bandwidth.

error. A successive approximation ADC uses an N-step algorithm when forming the conversion and if the signal varies during the conversion process the wrong approximation would take place. Even flash converters can benefit from being driven from a track and hold since the time delays of all the comparators are not identical. Figure 23 calculates the improvement in ADC performance that can be obtained when a track and hold precedes an ADC. Figure 23 shows that the maximum frequency that can be processed by a 1µs ADC would be only 38.9Hz. When a sample and hold drives the ADC the maximum frequency would rise to the Nyquist rate of 500kHz. Additionally, applications will be shown of how track and holds can be used to "deglitch" DACs and how a peak detector can be formed. Many track and hold architectures will be presented with a discussion of the strengths and weaknesses of each type. The discussion will show how the characteristics of the sample and hold interact to gain an understanding of how to optimize the design for particular applications. This will also be a useful way of understanding the increasing level of complexity. Before the comparison of different types of architectures begins, Figure 24 calculates the bandwidth of a track and hold and Figure 25 shows a plot of the frequency response.

As a way of introduction, the most elementary track and hold is shown in Figure 26. A FET switch is connected to a capacitor which in turn is isolated from the output by a high input-impedance buffer. When the sampling signal, which is connected to the gate of the N-channel enhancement mode FET, is in the high state, the FET series resistance is at its lowest which is R_{ON}. During this condition the output of the buffer is the input signal modified by the low pass filter action of R_{ON} and the holding capacitor C. The voltage across the holding capacitor will follow the input voltage until the gating signal is returned to the low state and the FET is turned off. At that point the holding capacitor retains the input voltage at the instant of sampling. Figure 27 shows waveforms that depict the dynamic characteristics of the track and hold. When the track and hold is driving an analog to digital converter, the held voltage is then converted to its digital equivalent. The circuit previously described has limited capability. To determine the nature of the limitations, a design example will show how the performance is determined. For this design example a typical N-channel D-MOS FET will be used along with a FET op amp connected as a voltage follower. The FET has the following characteristics:

1. $R_{ON} = 50\Omega$
2. $V_T = 2.5V$
3. $C_{GD} = 0.5pF$
4. $C_{DS} = 0.1pF$
5. $I_{DSS} = 25mA$
6. $I_{OFF} = 50pA$

Assume for this example that the input signal range is 10V peak to peak and it is tolerable that each error source can contribute ±0.01% of V_{IN} to the overall error. Particular

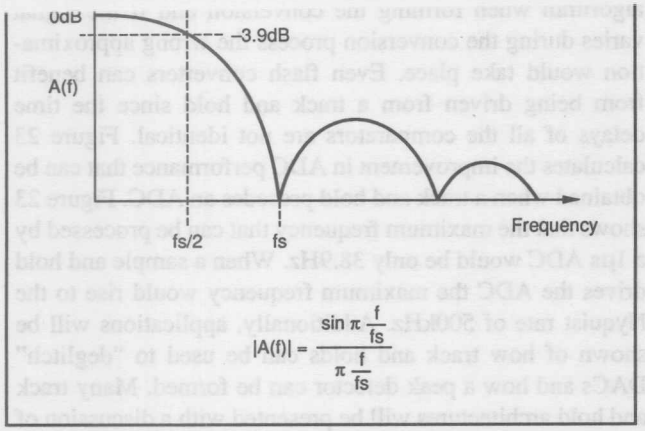


FIGURE 25. Frequency Response of Sample/Hold.

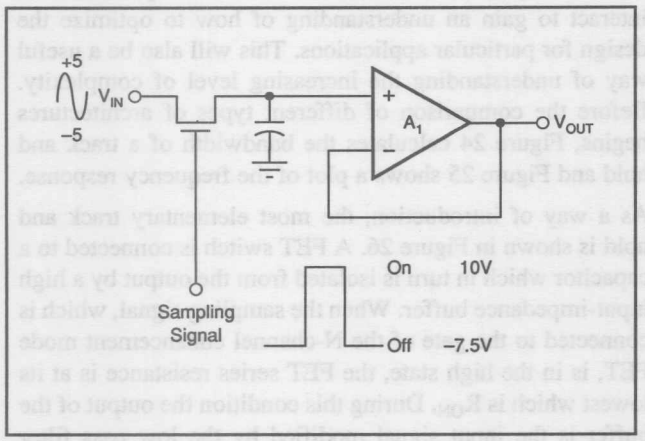


FIGURE 26. Basic Sample/Hold.

applications may assign the value of individual error sources differently. The sources of error that will be considered are:

1. Change induced offset error
2. Aperture non-linearity
3. Signal feedthrough
4. Aperture jitter
5. Aperture delay
6. Droop
7. Acquisition time
8. Track to hold settling
9. Full power bandwidth

CHARGE INDUCED OFFSET OR PEDESTAL ERROR

To ensure that the FET is turned on with a low resistance it is necessary to exceed the peak input signal by 5V. Therefore the voltage applied to the gate of the FET is

$$V_{ON} + V_{PEAK} = 5 + 5 = 10V$$

To ensure that the FET is off it is necessary that the FET is reverse biased under the worst case conditions. The minimum voltage that the sample and hold has to process is –5V and it is desirable to reverse bias the gate to source under

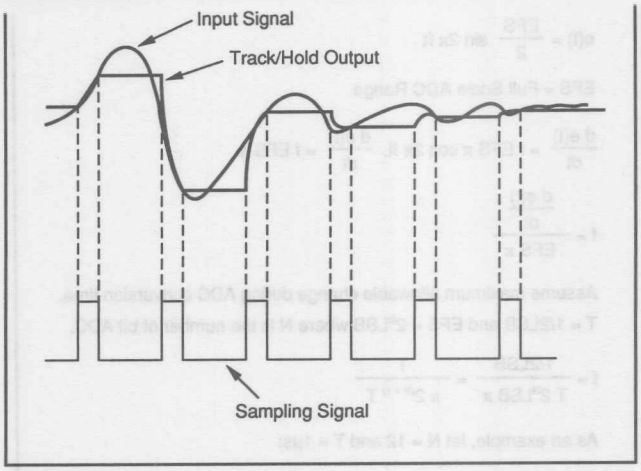


FIGURE 27. Track/Holds Wave Forms.

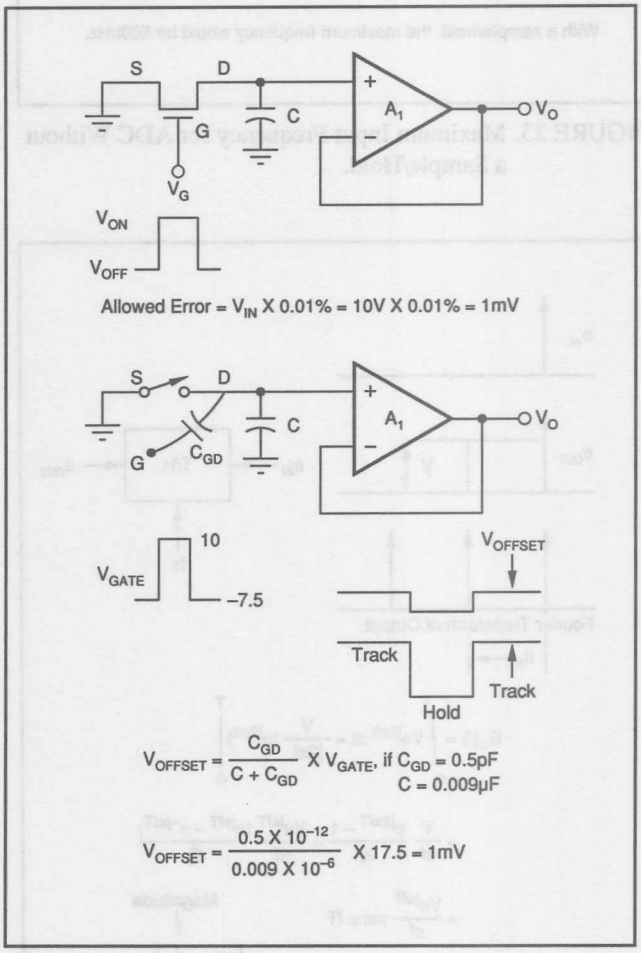


FIGURE 28. Charge Induced Error.

these conditions so the off signal that is applied to the gate of the FET is –7.5V. See Figure 26. The total signal swing that is applied to the gate of the FET is therefore 17.5V, the sum of the on and off signals. Figure 28 shows how a voltage divider is formed by the gate to drain capacitance C_{GD} and the holding capacitor C. A charge induced offset error is

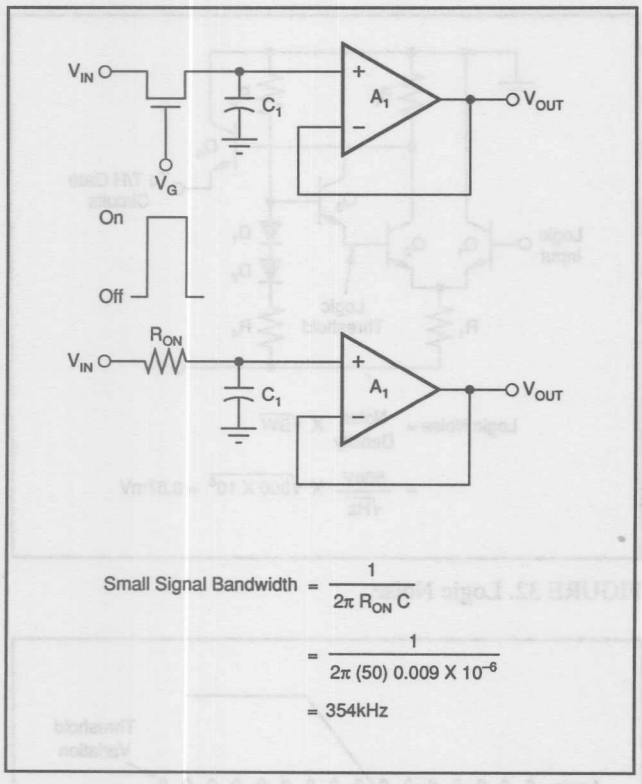


FIGURE 29. S/H Frequency Response.

then created by this voltage divider action and its value is given by:

$$V_{OFFSET} = V_{GATE} \left(\frac{C_{GD}}{C + C_{GD}}\right)$$

Therefore, to reduce the charge induced offset error to:

$$0.01\% \times 10 = 1mV$$

requires a holding capacitor of:

$$C = \frac{C_{GD} \cdot V_{GATE} - C_{GD} \cdot V_{OFFSET}}{V_{OFF}}$$

$$C = \frac{0.5pF \cdot 17.5V - 0.5pF \cdot 1mV}{1mV} = 8.75nF$$

Now since the value of the holding capacitor ($C_H = C$) is determined, the track and hold bandwidth would be (see Figure 29):

$$BW = 1/2\pi(R_{ON})(C_H) = 1/2\pi(50)(9 \times 10\text{–}9)$$
$$= 354kHz$$

APERTURE INDUCED NON-LINEARITY

In the previous discussion on charge induced offset error it was assumed that the gate turn off signal was always 17.5V. If the input signal were sampled at its peak of 5V and the FET threshold voltage were 2.5V, the FET would stop conducting when the voltage on the gate was 7.5V. The effective gate signal swing would be reduced to 15V and the amount of charge induced offset would also be reduced.

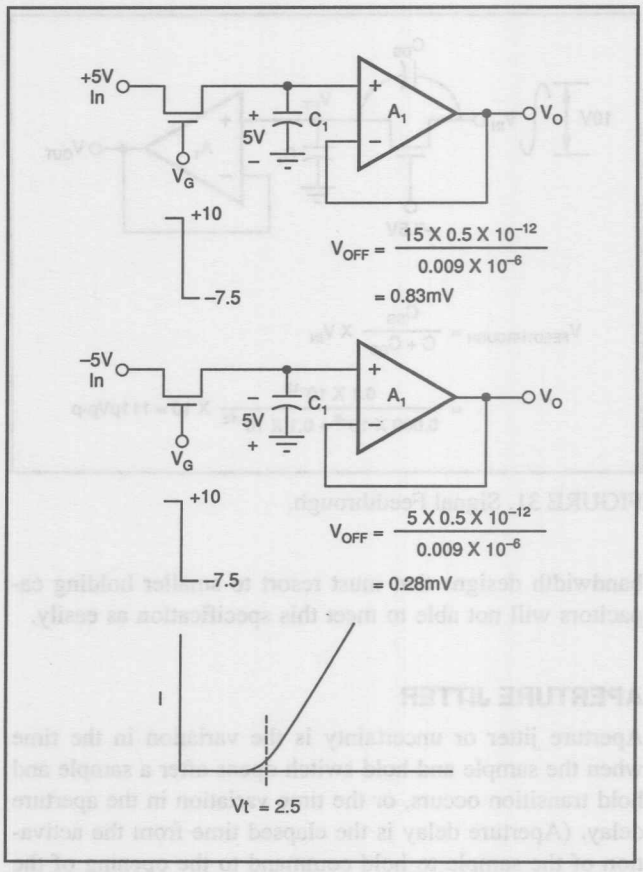


FIGURE 30. FET Threshold Characteristics and Aperture Non-linearity.

Similarly, if the input signal being sampled is at the minimum level of –5V, the effective gate swing would be 5V. In the previous section it was calculated that if the gate swing were 17.5V, the charge induced offset would be 1mV. See Figure 30. Actually the charge induced offset is modulated by the signal and varies between 0.83mV for the positive extreme and 0.28mV for the negative extreme. Since both offsets are less than the allowable error this is not a problem; the holding capacitor is relatively large. As will be seen later, this will not always be the case when it is desirable to achieve wider band operation. This effect will be considered again for wider band designs when it could become a serious source of error.

SIGNAL FEEDTHROUGH

Signal feedthrough occurs because of the presence of a capacitor that is connected from the drain to the source of the FET. This is a parasitic capacitor that is either due to layout or other stray effects. Referring to Figure 31, it is seen that the input signal will be coupled to the hold capacitor and is given by:

$$V_{FEEDTHROUGH} = (C_{DS}/C_H)(V_{IN}) = (0.1pF/0.009\mu F)(10)$$
$$= 111\mu Vp\text{-}p$$

which is a tolerable error. Again it will be seen that wider

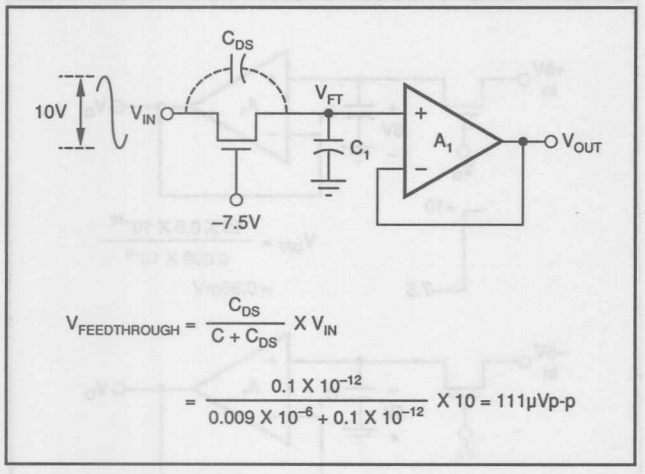


FIGURE 31. Signal Feedthrough.

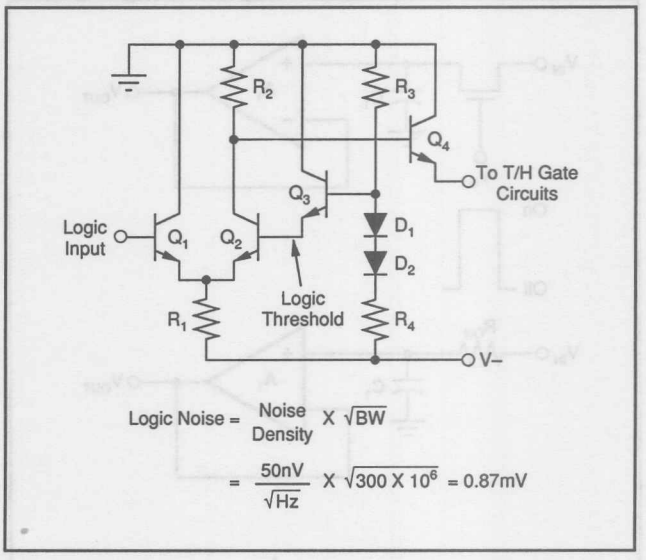


FIGURE 32. Logic Noise.

bandwidth designs that must resort to smaller holding capacitors will not able to meet this specification as easily.

APERTURE JITTER

Aperture jitter or uncertainty is the variation in the time when the sample and hold switch opens after a sample and hold transition occurs, or the time variation in the aperture delay. (Aperture delay is the elapsed time from the activation of the sample to hold command to the opening of the switch in the hold mode.) There are two sources of aperture jitter: power supply induced noise and threshold variation due to thermal noise. If attention is paid to filtering the power supply properly, as well as using a well-regulated power supply, this will not be a source of aperture jitter. As a practical matter, because of measurement difficulty, determining the amount of aperture jitter that is present in the system is often more of a problem than limiting it to an acceptable level. Techniques for measuring aperture jitter will be shown in the measurement section. Assume that the noise associated with the logic threshold is $50nV/\sqrt{Hz}$. This would be ten times greater than the noise of a typical linear amplifier. Further assume that the bandwidth of the logic circuit that develops the gate signal is 300MHz. The noise variation of the logic level would then be (see Figure 32):

$$\text{Threshold variation due to logic noise} = (50nV)(\sqrt{300E6})$$
$$= 0.87mV$$

If the logic signal rate of transition were 0.4V/ns, the aperture jitter would be (see Figure 33):

$$\text{Aperture jitter} = (\text{threshold noise})/(\text{logic slew rate}) = t_A$$
$$= (0.87mV)/(0.4V/ns) = 2.2ps$$

which will be seen to be negligible for all but the highest sampling rate data conversion applications. Aperture jitter can create amplitude noise by causing a variation of the sampling point of dynamic signals. The noise can be predicted by:

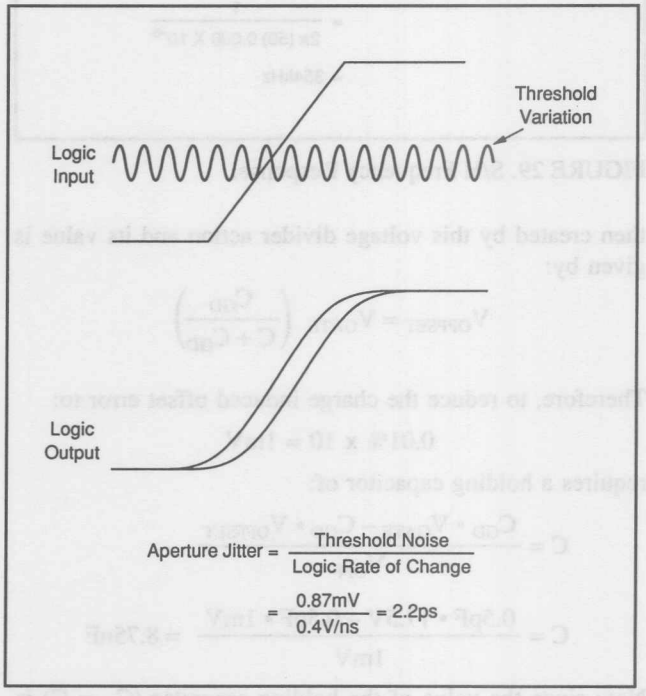


FIGURE 33. Aperture Jitter.

$$\text{Aperture induced noise}$$
$$= (\text{signal rate of change})(\text{aperture jitter})$$
$$= (de/dt)(t_A)$$
$$= (FS)(\pi)(f)(t_A)$$

Assume a 12-bit ADC with a sampling rate of 20MHz. FS = 4096LSB, f = 10MHz, t_A = 2.2ps.

$$\text{Aperture induced noise} = (4096)(\pi)(tA)$$
$$= (4096)(\pi)(10E6)(2.2E{-}12) = 0.28LSB$$

0.28LSB aperture induced noise would be acceptable for a 12-bit ADC with a Nyquist rate of 10MHz. Figures 34 and 35 illustrate this effect.

APERTURE DELAY

The aperture delay is the elapsed time from the activation of the sample to hold command to the opening of the switch in the hold mode. See Figure 36. Controlling aperture delay is important when multiple channels need to be matched to each other. Figure 37 shows a circuit diagram of a FET driver circuit that is TTL compatible and is suitable for driving the sample switch.

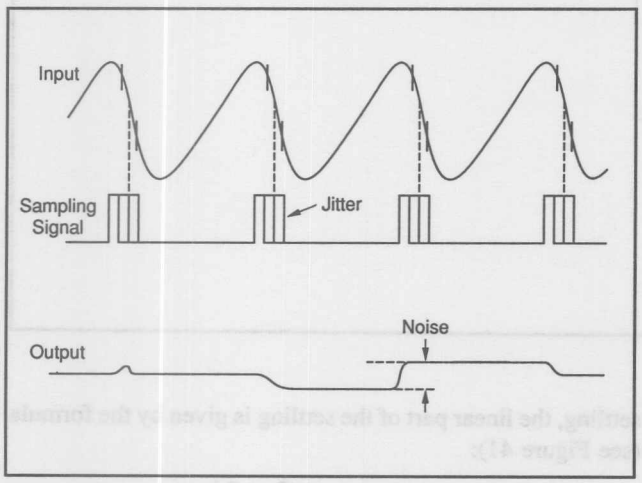


FIGURE 34. Aperture Induced Noise.

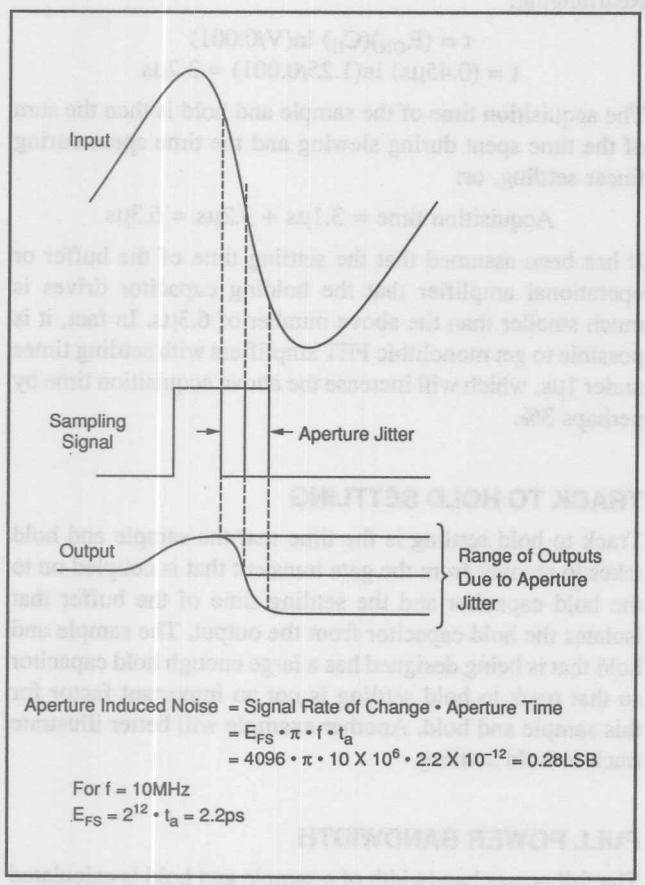


FIGURE 35. Aperture Induced Noise.

DROOP

While the sample and hold is in the hold mode the leakage current that flows through the FET and the input bias current of the operational amplifier will tend to discharge (or charge) the holding capacitor. Both sources of current are about 50pA at 25°C so the capacitor will change at a rate of (see Figure 38):

$$I/C = 100pA/0.009\mu F = 0.011V/s$$

If the sample and hold were driving an ADC with a 10µs conversion time, the held value would change by 0.11µV during the conversion process. Since the allowable error from each source is 1mV, this is not a source of error at room temperature. Since leakage current doubles every 10°C, when the operating temperature increases to 125°C, the voltage change, due to droop, during the conversion would increase to 0.11mV, which is still below the allowable value. Wider band designs that use smaller holding capacitors will not meet this specification as easily and other methods will be shown that can reduce the droop to acceptable levels.

ACQUISITION TIME

The calculation of acquisition time of a sample and hold is identical to the way settling time is determined for an operational amplifier. (It is really the same phenomenon.) The sample and hold will slew in response to a large signal change until the output rate of change of the sample and hold

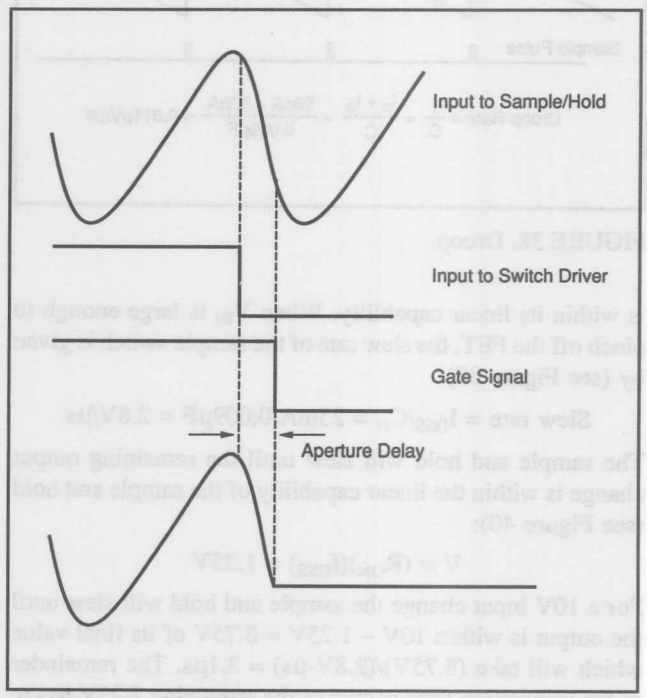


FIGURE 36. Aperture Delay.

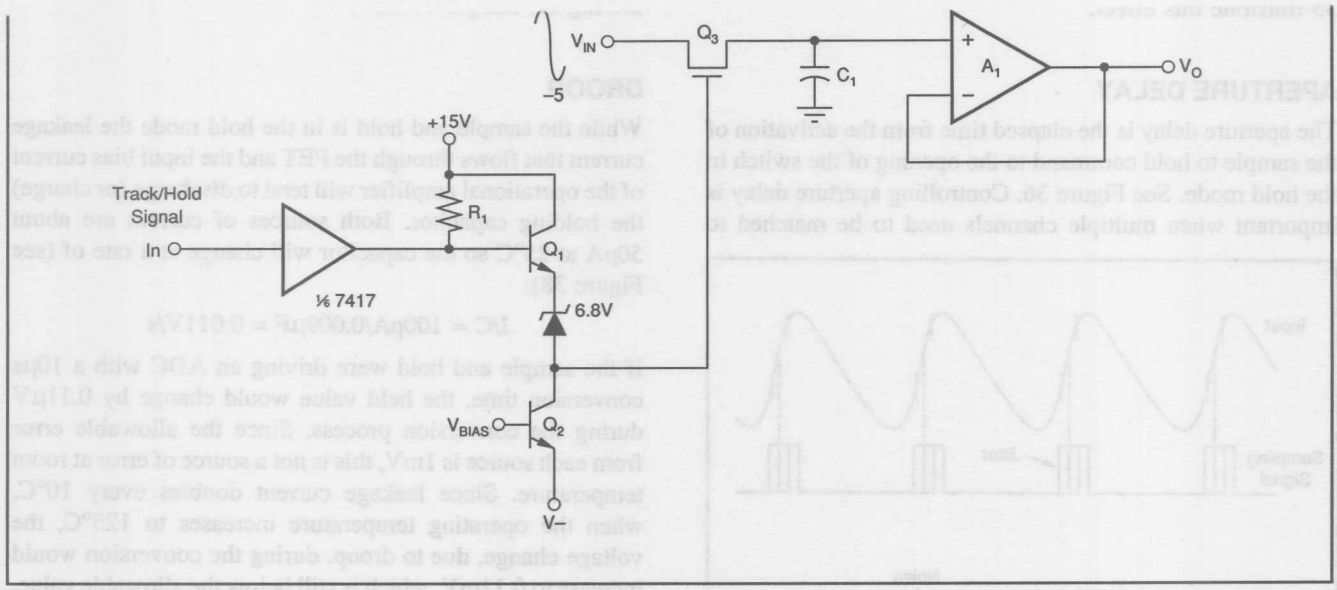


FIGURE 37. FET Switch Driver.

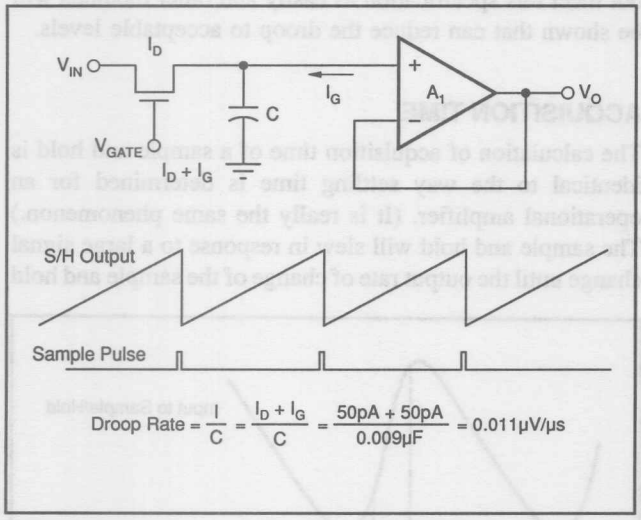


FIGURE 38. Droop.

is within its linear capability. When V_{IN} is large enough to pinch off the FET, the slew rate of the sample switch is given by (see Figure 39):

$$\text{Slew rate} = I_{DSS}/C_H = 25mA/0.009\mu F = 2.8V/\mu s$$

The sample and hold will slew until the remaining output change is within the linear capability of the sample and hold (see Figure 40):

$$V = (R_{ON})(I_{DSS}) = 1.25V$$

For a 10V input change the sample and hold will slew until the output is within 10V – 1.25V = 8.75V of its final value which will take (8.75V)/(2.8V-µs) = 3.1µs. The remainder of the acquisition time occurs as the remaining 1.25V has to settle to within 1mV of the final value. Assuming single pole settling, the linear part of the settling is given by the formula (see Figure 41):

$$V = V(1 - e^{-(t / R_{ON} \cdot C_H)})$$

Rearranging:

$$t = (R_{ON})(C_H)\ \ln(V/0.001)$$
$$t = (0.45\mu s)\ \ln(1.25/0.001) = 3.2\mu s$$

The acquisition time of the sample and hold is then the sum of the time spent during slewing and the time spent during linear settling, or:

$$\text{Acquisition time} = 3.1\mu s + 3.2\mu s = 6.3\mu s$$

It has been assumed that the settling time of the buffer or operational amplifier that the holding capacitor drives is much smaller than the above number of 6.3µs. In fact, it is possible to get monolithic FET amplifiers with settling times under 1µs, which will increase the above acquisition time by perhaps 3%.

TRACK TO HOLD SETTLING

Track to hold settling is the time that the sample and hold takes to recover from the gate transient that is coupled on to the hold capacitor and the settling time of the buffer that isolates the hold capacitor from the output. The sample and hold that is being designed has a large enough hold capacitor so that track to hold settling is not an important factor for this sample and hold. Another example will better illustrate track to hold settling.

FULL POWER BANDWIDTH

The full power bandwidth of a sample and hold is calculated in the same manner as it is for an operational amplifier.

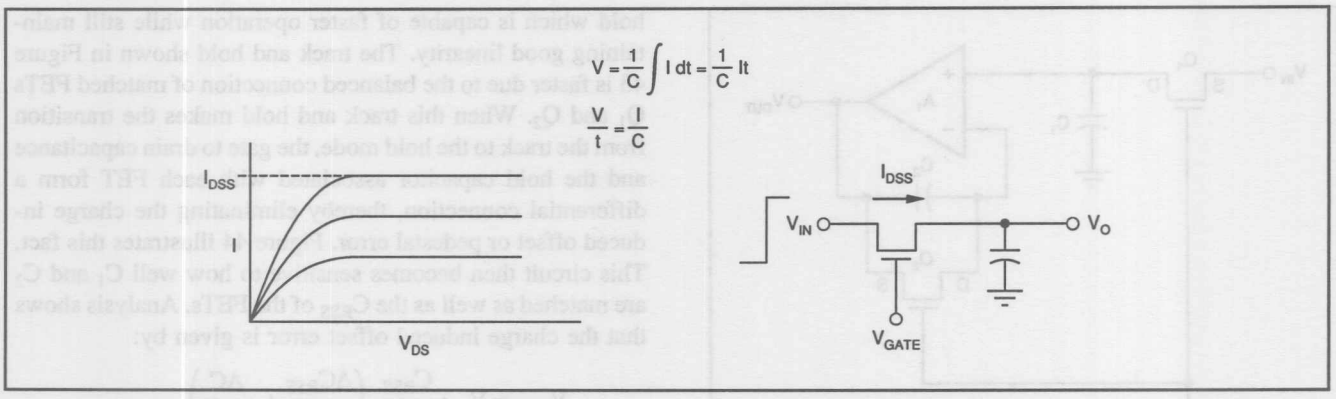


FIGURE 39. Capacitor Charged from a Constant Current.

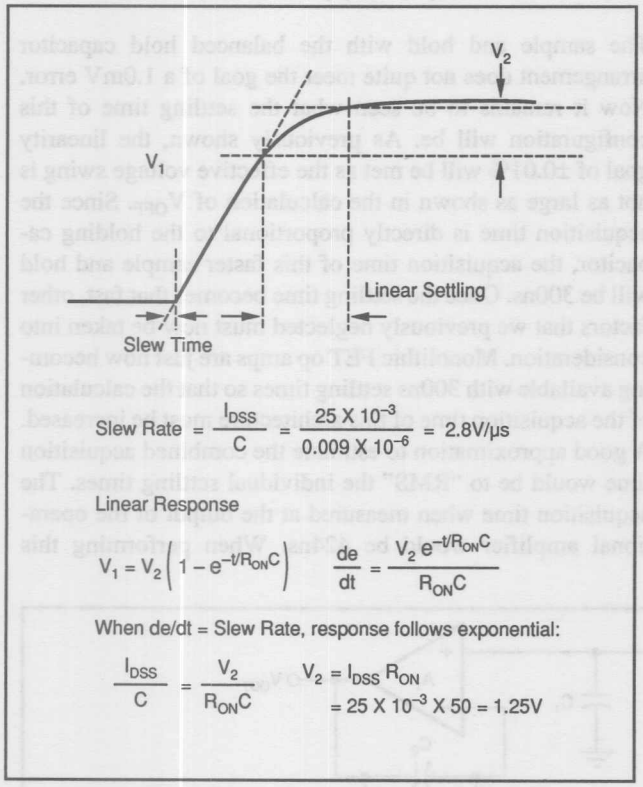


FIGURE 40. Acquisition Time.

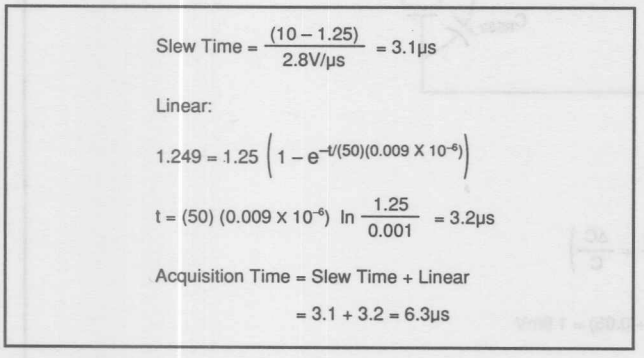


FIGURE 41. Acquisition Time.

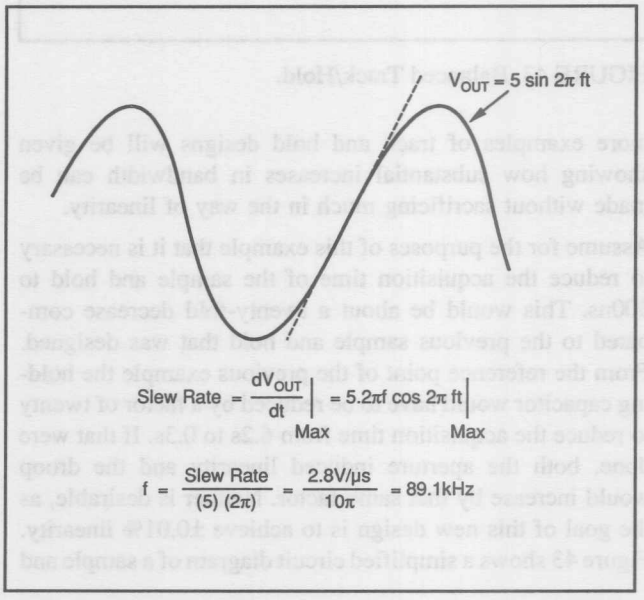


FIGURE 42. Full Power Bandwidth.

Knowing the full power bandwidth is important as it is necessary to operate at less than that frequency to maintain low levels of distortion. For the design example in question (see Figure 42):

$$V_{OUT} = (5)\ \sin(2\pi fT) \text{ and:}$$
$$dV_{OUT}/dT = \text{Max Slew Rate} = 10(\pi)f$$

Rearranging terms:

$$\text{Full Power Bandwidth} = (\text{Slew Rate})/10(\pi) = 89.1kHz$$

The above example demonstrates how to approach the design of the simplest type of track and hold. Even though it is simple, it would be very useful as the full power bandwidth of 89.1kHz would be adequate for processing audio signals. A sample and hold with an acquisition time of 6.2µs driving an ADC with a 10µs conversion time would have an adequate sampling rate to process an audio signal. Furthermore, this circuit could be built for a cost in the $5-10 range. While the design of this circuit is relatively straightforward, it does have limited bandwidth. Several

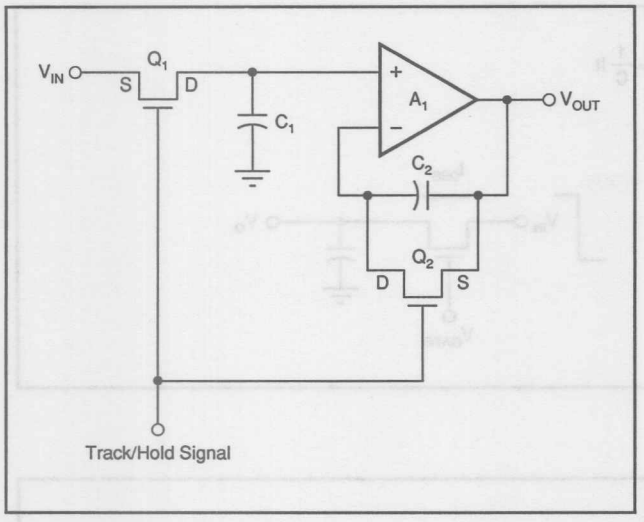


FIGURE 43. Balanced Track/Hold.

more examples of track and hold designs will be given showing how substantial increases in bandwidth can be made without sacrificing much in the way of linearity.

Assume for the purposes of this example that it is necessary to reduce the acquisition time of the sample and hold to 300ns. This would be about a twenty-fold decrease compared to the previous sample and hold that was designed. From the reference point of the previous example the holding capacitor would have to be reduced by a factor of twenty to reduce the acquisition time from 6.2s to 0.3s. If that were done, both the aperture induced linearity and the droop would increase by that same factor. Neither is desirable, as the goal of this new design is to achieve ±0.01% linearity. Figure 43 shows a simplified circuit diagram of a sample and hold which is capable of faster operation while still maintaining good linearity. The track and hold shown in Figure 43 is faster due to the balanced connection of matched FETs Q_1 and Q_2. When this track and hold makes the transition from the track to the hold mode, the gate to drain capacitance and the hold capacitor associated with each FET form a differential connection, thereby eliminating the charge induced offset or pedestal error. Figure 44 illustrates this fact. This circuit then becomes sensitive to how well C_1 and C_2 are matched as well as the C_{RSS} of the FETs. Analysis shows that the charge induced offset error is given by:

$$V_{OFF} = V_G \cdot \frac{C_{RSS}}{C}\left(\frac{\Delta C_{RSS}}{C_{RSS}} + \frac{\Delta C}{C}\right)$$

$$= 17.5\ (0.5/450)\ (0.05 + 0.05) = 1.9\text{mV}$$

The sample and hold with the balanced hold capacitor arrangement does not quite meet the goal of a 1.0mV error. Now it remains to be seen what the settling time of this configuration will be. As previously shown, the linearity goal of ±0.01% will be met as the effective voltage swing is not as large as shown in the calculation of V_{OFF}. Since the acquisition time is directly proportional to the holding capacitor, the acquisition time of this faster sample and hold will be 300ns. Once the settling time becomes that fast, other factors that we previously neglected must now be taken into consideration. Monolithic FET op amps are just now becoming available with 300ns settling times so that the calculation of the acquisition time of this architecture must be increased. A good approximation to estimate the combined acquisition time would be to "RMS" the individual settling times. The acquisition time when measured at the output of the operational amplifier would be 424ns. When performing this

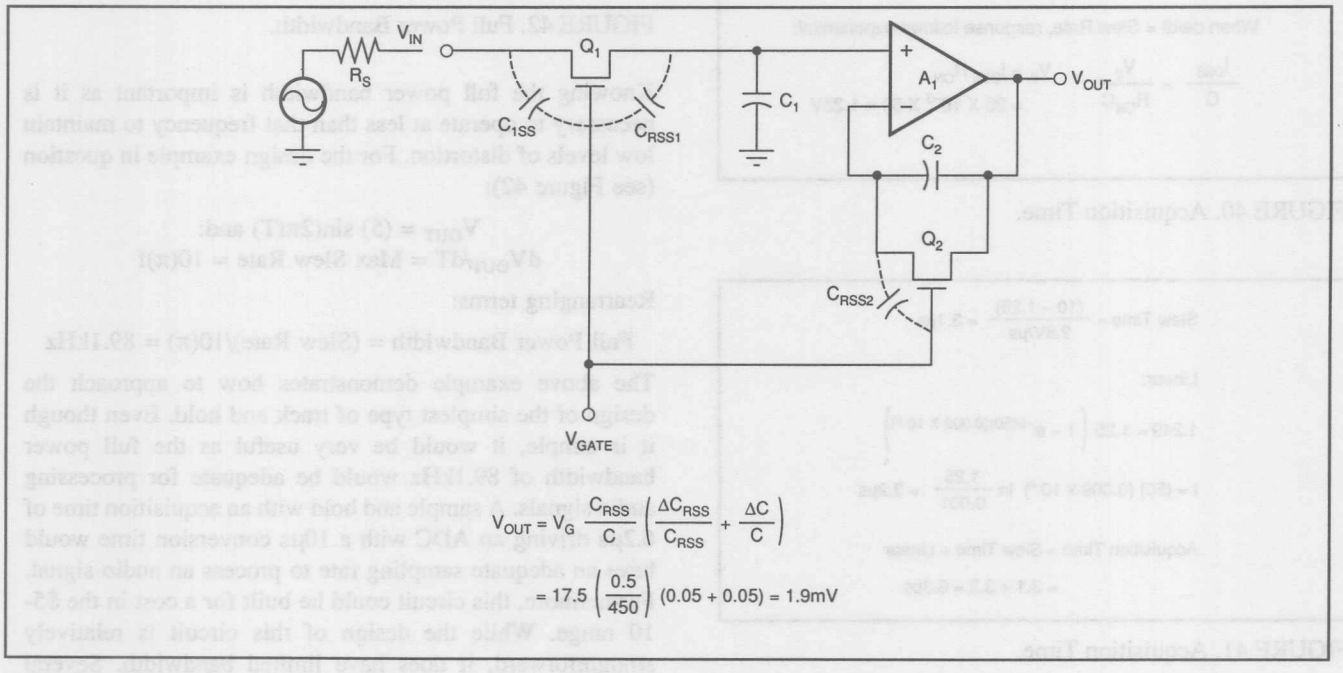


FIGURE 44. Capacitance Mismatch.

calculation for the example in question, a subtlety about acquisition time should be pointed out. The previous two architectures that have been discussed are ones where the sample and hold function is separate from the associated buffer or op amp. This is not true for a feedback architecture that will be discussed later. In some systems applications the distinction between the voltage developed across the hold capacitor and the output of the buffer are important. One important application that will be discussed in detail in the section on analog to digital converters is where the sample and hold drives a sub-ranging ADC. Even though the input signal must be acquired accurately, the voltage does not need to be accurately known to begin the conversion process. Figure 45 shows how the hold capacitor acquires the signal in 300ns while the output of the buffer reaches the same point in 424ns.

One of the drawbacks of this and the previously described circuit is the charge injection of the gate signal through the source to gate capacitance as shown in Figure 44. The nature of the driving impedance can create a great deal of uncertainty as to the nature of the pedestal during the time when the FET is being switched from on to off. The source may be ringing or settling in some unfavorable manner and the track and hold will store the results of the driving source not settling. The track and hold would then benefit from being driven from a buffer to eliminate this problem.

Another problem with the circuit shown in Figure 43 is the poor feedthrough performance. If the feedthrough capacitance is 0.1pF and the hold capacitance is 450pF, the feedthrough voltage could be as much as (10)(0.1/450) = 2.2mV which exceeds the goal of 1mV. To reduce the feedthrough voltage, the holding capacitor would have to be increased to 990pF. Increasing the hold capacitor to 990pF to reduce the feedthrough voltage would increase the acquisition time across the hold capacitor to 600ns.

This previous calculation shows how the various design parameters can interact and even though one specification is met other specifications must be re-evaluated before the design is complete. It has been shown that even though the arbitrary design goal of 300ns could not be met, this circuit should not be discarded, as improved performance has been achieved. The cost of this sample and hold is relatively modest and could be produced for about $10-15. As a practical matter, a sub-500ns sample and hold can be very useful when interfacing with a 5µs ADC and it is desirable to minimize the overall conversion time.

Let us return to the original design challenge, which was to design a sub-300ns sample and hold. Another architecture that is worth considering is shown in Figure 46. This architecture employs the switching FET in the summing junction of an inverting feedback amplifier. The advantage of this connection is that it is possible to drive the FET with a much smaller gate signal which allows the holding capacitor to become smaller. This architecture also has the compensating FET connected in a differential fashion so the circuit is only sensitive to the match of the FETs and is not

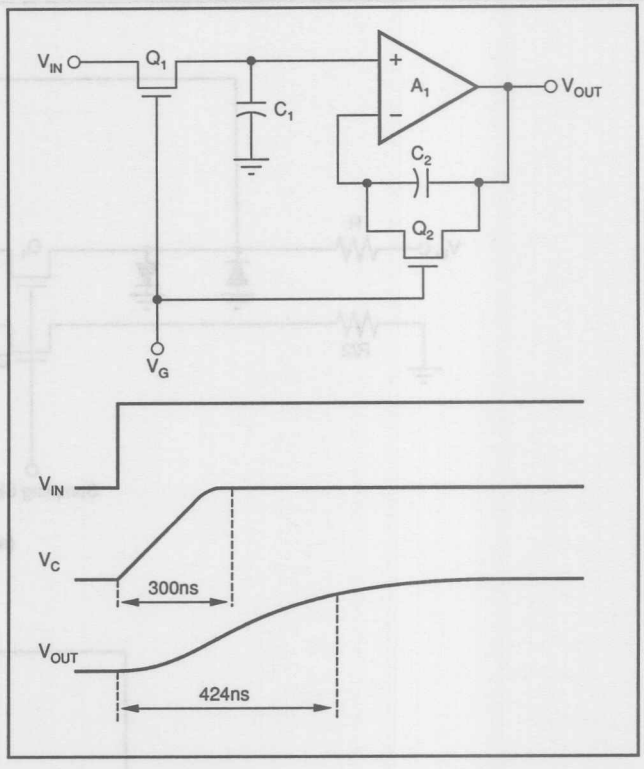


FIGURE 45. Difference in Acquisition Time Between Buffer and Hold Cap.

sensitive to the absolute value of C_{RSS}. Notice the clamping diodes that are placed at the summing junction. These diodes reduce the signal that the FETs have to hold off when the sample and hold is in the hold mode, thereby minimizing the magnitude of the drive signal that needs to be applied to the FET. Circuitry to minimize the feedthrough problem could have also been applied to the previous two design examples, although it would have been much more complicated than the two diodes connected to the feedback track and hold. The gate drive signal can be made smaller since the switch is located in the summing junction of the operational amplifier and the feedback action of the amplifier tends to drive the signal at the summing junction to zero. This also has the effect of linearizing the operation of the track and hold since the charge induced offset pedestal is not signal dependent as it is in the original designs. To ensure that the FET is on, a 5V signal is applied during the sample or track mode and to ensure that the FET is off during the hold mode, a -2.5V level needs to be applied. Therefore the total gate swing will be 7.5V.

Since diodes have been placed at the summing junction, the maximum voltage that can be developed at the input to the FETs is 0.6V peak. From the previous example it was found that it was necessary to have a 500pF holding capacitor to reduce the feedthrough voltage to an acceptable level. Since the feedback track and hold reduces the effective input voltage to the FET to 0.6V, the holding capacitor can be reduced to 60pF. The effective small-signal time constant for this track and hold connection is $T = (2R_{ON} + R_F)C$.

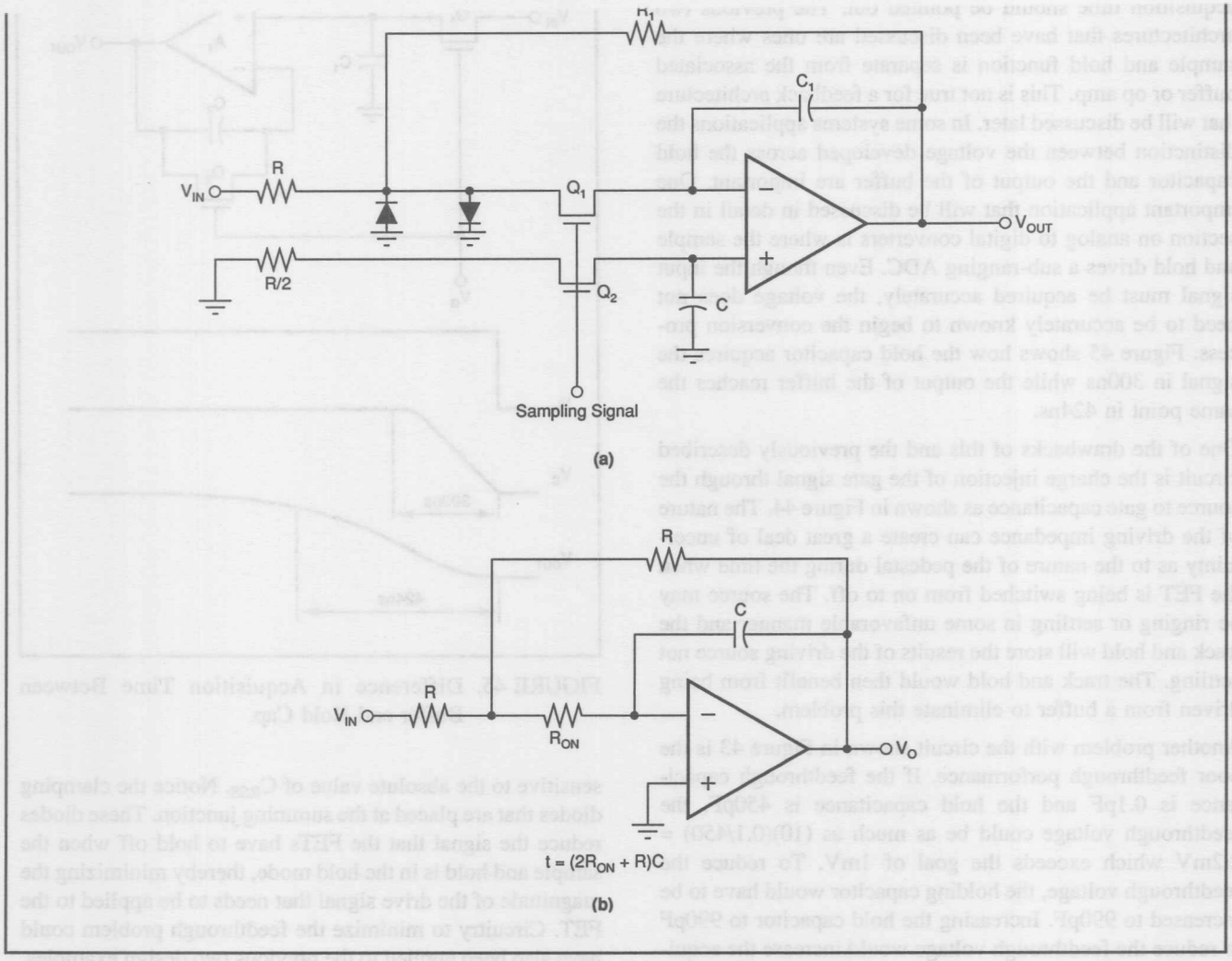


FIGURE 46. Inverting Sample/Hold.

$$\text{Amplifier will slew until slew rate} = \frac{E}{T}$$

$$T = (2\,R_{ON} + R_F)\,C = (2 \times 50 + 300)\,60\text{pF} = 24\text{ns}$$

$$E = T \times \text{Slew Rate} = 24 \times 10^{-9} \times \frac{200\text{V}}{10^{-6}} = 4.8\text{V}$$

$$\text{Acquisition Time} = \frac{\text{Input} - E}{\text{Slew Rate}} + T \ln \frac{E}{\text{Error}}$$

$$= \frac{10 - 4.8}{200\text{V}/\mu\text{s}} + 24\text{ns} \ln \frac{4\text{V}}{0.001\text{V}}$$

$$= 26\text{ns} + 203\text{ns} = 229\text{ns}$$

$$\text{Feedthrough} = 0.6\text{Vp-p} \times \frac{0.1\text{pF}}{60\text{pF}} = 1\text{mVp-p}$$

Feedthrough Capacitance

Input Clamped by Diode

Feedback Capacitance

FIGURE 47. Performance of Feedback Track/Hold.

Assume that the previously mentioned FET was used along with a monolithic amplifier with a 200V/µs slew rate and a 30MHz small signal bandwidth. Let R_F be 300Ω. The amplifier will then slew until the remaining voltage change is within the linear slew rate capability of the op amp. The small signal time constant of this track and hold is then:

$$T = [(2)50 + 300][60] = 24\text{ns}$$

This corresponds to a small-signal bandwidth of 6.6MHz so the small-signal bandwidth of the track and hold will be determined by the external components rather than by the op amp. Therefore, when the remaining voltage that the track and hold has to change is 4.8V, the track and hold will cease to slew. The time consumed in slewing is then (10 - 4.8)/(200V/µs) = 26ns. (See Figures 40 and 41 for a view of the acquisition time calculation.) The remaining time is given by (24) ln(4.8/0.001%) = 203ns; therefore the acquisition of the track and hold is 229ns and the goal of 300ns can be met with the architecture shown in Figure 46. Figure 47 summarizes the performance of the feedback track and hold. While this track and hold configuration is able to achieve a lower

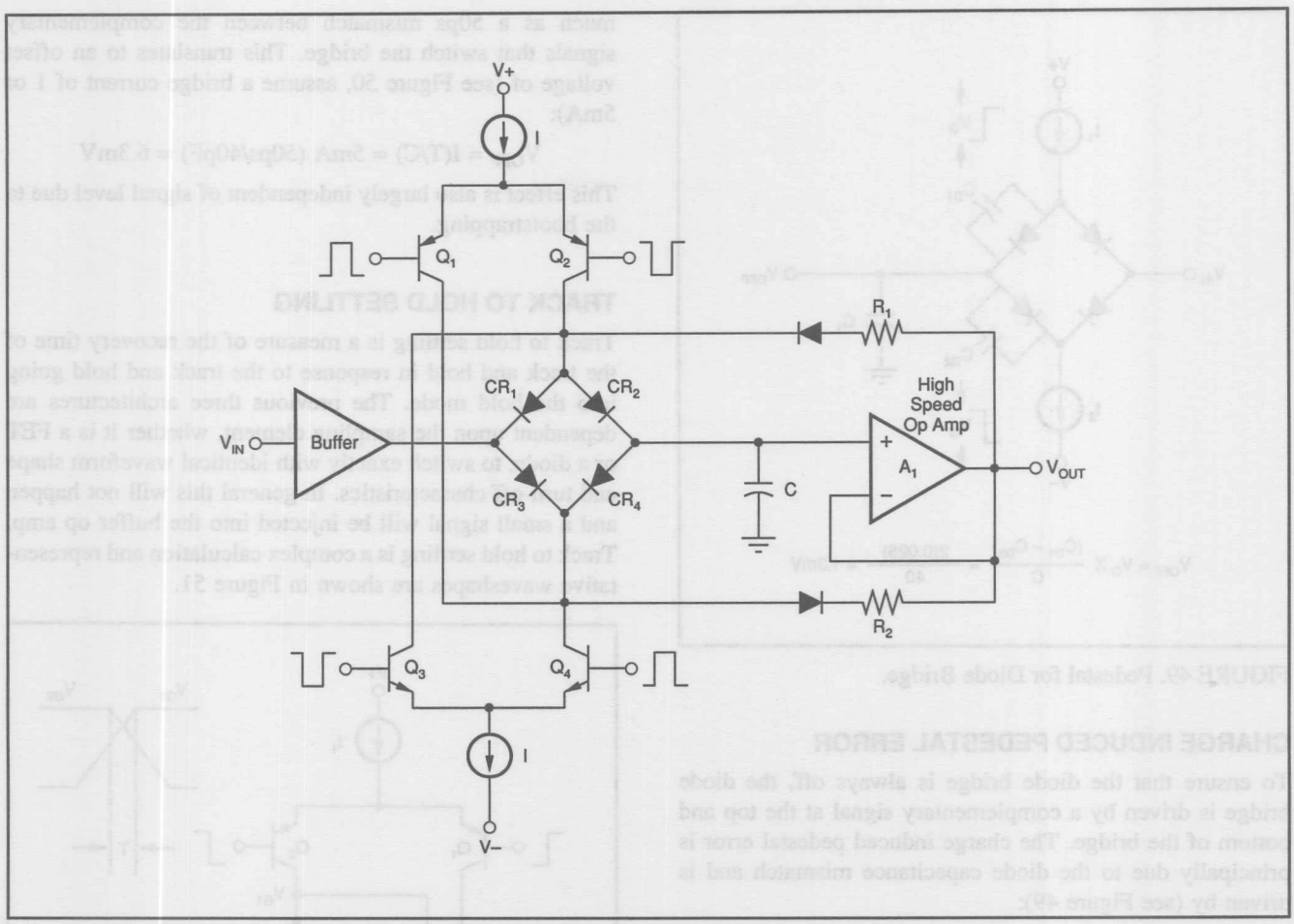


FIGURE 48. Very High Speed Sample/Hold.

acquisition time, it does so at the expense of a lower input impedance. This may not be much of a penalty as the input impedance of 300Ω is within the capability of many op amps to drive with ±5V input.

The last track and hold that will be described is capable of acquisition times that are about an order of magnitude faster than the last one that was described. This track and hold, shown in Figure 48, shares some of the architectural features of the previously described ones, although the sampling element is different. This higher speed sample and hold uses hot carrier diodes in a bridge configuration to form the sampling element. Diodes, while more complex to form a sample and hold, achieve high sampling speed due to the lower time constant compared to a FET and lower threshold voltages. As an example, a hot carrier diode operated at 5mA has a resistance of 5Ω, V_D of 0.6V and a capacitance of 5pF. Figure 48 shows a diagram of a sample and hold that has an acquisition time of 40ns to ±0.02% for a 2V step input. This sample and hold has a measured aperture time of under 3ps. (A technique to measure aperture time is shown in the measurement section.) The sampling function is performed by switching the bridge of hot carrier diodes CR_1 through CR_4 from the "on" to the "off" state. During the sample mode the current I is steered through the diode bridge by turning on transistors Q_2 through Q_4. The bridge is returned to the hold mode by turning Q_3 and Q_4 off and turning Q_1 and Q_3 on. The action of turning Q_1 and Q_3 on creates a negative bias on CR_1 and CR_4. Since these bias voltages are referenced to the output, creating "bootstrap effect," the reverse bias voltage that diodes CR_1 through CR_4 experience becomes independent of signal level. This is an important aspect of the design as this action prevents the charge offset pedestal from becoming a non-linear function of signal level. An ECL signal is coupled to switching transistors Q_1 through Q_4. The hold capacitor is isolated from the output by the type of high speed buffers and op amps described in the amplifier section. The sampling bridge is isolated from the analog input signal by a high speed open loop buffer.

As a means of comparison, calculations will demonstrate the different performance parameters of this track and hold. As will be seen from the calculations below, the diode bridge will not achieve as accurate performance as compared to the FET designs.

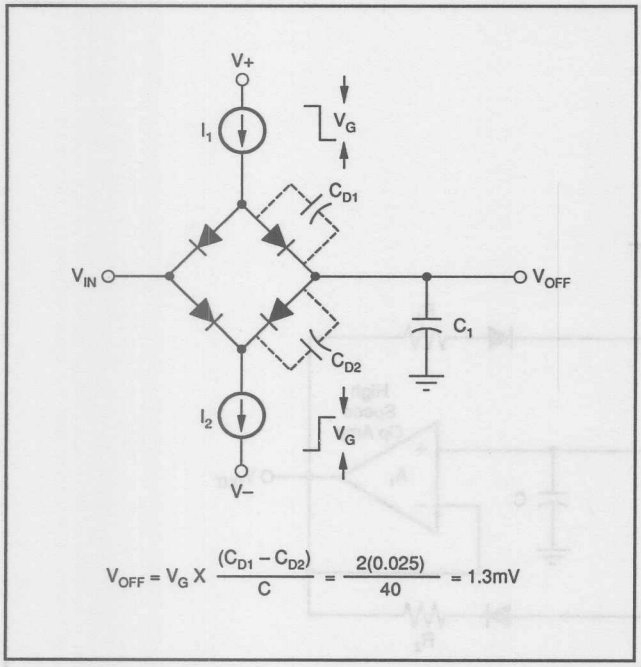


FIGURE 49. Pedestal for Diode Bridge.

CHARGE INDUCED PEDESTAL ERROR

To ensure that the diode bridge is always off, the diode bridge is driven by a complementary signal at the top and bottom of the bridge. The charge induced pedestal error is principally due to the diode capacitance mismatch and is driven by (see Figure 49):

$$V_{OFF} = (V_{OFF})(C_{D1} - C_{D2})/C$$

With care diodes can be matched to 0.025pF. (In actual practice means are provided to adjust the capacitance to this level and once the adjustment is performed the difference in diode capacitance can be held to 0.025pF.) For proper dynamic operation V_G = 2V and the holding capacitor is 40pF. Substituting into the above equation yields:

$$V_{OFF} = (2)(0.025/40) = 1.3mV$$

Unlike the FET designs, this is strictly an offset error as the bootstrapping action renders this offset voltage independent of signal level.

SWITCH DELAY PEDESTAL ERROR

The diode bridge switching arrangement has an additional source of error that is not possessed by the FET switch. If the current sources that bias the bridge are not symmetrically switched, the hold capacitor will start to discharge until the other current source is switched. This error manifests itself at the system level as if it were an offset voltage. To a first approximation the cross-coupling eliminates the time mismatching that exists between the NPN and PNP switching pairs. However, due to second order effects as a result of different levels of parasitic capacitances, there is typically as much as a 50ps mismatch between the complementary signals that switch the bridge. This translates to an offset voltage of (see Figure 50, assume a bridge current of 1 or 5mA):

$$V_{OFF} = I(T/C) = 5mA\ (50ps/40pF) = 6.3mV$$

This effect is also largely independent of signal level due to the bootstrapping.

TRACK TO HOLD SETTLING

Track to hold settling is a measure of the recovery time of the track and hold in response to the track and hold going into the hold mode. The previous three architectures are dependent upon the sampling element, whether it is a FET or a diode, to switch exactly with identical waveform shape and turn-off characteristics. In general this will not happen and a small signal will be injected into the buffer op amp. Track to hold settling is a complex calculation and representative waveshapes are shown in Figure 51.

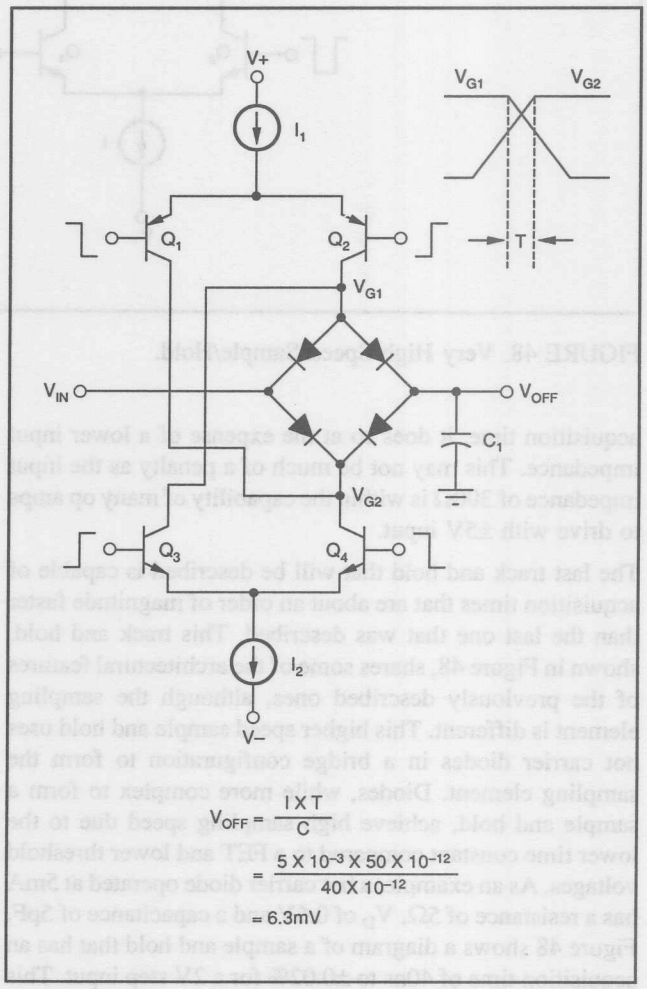


FIGURE 50. Switch Delay.

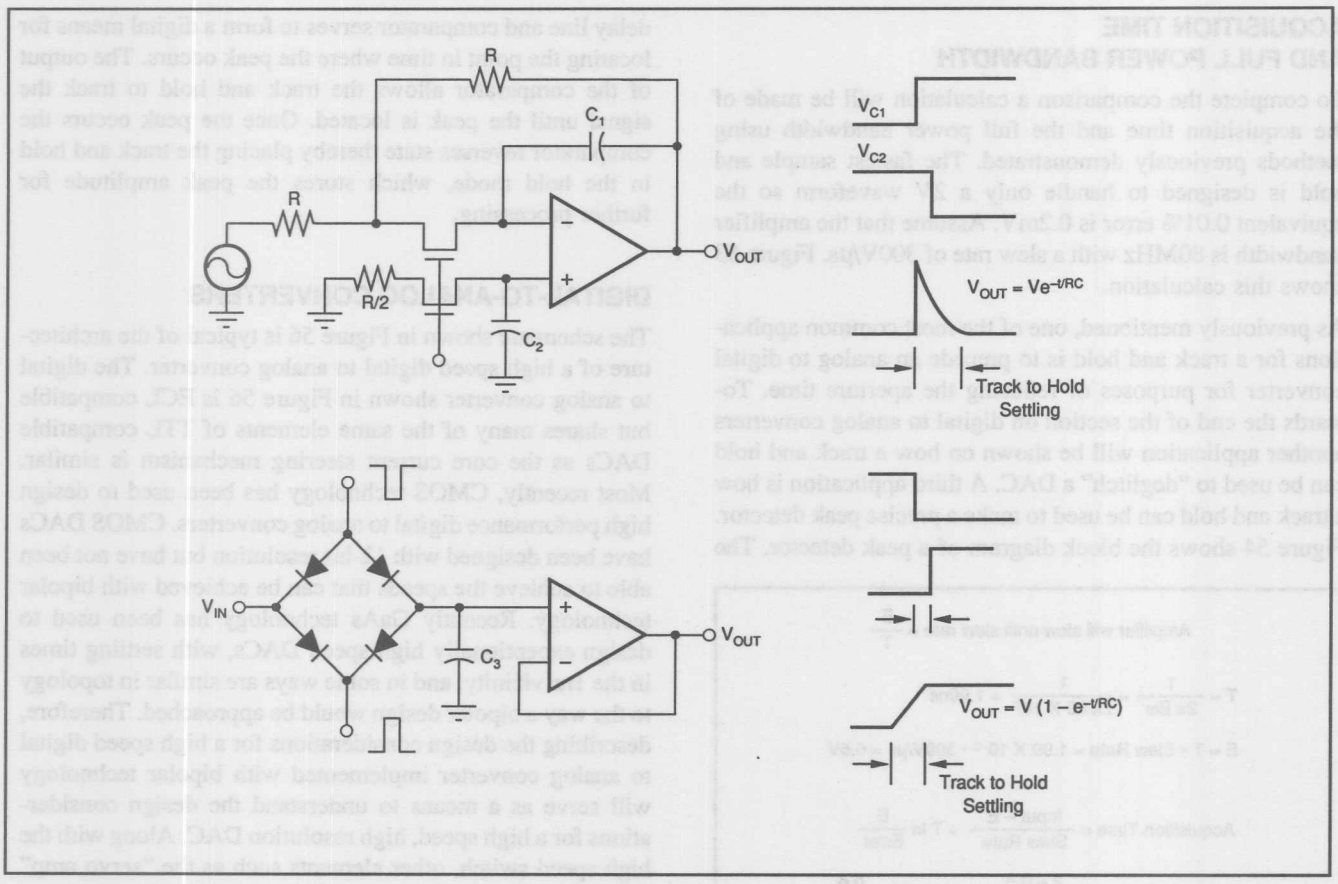


FIGURE 51. Track to Hold Settling.

SIGNAL FEEDTHROUGH

When in the off state, the top and bottom of the bridge are clamped by a low impedance, thereby preventing any signal coupling through that path. Signal feedthrough does occur due to layout and with care a coupling capacitance of 0.01pF can be achieved between the input and output of the bridge. This would yield a feedthrough level of (Figure 52 shows the bridge in the off state):

$$V_{FEEDTHROUGH} = V_{IN}(C_C/C) = 2(0.01/40) = 0.5mV$$

APERTURE JITTER AND DELAY

Aperture jitter of less than 3ps can be achieved and aperture delay of 3ns is also achievable. The lower aperture delay is due to the interface circuitry being wideband ECL.

DROOP

The leakage current that can be achieved with a pair of matched hot carrier diodes is much higher compared to the current levels that can be attained with FETs. Leakage current of 1nA can be achieved with proper thermal level layout. The droop will then be:

Droop = 1nA/40pF = 25µV/µs at 25°C,
or about 25mV/µs at 125°C

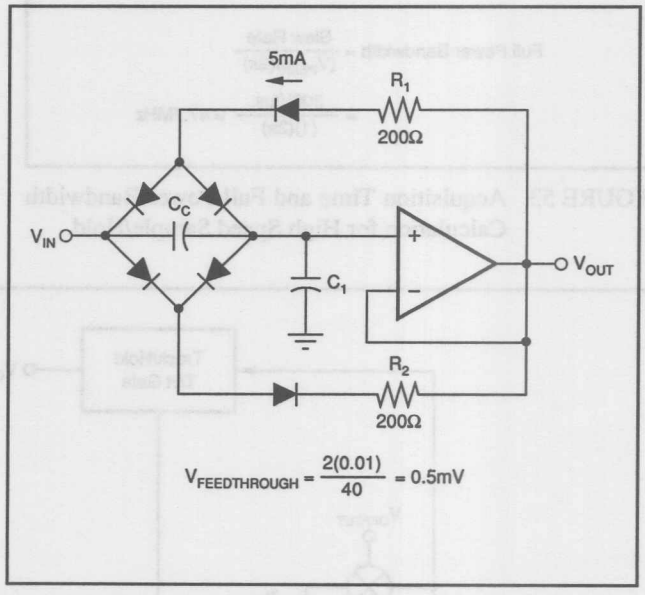


FIGURE 52. Bridge in Off State.

AND FULL POWER BANDWIDTH

To complete the comparison a calculation will be made of the acquisition time and the full power bandwidth using methods previously demonstrated. The fastest sample and hold is designed to handle only a 2V waveform so the equivalent 0.01% error is 0.2mV. Assume that the amplifier bandwidth is 80MHz with a slew rate of 300V/µs. Figure 53 shows this calculation.

As previously mentioned, one of the most common applications for a track and hold is to precede an analog to digital converter for purposes of reducing the aperture time. Towards the end of the section on digital to analog converters another application will be shown on how a track and hold can be used to "deglitch" a DAC. A third application is how a track and hold can be used to make a precise peak detector. Figure 54 shows the block diagram of a peak detector. The

$$\text{Amplifier will slew until slew rate} = \frac{E}{T}$$

$$T = \frac{1}{2\pi B\omega} = \frac{1}{2\pi\ 80 \times 10^6} = 1.99\text{ns}$$

$$E = T \cdot \text{Slew Rate} = 1.99 \times 10^{-9} \cdot 300\text{V}/\mu\text{s} = 0.6\text{V}$$

$$\text{Acquisition Time} = \frac{\text{Input} - E}{\text{Slew Rate}} + T \ln \frac{E}{\text{Error}}$$

$$= \frac{2 - 0.6}{300\text{V}/\mu\text{s}} + 1.99\text{ns} \ln \frac{0.6}{0.0002}$$

$$= 4.7\text{ns} + 15.9\text{ns} = 20.6\text{ns}$$

$$\text{Full Power Bandwidth} = \frac{\text{Slew Rate}}{(V_{PEAK})(2\pi)}$$

$$= \frac{300\text{V}/\mu\text{s}}{(1)(2\pi)} = 47.7\text{MHz}$$

FIGURE 53. Acquisition Time and Full Power Bandwidth Calculation for High Speed Sample/Hold.

locating the point in time where the peak occurs. The output of the comparator allows the track and hold to track the signal until the peak is located. Once the peak occurs the comparator reverses state thereby placing the track and hold in the hold mode, which stores the peak amplitude for further processing.

DIGITAL-TO-ANALOG CONVERTERS

The schematic shown in Figure 56 is typical of the architecture of a high speed digital to analog converter. The digital to analog converter shown in Figure 56 is ECL compatible but shares many of the same elements of TTL compatible DACs as the core current steering mechanism is similar. Most recently, CMOS technology has been used to design high performance digital to analog converters. CMOS DACs have been designed with 12-bit resolution but have not been able to achieve the speeds that can be achieved with bipolar technology. Recently GaAs technology has been used to design exceptionally high speed DACs, with settling times in the 1ns vicinity, and in some ways are similar in topology to the way a bipolar design would be approached. Therefore, describing the design considerations for a high speed digital to analog converter implemented with bipolar technology will serve as a means to understand the design considerations for a high speed, high resolution DAC. Along with the high speed switch, other elements such as the "servo amp" and reference circuitry are also representative of other high precision digital to analog converters ranging in settling times down to 5ns and resolutions to 16 bits. The particular DAC that will be described has 12 bits of resolution with a settling time to ±0.01% accuracy in 25ns and is capable of operating over the temperature range from –55°C to +125°C. This converter is representative of what can be achieved with modern monolithic processing. The DAC is built on a 20V process that contains 1GHz NPNs along with compatible thin film resistors. As will be described later, the thin film resistors are laser-trimmed to achieve true 12-bit linear-

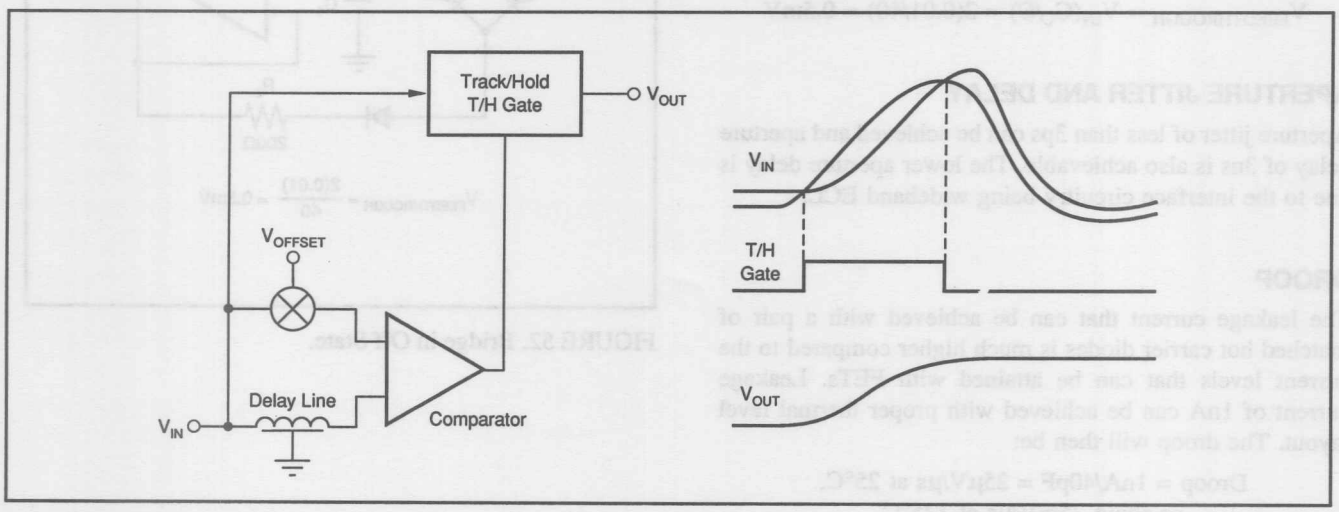


FIGURE 54. Peak Detector.

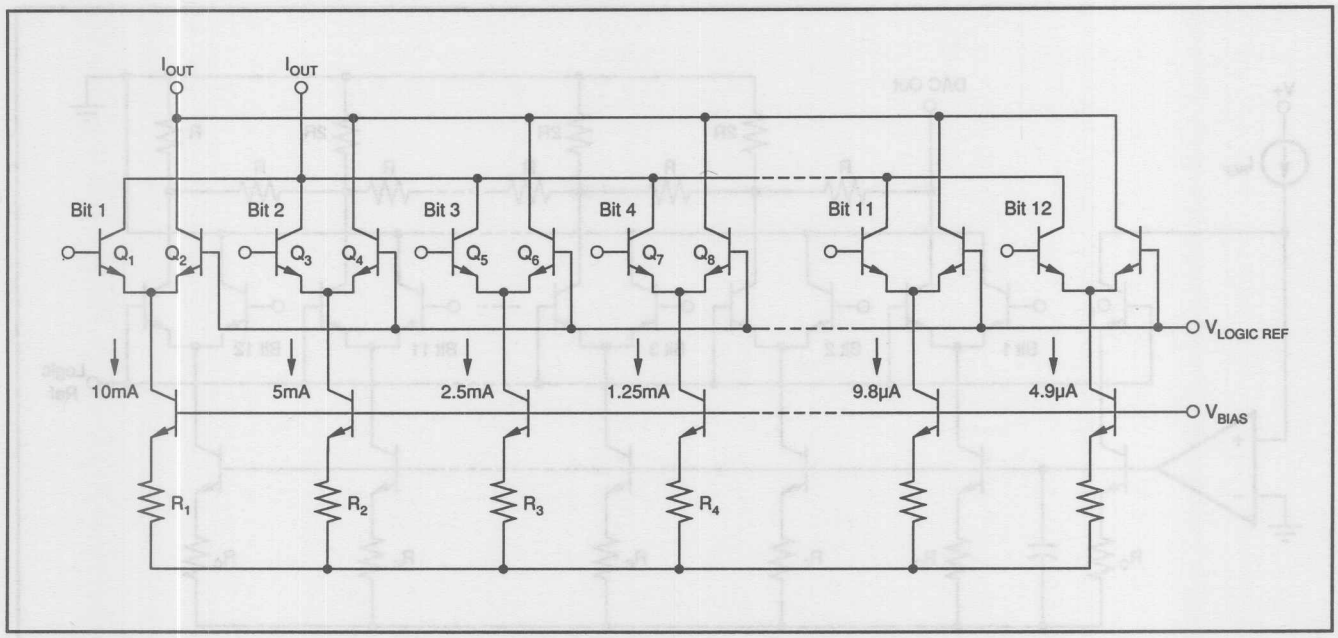


FIGURE 55. Binarily Weighted Current Source DAC.

ity over a very wide temperature range. Furthermore, the thin film resistors are capable of maintaining their accuracy over long periods of time and represent a reliable technique for producing a high speed, high resolution, low cost digital to analog converter. The converter that will be described is entirely monolithic as it contains the precision current switches, servo amp, and low drift references. Only a few capacitors that are too large to be integrated and are needed for filtering and bypassing are left off of the chip.

The converter consists of twelve switches that are driven in a non-saturating manner. In order to steer the current as fast as possible through the output switch, it is very important to pay careful attention to avoid saturation; once a transistor saturates, the recovery time can easily increase by a factor of twenty or more. There are many ways to approach the design of this kind of a DAC. The detailed design considerations will be described, but before that explanation will be given, an overview of different DAC architectures is offered. One method would be to binarily weight the individual bit switches and then sum the outputs as shown in Figure 55. High accuracy can not be achieved using this method as it is difficult to accurately match the separate current sources and switches over such a wide range of currents. If the full scale output current of the 12-bit DAC were 10mA, the weight of the LSB would be 4.9µA which would be too low to achieve high speed switching. Additionally, with all those switches in parallel, the output capacitance would become quite high. The only redeeming feature of a binarily weighted DAC is that there would be no wasted current and the net power dissipation for this type of digital to analog converter would be the lowest as compared to other design approaches.

Another way to approach this design would be to have twelve equally weighted current switches. The twelve equally weighted current switches would then be binarily weighted by passing their currents through an R-2R ladder as shown in Figure 56. Twelve equally weighted current sources could then be precisely matched using a "servo mechanism" control loop as shown in Figure 57. The servo loop is able to cause the value of the output current to be exactly (within circuit tolerances) the same as the reference current. A reference current is connected to the positive input of the op amp and the collector of transistor Q_1. The same reference current then passes through Q_1 and emerges as emitter current by the addition of base current. The emitter current of Q_1 then becomes the collector current of Q_2. The voltage current developed across the base to emitter junction of Q_2 and the voltage drop across R_1 create an identical current through Q_3. The collector current of Q_3 becomes the emitter current of Q_5 which in turn emerges from Q_5 as the output current. Examination of the analysis shown in Figure 57 shows that if all the transistors and resistors are well-matched, the output current will be equal to the reference current. This is an ideal technique to be implemented in a monolithic process, as it is very practical to make transistors and resistors identical. A more detailed analysis of error sources will be shown later. A digital to analog converter designed in this manner would have the lowest glitch performance but at the expense of the highest power dissipation. "Glitch" refers to the uncertain DAC output that occurs when the digital input changes and the DAC switches do not change simultaneously. More will be given on the design of low glitch DACs toward the end of the section on high speed digital to analog converters.

Practical digital to analog converters are a mixture of the two previously described examples as shown in Figure 60. Starting with the MSB (most significant bit), the currents are binarily weighted until the current becomes low enough to

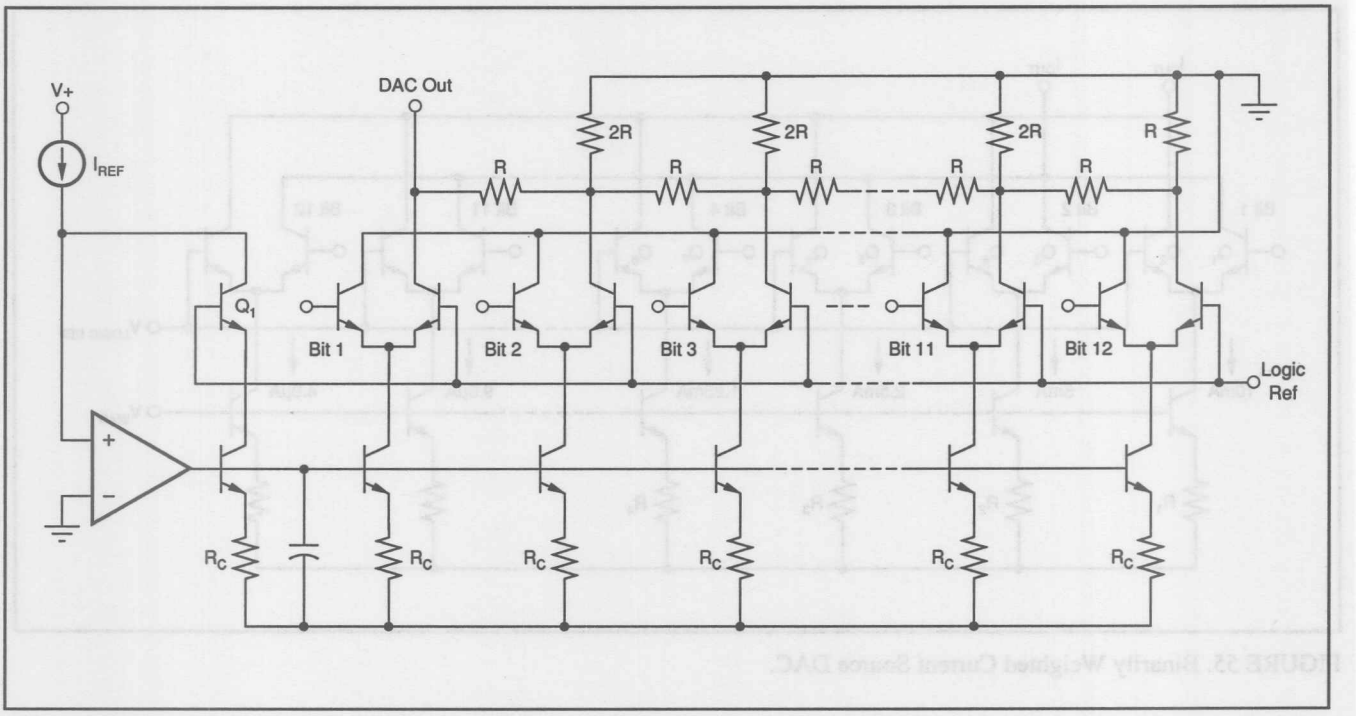
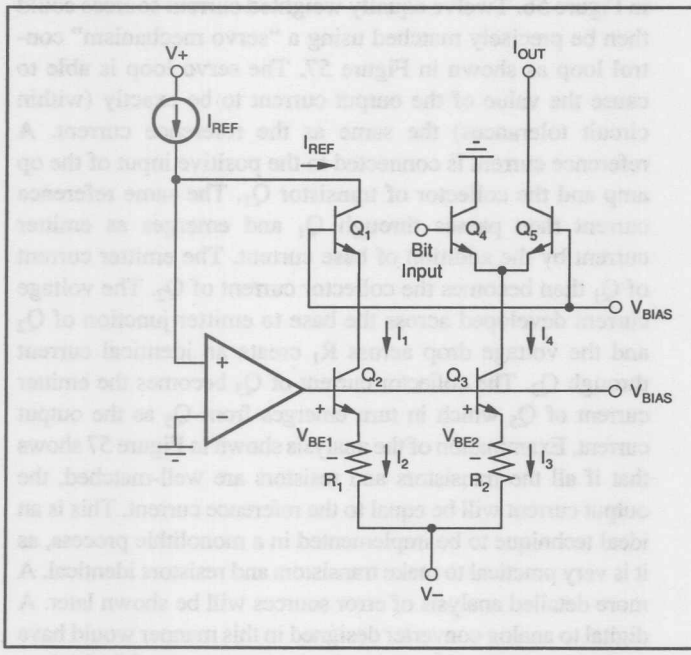


FIGURE 56. High Speed DAC with Equally Weighted Currents.



$$I_1 = \frac{\beta + 1}{\beta} I_{REF}$$

$$I_2 = \left(\frac{\beta + 1}{\beta}\right)^2 I_{REF}$$

$$V_{BE1} + I_2R_1 = V_{BE2} + I_3R_2$$

If $V_{BE1} = V_{BE2}$ and $R_1 = R_2$,

$$I_2 = I_3$$

$$I_4 = \left(\frac{\beta}{\beta + 1}\right) I_3$$

$$I_{OUT} = \left(\frac{\beta}{\beta + 1}\right) I_4 = \left(\frac{\beta}{\beta + 1}\right)^2 I_3 = \left(\frac{\beta}{\beta + 1}\right)^2 I_2$$

$$I_{OUT} = \left(\frac{\beta}{\beta + 1}\right)^2 I_2 = \left(\frac{\beta}{\beta + 1}\right)^2 \cdot \left(\frac{\beta + 1}{\beta}\right)^2 I_{REF}$$

$$I_{OUT} = I_{REF}$$

FIGURE 57. DAC Servo Loop.

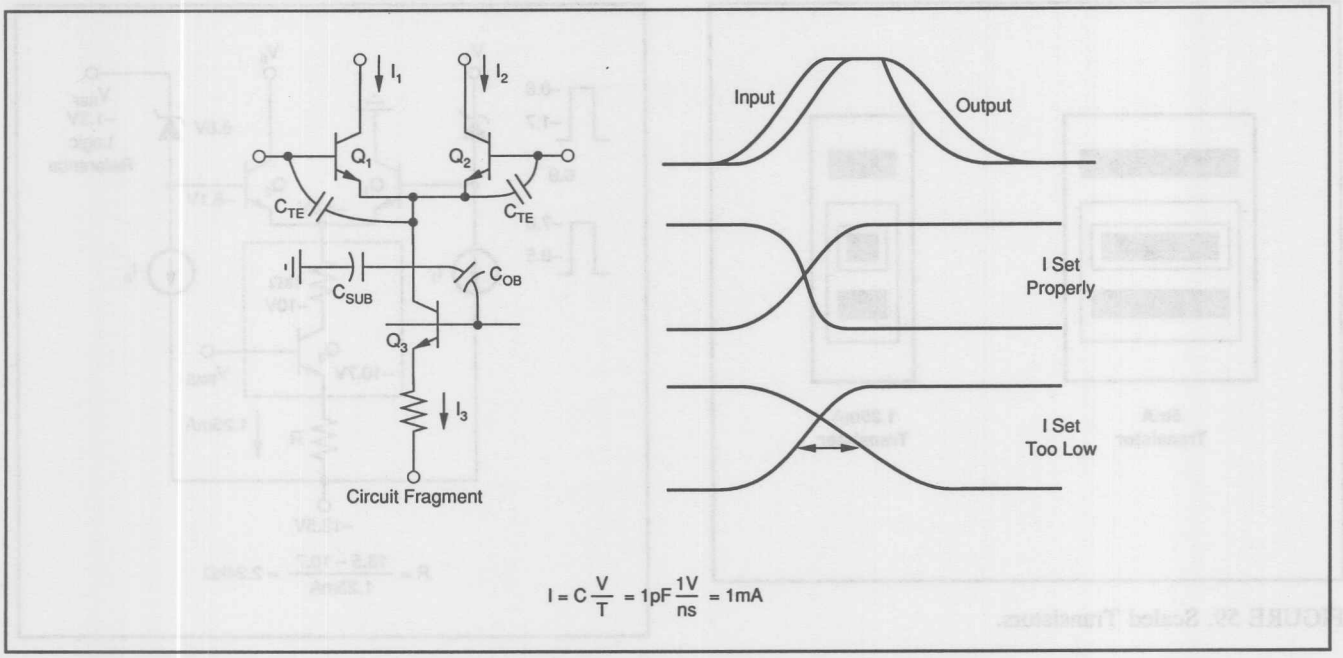


FIGURE 58. DAC Switching.

effect switching speed. Even though the MSB currents are not the same value as the LSB currents, matching is maintained as the current density is made to be the same. The current density is maintained by making the transistors that are to conduct larger currents physically larger, thereby causing the voltage drop associated with the transistor to be the same. This is similar to placing transistors in parallel.

Figure 58 shows a diagram depicting the switching of one DAC current switch. This type of an emitter coupled pair is capable of switching very rapidly in response to a positive going input logic change as Q_1 acts as an emitter follower which is capable of driving the capacitance attached to the common mode where the emitters of Q_1 and Q_2 are joined. If the base of Q_1 is driven from and ECL input the speed at the emitter of Q_1 is determined by the rate of change of the ECL input of about 1V/ns. To obtain low glitch performance it is necessary to have the DAC propagation delay to be equal for negative as well as for positive logic changes. Therefore, when the logic input makes negative going transition the current supplied by current source Q_3 will have to provide enough current to drive the node capacitance to allow the voltage change at the emitters to track the negative going input signal. Some digital to analog converter designs will drive the current switch differentially, which means that either side of the switch is capable of actively driving the node capacitance instead of depending upon the current that is being switched. While this approach solves the problem of providing high current for the lower order bits, it does so at the expense of providing a differential driver. If done so externally, the chip would have to have an additional twelve inputs as well as require that the user supply differential inputs. Alternatively, a differential driver could be placed on the chip at the expense of loss in speed and extra circuit complexity. This particular approach is taken to emphasize simplicity. Returning to the design at hand: the amount of current necessary to follow a negative going logic change is given by the formula (see Figure 58):

$$I = C(V/T)$$

where C is the total node capacitance and (V/T) is the rate of change of the logic input.

Substituting:

$$I = 1pF(1V/ns) = 1mA$$

An extra amount of current is provided to assure equal propagation delays in both directions so that the minimum current that is set for the lower order bits is 1.25mA. The MSB current switch is scaled to be four times this value of 5mA and the next bit, Bit 2, is scaled at twice the minimum, or 2.5mA. Bits 3 through 12 are then set at 1.25mA. Bits 1 through 3 are connected together while Bits 4 through 12 are passed through the R-2R ladder to establish the proper binary weighting. In order to maintain high accuracy, Bits 1 and 2 are also physically scaled. Physical scaling can be thought of as placing unit current switches in parallel, thereby allowing proper matching and compensation by the servo amp. Figure 59 shows how this is done.

Typically the output resistance of the ladder is 250Ω (see Figure 60), so the DAC output voltage swing will be 2.5V. For greatest flexibility there is a resistor connected to the positive reference that allows that DAC output to be able to swing ±1.25V around ground. In order to accommodate the negative level of –1.25V, care must be taken so the output transistor is not saturated. Figure 61 shows a circuit diagram that includes the parasitic collector resistances which must be accounted for. This diagram also shows the translation

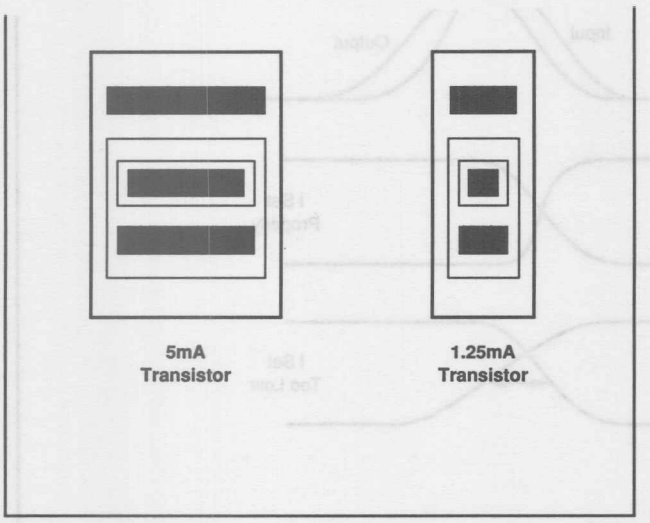


FIGURE 59. Scaled Transistors.

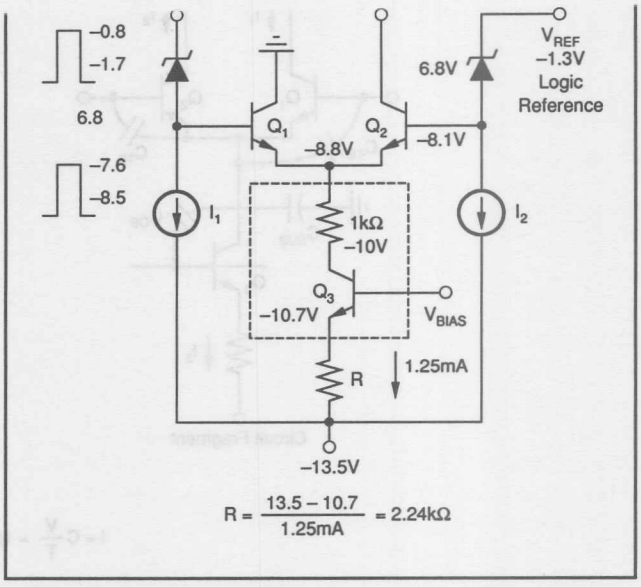


FIGURE 61. DAC Bias Voltages.

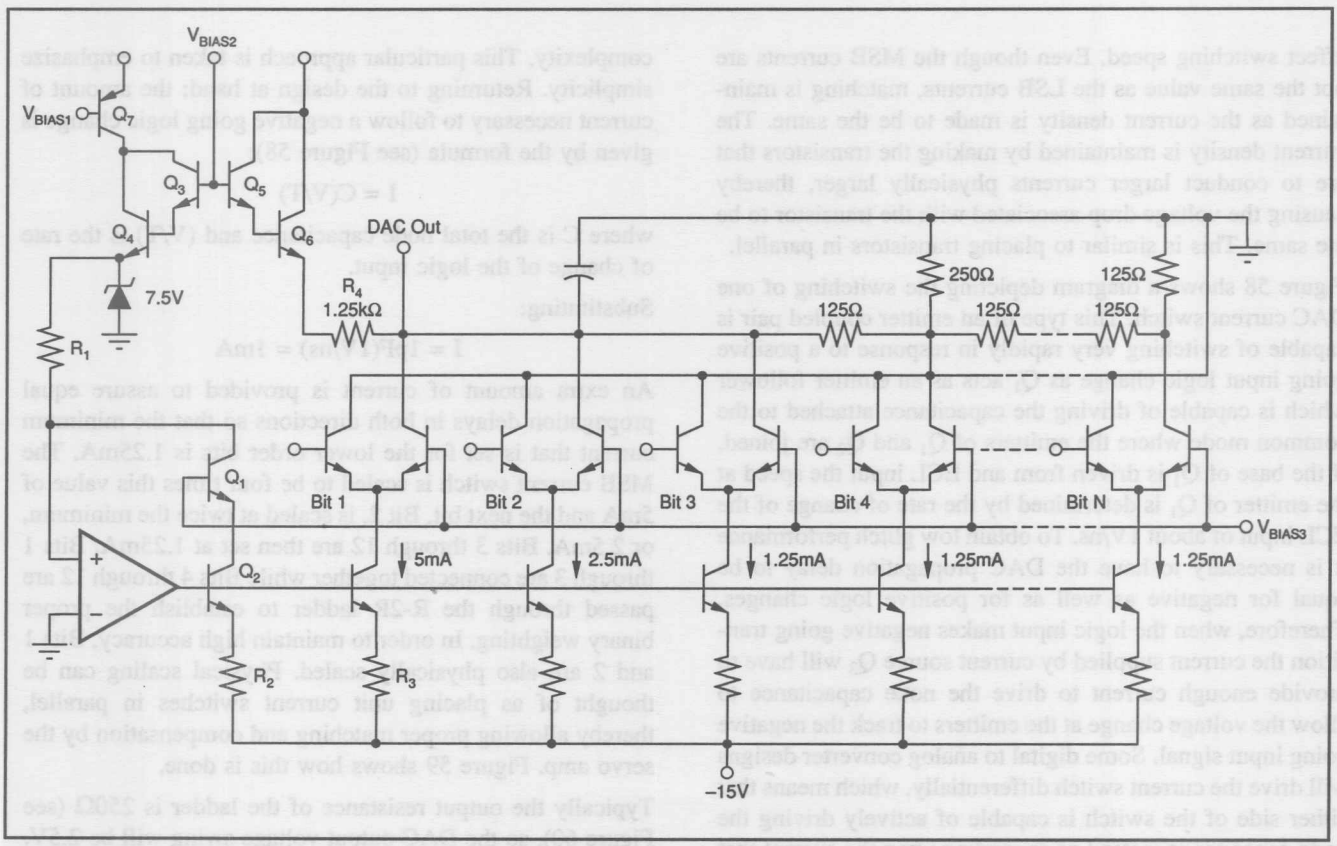


FIGURE 60. Practical DAC.

zener so that the DAC switch can properly interface to the ECL level inputs. A 6.8V zener is a useful voltage translation device as the impedance level is low, about 50Ω, which is necessary for maintaining high speed. When the ECL level is at a low of –1.7V, the voltage at the base of Q_1 will be –8.5V. Since the voltage at the base of Q_2 is –8.1V, Q_1 will be off and Q_2 will be on. Even though Q_1 is slightly forward biased, the amount of conduction is tolerable for 12-bit applications. The voltage at the emitter is then –8.8V when Q_2 is on. The saturation resistance for the transistors used in this DAC design is 1kΩ and since the current level is 1.25mA, the voltage at the actual collector is –10V. Under worst case conditions, the base voltage should not be allowed to become greater than –10V or the onset of saturation will begin. Therefore, under these conditions the emitter of Q_3 will be at –10.7V. It is always desirable for maximum accuracy (as will be shortly seen) to create as large an emitter degeneration voltage as possible. The largest voltage tolerable will be when the emitter voltage is –10.7V and the power supply voltage, which is nominally –15V, is at its lowest of –13.5V. Under these conditions the emitter degeneration voltage will be: 13.5 – 10.7 = 2.8V. The emitter degeneration resistance will then be (2.8V)/(1.25mA) = 2.24kΩ.

Refer to Figure 62, which shows an analysis of the principal error-producing elements of a typical DAC switch and current source. There are three error sources that can be eliminated by adjustments after the DACs are assembled and two sources of error that must be eliminated by design. The three sources of error that can be adjusted to zero or "trimmed out" are the beta and V_{BC} matching of the transistors and the matching of the thin film resistors. While these error producing effects can be corrected at room temperature, they will change over temperature. As an example: The beta of a transistor will be assumed to be 150 and to have a temperature coefficient of +7000ppm/°C. An uncompensated transistor collector current will experience a beta error of (7000/C)/150 = 47ppm/°C. This means that at room temperature the ratio of the collector to emitter current will be 150/151 = 0.99348 and at 125°C the ratio will be 0.99609. Due to the compensation action of the servo-loop, experience has shown that a further reduction by a factor of 200 can be attained so that the net drift over temperature due to this effect is 0.24ppm/°C. If transistors Q_2 and Q_3 are carefully matched, their V_{BE}s will track each other to 1μV/°C and the effect upon the accuracy of the switch will be (1μV/°C)/2.8V = 0.36ppm/°C. Lastly, resistor matching of 0.5ppm/°C is achievable if the resistors are laid out properly. Adding these three effects yields a net current source drift over temperature of:

$$\text{Change over temperature} = (2)\text{Beta} + V_{BE} + \text{Resistor}$$
$$= 0.47 + 0.36 + 0.5 = 1.33\text{ppm/°C}$$

Assuming that these errors can be laser-trimmed to arbitrary accuracy at room temperature, any bit switch over a 100°C temperature change will experience a 133ppm change which implies that if these assumed tracking values were attained

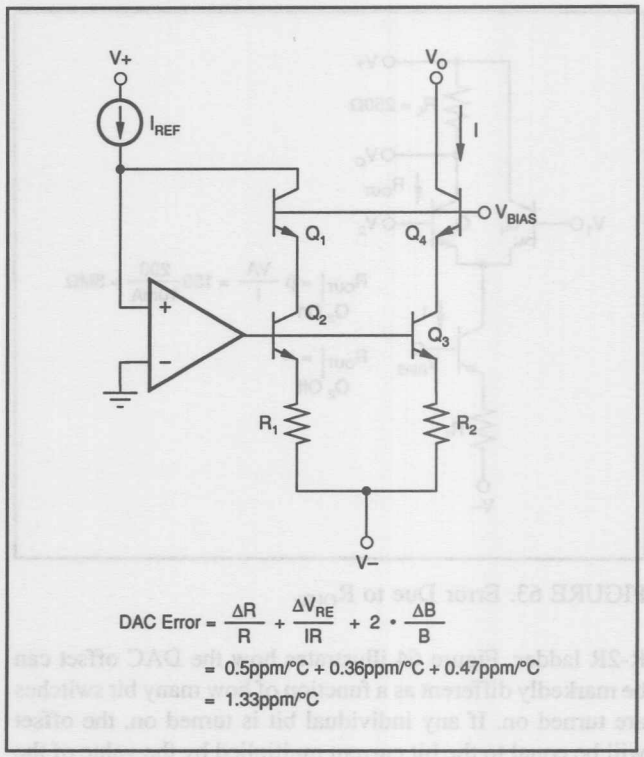


FIGURE 62. Trimmable DAC Errors.

it would be difficult to produce with high yield a DAC that had ±1/2LSB linearity. The art of building high accuracy digital to analog converters is the ability of design, layout, processing, and manufacturing engineers to control the previously described elements to sufficient accuracy. In fact it is possible to manufacture 12-bit DACs from –55°C to +125°C within ±1/2LSB accuracy and the above assumed parameters are achievable.

There are two other sources of error that can only be eliminated by proper design: the output impedance and superposition error. Due to the cascoded nature of the DAC switch, the output resistance is given by (see Figure 63):

$$R_{OUT} = (\text{Beta})(V_A/I) \quad (V_A = \text{Early voltage})$$
$$= (150)(200/10)$$
$$= 3\text{Meg}$$

Since the ladder impedance is 250Ω, the output resistance represents an error of 83.3ppm which is below the error budget of 122ppm needed for a 12-bit design. The output resistance causes a non-linear error since there is a difference in this value when the switch is on compared to the off value.

The last error source that needs to be considered is superposition error. Superposition error occurs when the individual bits do not add up to the proper sum defined by their values when they are individually turned on. Superposition error can have many causes, but one of the most prevalent causes for the type of DAC being discussed is the offset created by the resistance in the return line of the

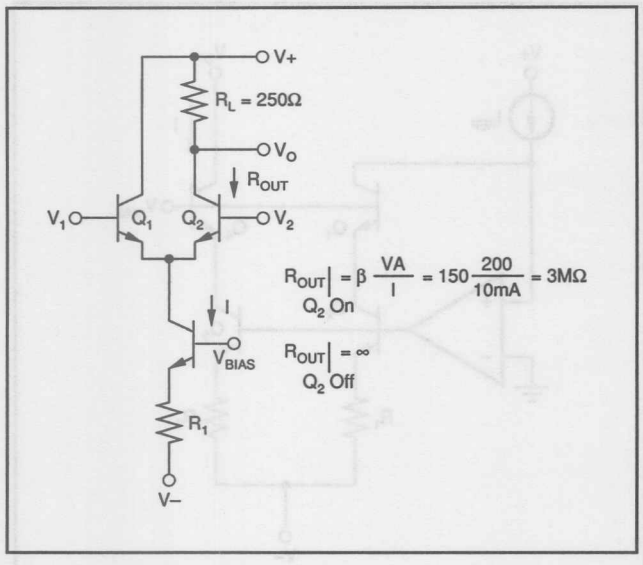


FIGURE 63. Error Due to R_{OUT}.

R-2R ladder. Figure 64 illustrates how the DAC offset can be markedly different as a function of how many bit switches are turned on. If any individual bit is turned on, the offset will be equal to the bit current multiplied by the value of the resistance in the ladder return. As long as only one bit switch is turned on the offset voltage will be constant. However, when multiple bit switches are turned on this error will not be constant. Take the case when the DAC makes a 1LSB transition around the MSB. When the MSB is on, the offset voltage is the small value defined by only one switch being on. However, 1LSB below the MSB occurs when the lower eleven bits are turned on with the MSB off, and this offset voltage will now be eleven times greater compared to when only the MSB is turned on. This effect can be minimized by making the ladder return impedance as small as possible and by returning the opposite side of the bit switch back to the same point as the on side is to be returned to. This has the effect of keeping this offset voltage constant for any digital code combination. It is important to sense the voltage at the true reference point on the ladder to achieve maximum when the DAC is trimmed at the factory level.

This digital to analog converter has the capability of settling to ±0.01% accuracy for a full scale change in about 26ns. The settling time is primarily determined by the ladder impedance and the total capacitance that is accumulated on the output node. The combined capacitance of the R-2R ladder, the offset resistor, the output transistors, and the load capacitance is about 10pF. The propagation delay from the digital input to the actual current switch is 3ns. The remaining part of the settling time is due to the voltage settling of the output time constant formed by the ladder impedance of 250Ω and the node capacitance of 10pF which forms a 2.5ns time constant. Settling to ±0.01% accuracy requires (2.5) ln(1/0.01%) = 23ns, and when the digital propagation delay is added to the voltage settling, the total becomes 26ns. Achieving fast and accurate settling times requires paying attention to several other aspects of the design that will be described. Improperly designed reference and servo-amp circuitry can lead to a DAC that will not achieve the previously calculated 26ns. Figure 65 shows a path of how the digital input coupled onto the fence line which determines the value of the bit currents. The servo operational

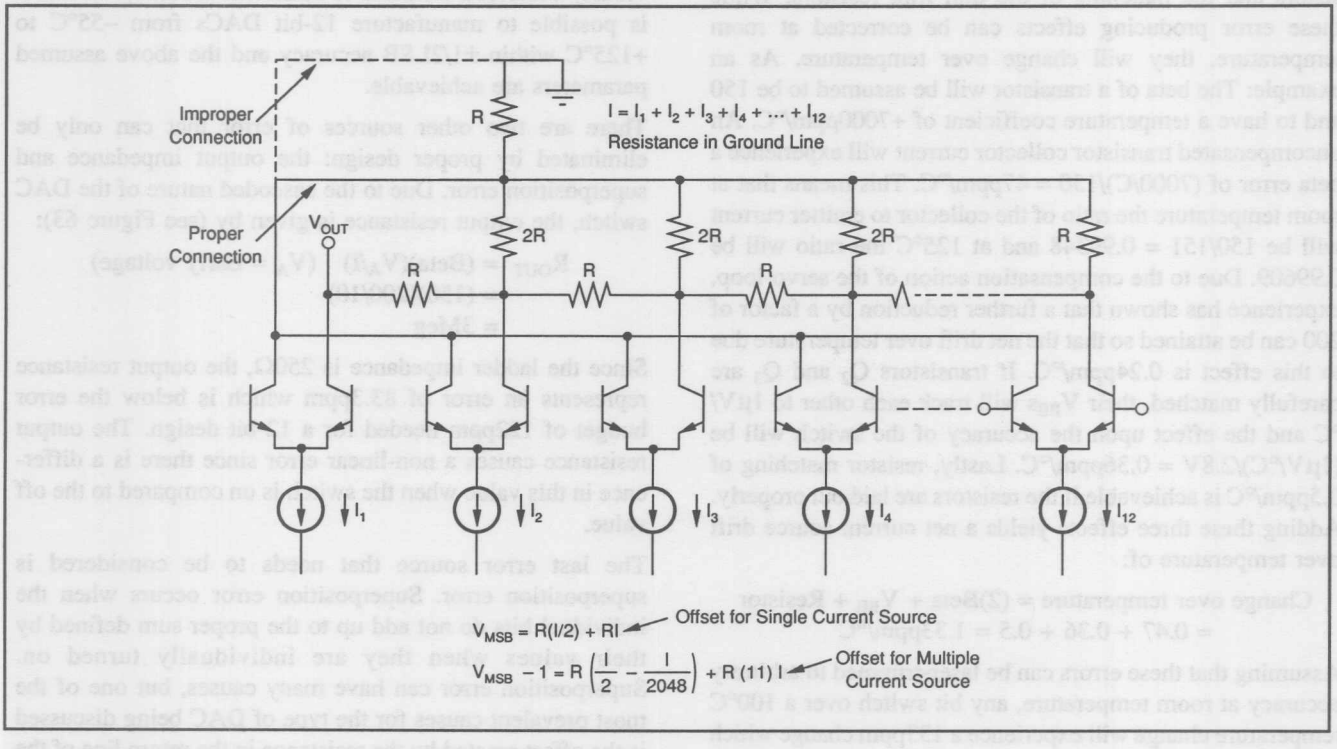


FIGURE 64. Superposition Error.

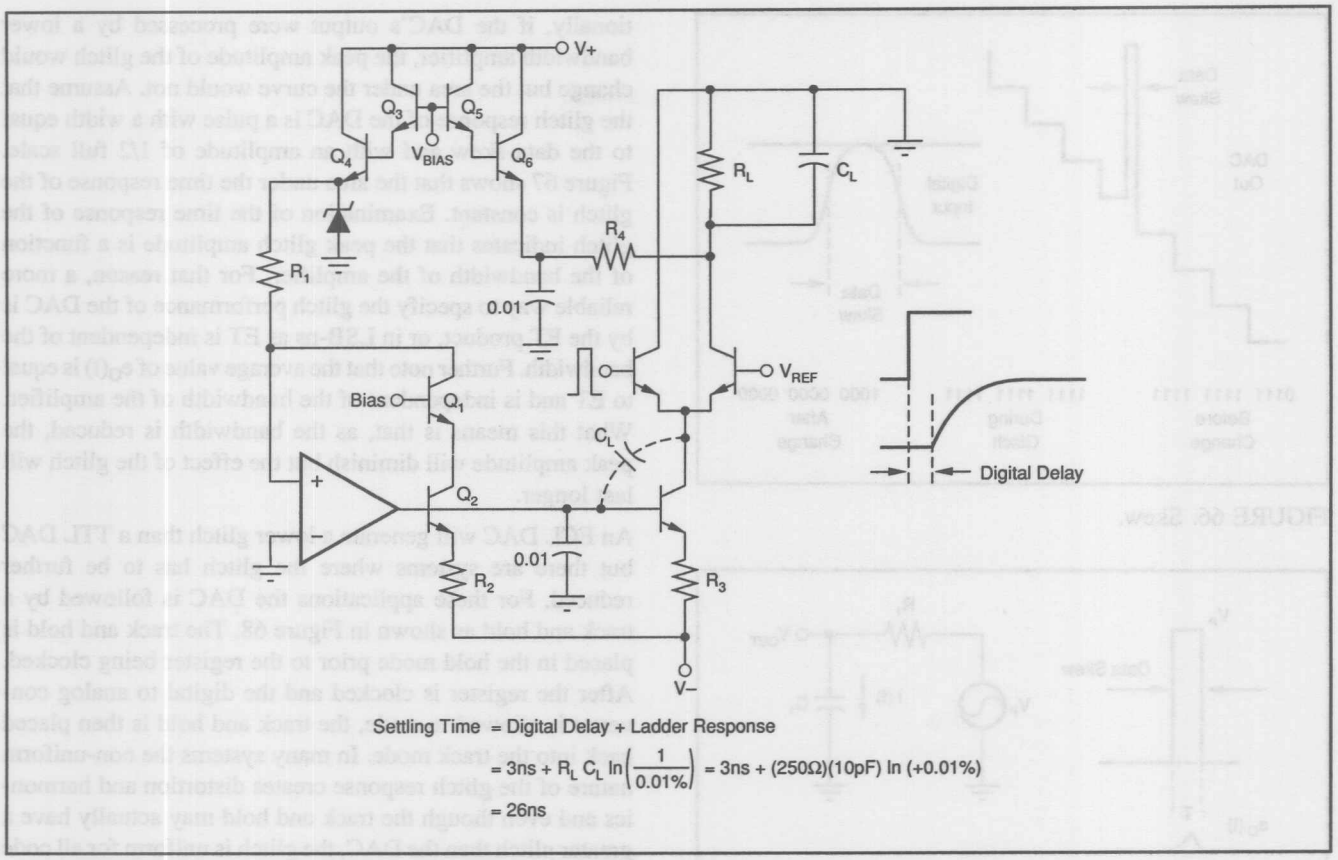


FIGURE 65. Settling Time.

amplifier would have to have a bandwidth of 25MHz to 50MHz to be able to respond and to settle to the capacitively injected transient onto its output. This is not a practical requirement since only the fastest op amp can settle in 24ns even if separately designed and not part of a DAC chip. A more practical solution would be to place a 0.01pF capacitor on this reference line to absorb the transient and then design a low frequency op amp that was stable.

The switches that form the DAC are unipolar and in its natural form the DAC has an output that swings from ground to some negative voltage. For maximum flexibility it is desirable to have a bipolar DAC which requires a means of translating the output voltage in a positive direction. This is accomplished by connecting a 1.2kΩ resistor back to the 7.5V reference voltage. Examination of Figure 65 reveals a buffer compound emitter follower that is used to isolate the low current offset resistor. This buffer isolates the reference offset current change from entering the low bandwidth reference and servo-amp circuitry. A 0.01μF capacitor is added to the isolation circuit to prevent transients from entering the low frequency servo-loop.

Ordinarily a designer would not consider the use of an ECL DAC but there are several reasons that the DAC previously described will have superior performance compared to a TTL DAC. Briefly, ECL has a lower logic delay than TTL, is less noisy, and ECL data registers have lower data skew.

Data skew occurs when all the digital inputs do not change at exactly the same time and is defined as the difference between $T_{PD}(+)$ and $T_{PD}(-)$. $T_{PD}(+)$ is the positive going propagation delay while $T_{PD}(-)$ is its negative counterpart. As an example of this phenomenon, consider the major carry change for a 12-bit DAC. For a 1LSB change around the MSB, the code would change from 0111 1111 1111 to 1000 0000 0000 under ideal conditions. With the presence of data skew all bits might not change at the same time and an intermediate code could exist. Consider what happens if the MSB changed more rapidly compared to the rest of the bits, so that the code transition pattern would be:

0111 1111 1111 → 1111 1111 1111 → 1000 0000 0000
code before intermediate code code after

See Figure 66 which shows a timing diagram depicting data skew. Therefore, for a period of time equal to the data skew, the DAC output would start to head in the direction of an output that was considerably different than a 1LSB change from the previous code. This large transient-like waveform that is created by data skew is often referred to as a DAC output "glitch." A convenient way to specify the glitch is by measuring the area of the glitch in units of LSB-ns. This is a more effective method for specifying the glitch than if it were defined as a voltage amplitude, as one could not compare DACs with different full scale output levels. Addi-

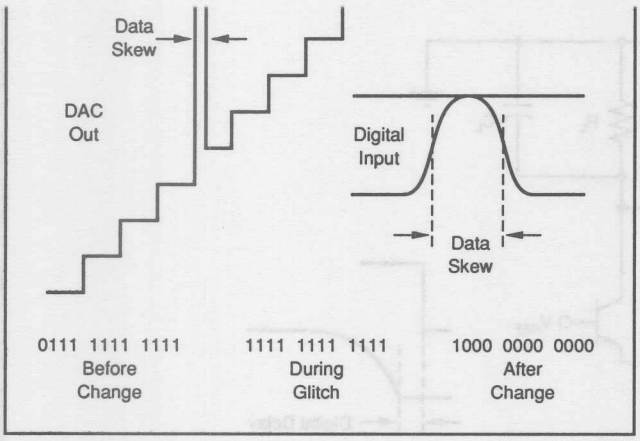


FIGURE 66. Skew.

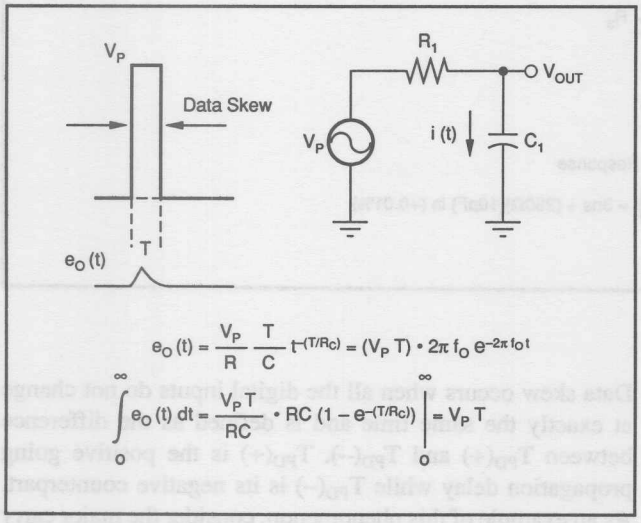


FIGURE 67. Glitch Response.

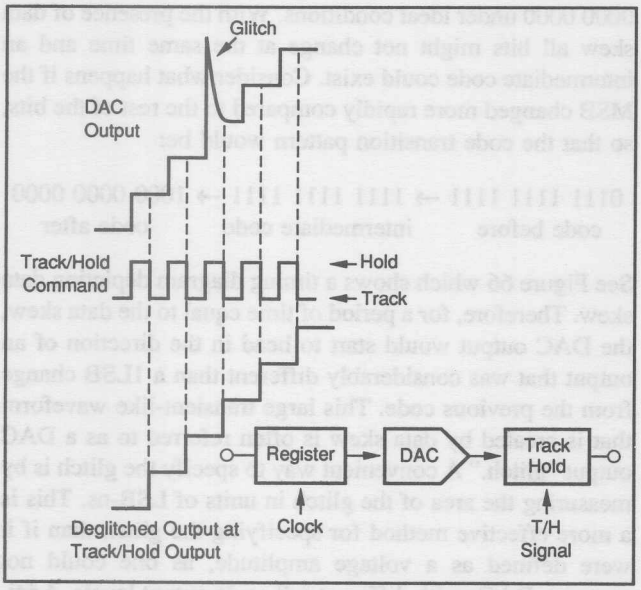


FIGURE 68. Deglitched DAC.

bandwidth amplifier, the peak amplitude of the glitch would change but the area under the curve would not. Assume that the glitch response of the DAC is a pulse with a width equal to the data skew and with an amplitude of 1/2 full scale. Figure 67 shows that the area under the time response of the glitch is constant. Examination of the time response of the glitch indicates that the peak glitch amplitude is a function of the bandwidth of the amplifier. For that reason, a more reliable way to specify the glitch performance of the DAC is by the ET product, or in LSB-ns as ET is independent of the bandwidth. Further note that the average value of $e_O(t)$ is equal to ET and is independent of the bandwidth of the amplifier. What this means is that, as the bandwidth is reduced, the peak amplitude will diminish but the effect of the glitch will last longer.

An ECL DAC will generate a lower glitch than a TTL DAC but there are systems where the glitch has to be further reduced. For these applications the DAC is followed by a track and hold as shown in Figure 68. The track and hold is placed in the hold mode prior to the register being clocked. After the register is clocked and the digital to analog converter is allowed to settle, the track and hold is then placed back into the track mode. In many systems the non-uniform nature of the glitch response creates distortion and harmonics and even though the track and hold may actually have a greater glitch than the DAC, the glitch is uniform for all code combinations and will manifest itself at the system level as an offset or gain error but not as a code dependent non-linearity.

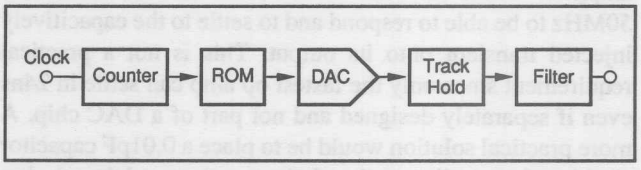


FIGURE 69. Arbitrary Waveform Generator.

Figure 69 shows a system with a high speed digital to analog converter that can be used to generate a precise arbitrary waveform. While there are many ways to accomplish this with lower frequency circuitry, the use of a high speed DAC is an attractive alternative. A high frequency DAC is capable of being updated at a 50MHz rate, which will substantially ease the subsequent analog filtering requirements. Since the waveform is effectively sampled at a 50MHz rate it would be possible to create a waveform with frequency components up to the Nyquist rate of 25MHz. Generating an arbitrary waveform is the inverse of digitizing a waveform with an analog to digital converter and the same sampling considerations apply. Figure 70 shows an arbitrary analog waveform that is to be synthesized. If the waveform were sampled at periodic intervals, the synthesized waveform would be created. The synthesis procedure consists of mathematically computing the closest 12-bit approximation to each sample point which would be used to generate the

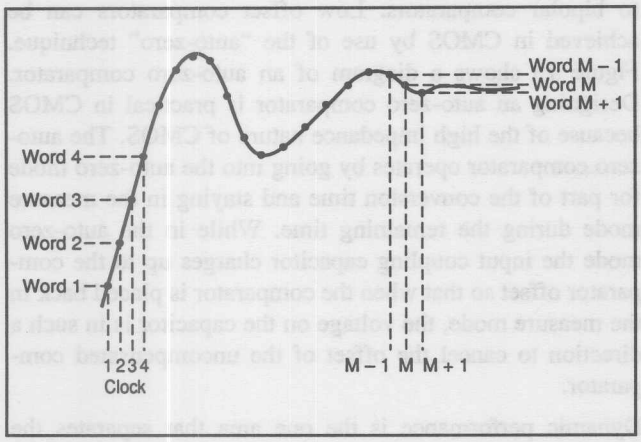


FIGURE 70. Arbitrary Waveform.

encoding table for the ROM. Refer to Figure 69 which shows a simplified block diagram of a system that will generate a synthesized waveform. The sample points would correspond to the ROM address while the ROM output would be the associated code at each one of these addresses.

DIFFERENT HIGH SPEED ADC ARCHITECTURES

This section will compare the performance features, and trade-offs, of three commonly found architectures of high speed analog to digital converters to gain an understanding of how resolution, speed, and complexity interact in the design of an analog to digital converter. These three architectures form the basis of most high speed ADCs that are on the market, although there are many variations of these basic circuit arrangements due to the nature of particular technologies. It is useful, though, to gain an understanding of the architectures in their most elementary form before an appreciation of the variations can be gained. Each architecture has distinct characteristics that need to be properly understood to maximize the benefits of the chosen analog to digital converter with the application.

The three types of designs that will be compared are flash, successive approximation, and sub-ranging. Each method of conversion has strengths and weaknesses which will be clearly contrasted. This section will compare the relative merits of each converter with respect to accuracy, dynamic characteristics, aperture effects, simplicity, and cost. A description of each analog to digital converter will first be given which will then be followed by the performance features of each architecture.

FLASH ADC

The fastest of all types of high speed analog to digital converters, and perhaps the easiest to understand, is the flash or parallel type of converter. The flash converter is considered to be the fastest because the conversion takes place in a single cycle, hence the name "flash." The resolution of flash converters is typically 8 bits, although expensive or experimental designs have been reported with up to 10 bits of resolution. Flash converters are very appealing to monolithic designers due to the highly repetitive nature of the design. Refer to Figure 71 which shows a block diagram of a flash converter. Speeds of up to 500MHz have been achieved and conversion times of up to 200MHz are readily available on the commercial market. Bipolar technology is used for the fastest designs with CMOS achieving conversion rates of up to 30MHz. The resolution of a flash converter tends to be limited to 8 bits due to the fact that the amount of circuitry doubles every time the resolution is increased by 1 bit. The input comparators are arranged in a "thermometer" code fashion with each comparator's reference biased 1LSB higher that of the adjacent comparator. The reference for each one of the comparators is derived

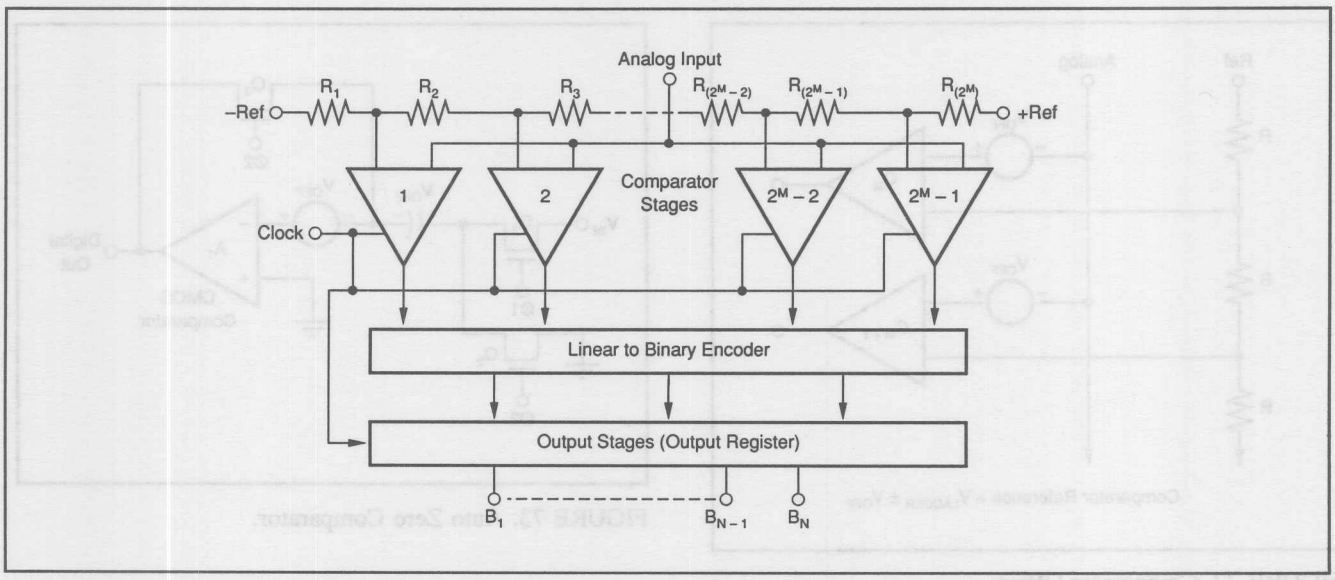


FIGURE 71. Block Diagram of a Flash Encoder.

from a series connection of a string of resistors that is placed between the negative and positive reference. This resistor string is monotonic by design but it is possible for the entire flash converter not to be monotonic due to the comparator offset. This condition could possibly occur if the reference voltage is set too low thereby enabling the offset of the comparator to dominate the effective reference level which is the sum of each. Figure 72 illustrates this point. Suppliers of flash converters are able to produce monotonic results and still maintain LSB weight of 5mV, although LSB weights of 10mV are required for ±1/2LSB linearity. The output of the comparators must be converted to a more economical digital code to be convenient to use. The thermometer code is typically converted to a conventional binary output. To achieve high sampling rates, digital pipelining is often employed in the design of the flash converter. This has the benefit of enabling a new sample to take place before the previous binary code has been formed.

The design of a comparator that is often employed in a flash converter is somewhat different compared to the design of a stand-alone comparator. The comparator input stage is configured to have a low gain state while in the tracking mode, and a high gain state while it is making the transition to the held state, the held state being the result of the comparison between the two inputs at the moment of sampling. Sampling takes place when a strobe pulse initiates positive feedback thereby causing regenerative action to take place which then sets the output of the comparator based upon the condition of the input. This method of design is necessary to achieve the simplicity required for a high resolution flash converter. Figure 22 shows a circuit diagram of a typical comparator stage of a flash ADC.

As previously mentioned, CMOS technology is employed in the design of low power flash converters with conversion rates of up to 20MHz. One of the drawbacks of CMOS comparators is that their offsets are much higher compared to bipolar comparators. Low offset comparators can be achieved in CMOS by use of the "auto-zero" technique. Figure 73 shows a diagram of an auto-zero comparator. Designing an auto-zero comparator is practical in CMOS because of the high impedance nature of CMOS. The auto-zero comparator operates by going into the auto-zero mode for part of the conversion time and staying in the measure mode during the remaining time. While in the auto-zero mode the input coupling capacitor charges up to the comparator offset so that when the comparator is placed back in the measure mode, the voltage on the capacitor is in such a direction to cancel the offset of the uncompensated comparator.

Dynamic performance is the one area that separates the performance of one flash converter from that of another. Dynamic performance is a measure of how a flash converter is able to accurately digitize a high frequency signal. This requires that the user understand how aperture jitter, aperture delay distortion and input bandwidth affect overall system performance. Input bandwidth is easily understood as this specification is similar to that of any band-limited device. The input bandwidth of a flash converter consists of both a small and large signal component that must be separately specified. Sometimes the large signal bandwidth is not directly specified but can be determined from the input slew rate. The input capacitance of flash converters can be high; therefore it is necessary to drive the encoder from a low impedance source to achieve high bandwidth.

Another phenomenon that limits the high frequency performance of a flash converter is aperture time. Aperture time is defined as the effective point where the comparator makes its decision. It should be noted that the aperture time is actually the difference between the delay in the path that is processing the compared signal and the delay in the path that processes the strobe. This can become a serious source of distortion if the aperture delay of each comparator within the

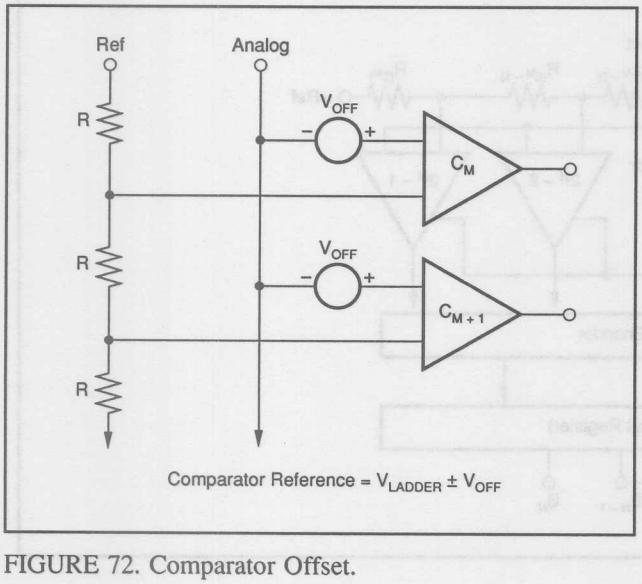


FIGURE 72. Comparator Offset.

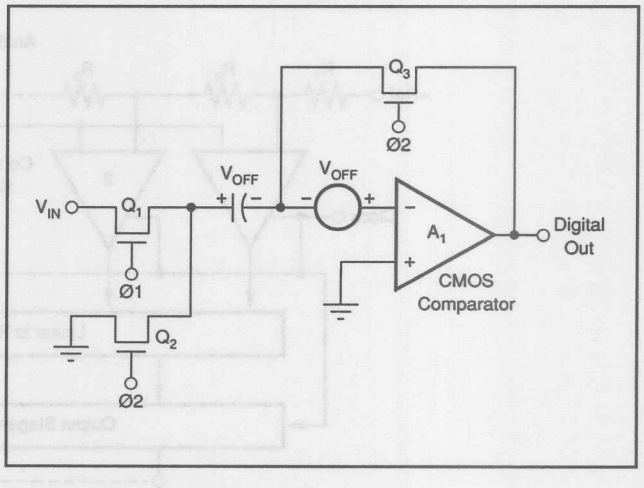


FIGURE 73. Auto Zero Comparator.

flash converter is different. As an example of this effect, consider how closely the aperture delay of an 8-bit, 200MHz flash converter needs to be matched to digitize a signal at the Nyquist rate while making only a 1LSB error.Aperture error is given by:

$$T_A = E_n/(D_{Fs}/D_T)$$

Where:
T_A = aperture time
E_n = allowable noise = 1LSB
Fs = signal frequency
D_{Fs}/D_T = max signal rate of change = $(2^N)(LSB)(7)(Fs)$

Substituting:

$T_A = LSB/(2^N)(LSB)(\pi)(Fs) = 1/(256)(\pi)(100E6) = 12.5ps$

If the effective analog bandwidth of each comparator were 1GHz, the propagation delay of each comparator stage would be in the 100ps to 200ps range. It would then be necessary to match the delay of each comparator to 12.5ps to preserve the accuracy. Since flash converters can easily be 250mils in length and the signal could take as long as 400ps to propagate the length of the chip. The physical layout of the chip is extremely important to achieve acceptable high speed performance.

The high frequency performance of most analog to digital converters can be improved by conditioning the input signal by a sample and hold. This happens as the aperture distortion occurs due to the time delay of the individual comparators within the flash encoder not being matched. Since the sample and hold utilizes a single switch, the aperture performance of the combined system will be improved. One of the methods that can be used to determine the existence of aperture induced distortion is to measure the spectral response of the ADC by performing an FFT. This should first be performed at a low frequency to eliminate static accuracy as the source of the distortion. Aperture induced distortion will then be noted as the component of the distortion that increases with frequency. Even when a sample and hold is not required, interfacing an analog signal to a flash encoder deserves serious consideration. Both the input capacitance and resistance vary with signal level so it is important to drive these types of high speed converters with a low impedance source that can be supplied either from an op amp or from a buffer. This solution is not without its difficulties as high speed op amps are prone to oscillating when required to drive large capacitive loads characteristic of flash encoders. Usually, high speed op amps and buffers are capable of driving low resistive loads so it is possible to decouple the capacitive load from the driving source by placing a small resistor between the two. The resistor has the effect of making the impedance seen by the buffer look resistive thereby preventing an oscillatory condition. Setting the value of the resistor between 10Ω to 50Ω has minimal effect on the system bandwidth. Reference to the beginning of this study will show numerous buffers and amplifiers that could be suitable for interfacing to a flash encoder. Refer to Figure 74 which shows how the coupling resistor helps stabilize the driving source.

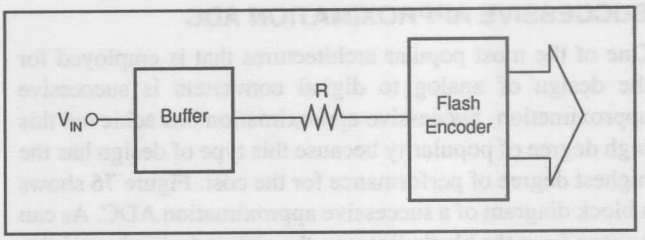


FIGURE 74. Buffer Driving Flash Encoder.

It is straightforward to increase the resolution of a flash encoder by stacking two together as shown in Figure 75. It should be noted that two encoders stacked together in this manner will have poor aperture performance as matching the aperture delays of two separate encoders is difficult. This can be connected by driving the stacked flash encoders by a sample and hold.

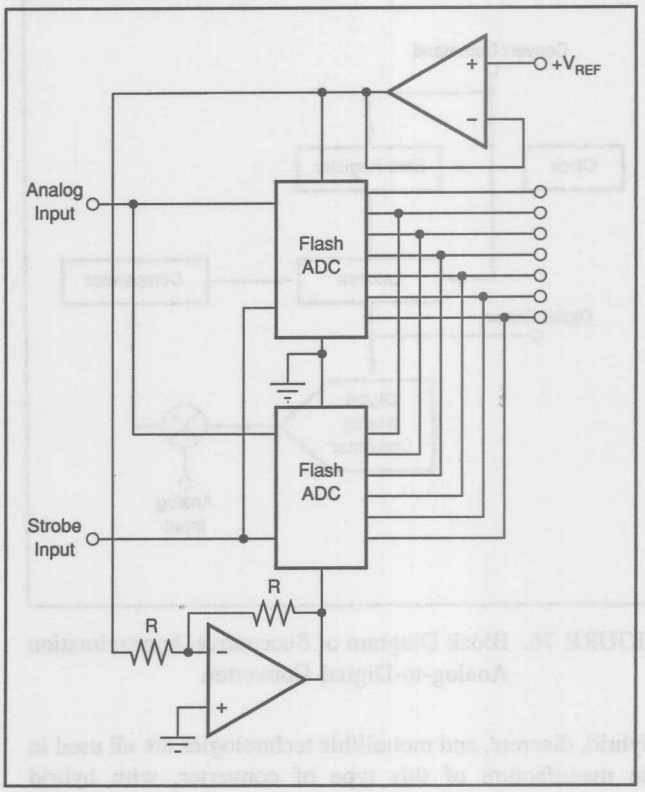


FIGURE 75. Stacked Flash Encoder.

As previously mentioned, the resolution of flash converters is generally not greater than 8 bits. If the resolution of the converter were to increase by 1 bit, the amount of additional circuitry would have to double. Therefore, a 10-bit converter operating at the same speed as an 8-bit one would be four times as large and dissipate four times as much power. A conflict now develops when the designer attempts to use smaller geometry devices to reduce the size of the chip. With the use of smaller devices comes less accuracy which then compromises the possibility of achieving a 10-bit flash converter design. Similarly, the speed tends to be reduced to avoid excessive power dissipation on the chip.

the design of analog to digital converters is successive approximation. Successive approximation has achieved this high degree of popularity because this type of design has the highest degree of performance for the cost. Figure 76 shows a block diagram of a successive approximation ADC. As can be seen from the block diagram, the circuit design is straightforward, employing only a single comparator along with a digital to analog converter and the successive approximation logic. The previously mentioned comparators and digital to analog converter would serve as suitable subassemblies for a successive approximation ADC. Performance varies widely for designs employing this type of architecture, ranging from 8 to 16 bits of resolution with conversion rates from 400ns to 25µs.

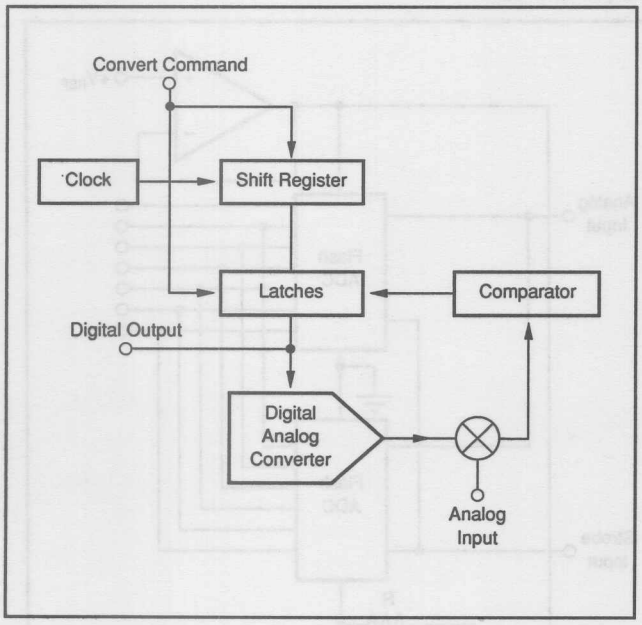


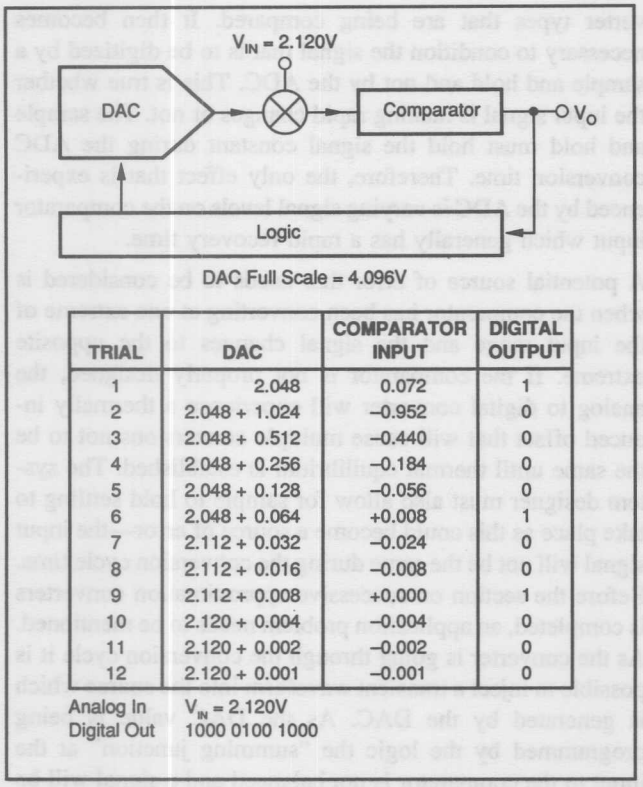
FIGURE 76. Block Diagram of Successive Approximation Analog-to-Digital Converter.

Hybrid, discrete, and monolithic technologies are all used in the manufacture of this type of converter, with hybrid designs dominating the high performance sectors. Recently monolithic designs have been introduced that were formerly the exclusive province of converters designed with hybrid technology. Performance levels with 12 bits of resolution at conversion times of 3µs can now be achieved in monolithic form with speeds down to 1µs on the "drawing board." These single chip 12-bit ADCs employ bipolar, CMOS, and BiMOS for their design. Through BiMOS it is possible to use the most desirable features of CMOS and bipolar technologies. BiMOS processing offers both technologies on the same process. CMOS is optimum for achieving high speed logic with very little power dissipation, and bipolar technology is better suited for low noise and high speed which is required by the analog section of the ADC.

for either monolithic converters or for supplying the logic function in hybrid designs. This is a very important development as CMOS offers lower power dissipation and current drain than bipolar logic. Both of these features are important to a system user as lower power dissipation leads to a lower temperature rise, greater reliability, and fewer problems with warm-up and temperature drift. Reduced current drain will enhance system accuracy as noise due to common analog and digital current paths will be reduced. At the present time successive approximation designs are dominated by the conventional R-2R ladder approach used by the digital to analog converter that lies within the ADC. Just over the horizon, several manufacturers have designs based upon charge distribution techniques employing CMOS. These newer CMOS designs also hold the potential of error correction and self-calibration that will enable converters to achieve greater stability with time than can be achieved with bipolar converters. This arises from the fact that higher circuit density can be achieved with CMOS which is required to implement the error correction function.

The successive approximation process begins with a start conversion pulse, setting the most significant bit to the "on" state with the remaining least significant bits in the "off" state. The output of the digital to analog converter is sent to one of the inputs of the comparator. The other input to the comparator is the analog signal that is to be digitized. After allowing an adequate amount of time for the digital to analog converter to settle, the output of the comparator is read into a latch where the decision is made whether to keep the bit on or not. If the input signal exceeds the weight of the MSB, the decision is made to keep the bit on. During the next trial period, Bit 2 is turned on and added to the result of the initial MSB comparison. In the event that the signal was greater than the MSB but not as great as the sum of the MSB and Bit 2, the MSB would be left on with Bit 2 being left off. This process of adding one more bit and testing the state of the comparator continues until all the bits of the digital to analog converter have been exercised. Figure 77 illustrates this process. Figure 78 shows a timing diagram of the successive approximation conversion cycle. One manufacturer adds digital correction to the conventional successive approximation algorithm. The first eight bits are converted only to 8-bit accuracy when the converter goes into a tracking mode to correct the conversion to 12-bit accuracy. This correction capability allows the first eight bits to operate at a higher sampling rate compared to conventional successive approximation.

Successive approximation has achieved wide popularity due to the simplicity of the design. The linearity of the ADC only depends on linearity of the digital to analog converter which is typically not true of the other ADC architectures being compared. The offset of the comparator creates an overall offset but not a linearity error as would be created in a flash converter. The state of the art in producing accurate digital



TRIAL	DAC	COMPARATOR INPUT	DIGITAL OUTPUT
1	2.048	0.072	1
2	2.048 + 1.024	–0.952	0
3	2.048 + 0.512	–0.440	0
4	2.048 + 0.256	–0.184	0
5	2.048 + 0.128	–0.056	0
6	2.048 + 0.064	+0.008	1
7	2.112 + 0.032	–0.024	0
8	2.112 + 0.016	–0.008	0
9	2.112 + 0.008	+0.000	1
10	2.120 + 0.004	–0.004	0
11	2.120 + 0.002	–0.002	0
12	2.120 + 0.001	–0.001	0

Analog In V_{IN} = 2.120V
Digital Out 1000 0100 1000

FIGURE 77. Successive Approximation Process.

to analog converters is highly developed, which directly benefits successive approximation converters. ADCs employing these DACs will have correspondingly wide temperature ranges. Typically, successive approximation ADCs will operate over a wider temperature range, compared to other techniques, and designs are even available that operate at 200°C. Sub-ranging analog to digital converters have additional sources of error that distort the linearity, as will be explained later. Since there is only a single comparator, more power can be applied to the DAC and comparator to reduce the overall conversion time. Additionally, a successive approximation converter will naturally produce a serial form of the converted output. The serial output feature is very useful for economical digital transmission. Also, it lends itself for optical isolation techniques which helps reduce the interaction between the analog and digital sections of the processing system. With this design, only the DAC has to settle to the final accuracy. This is not true of the sub-ranging arrangement as will be explained later. Assuming that the conversion rate could be achieved, successive approximation would be the architecture of choice as a higher level or performance can be obtained at a given selling price for a particular conversion rate. Another attractive feature of successive approximation is that speed can be traded off against accuracy. Accuracy will degrade gradually due to the DAC not settling and the additional overdrive

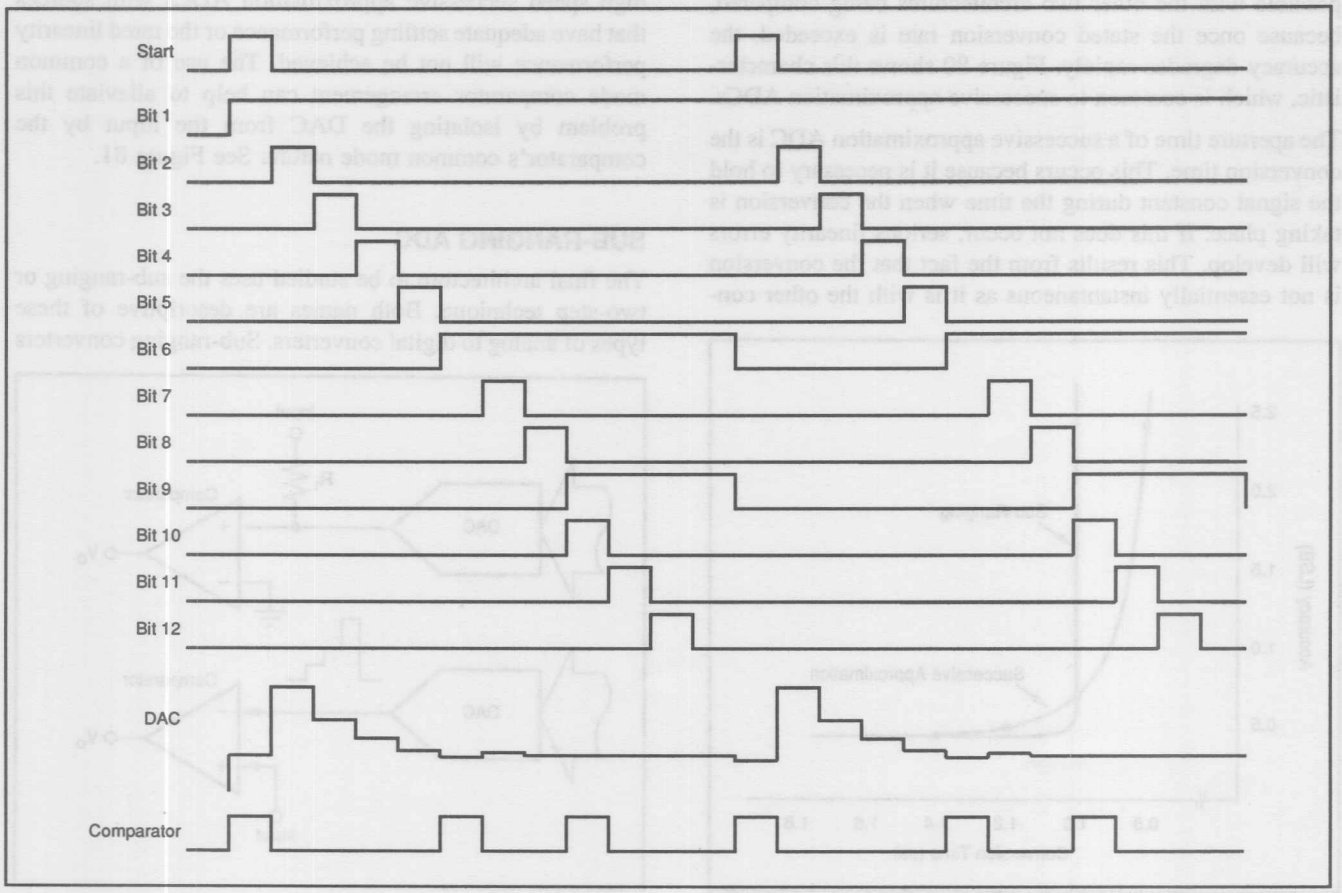


FIGURE 78. Timing Diagram of a Successive Approximation Converter.

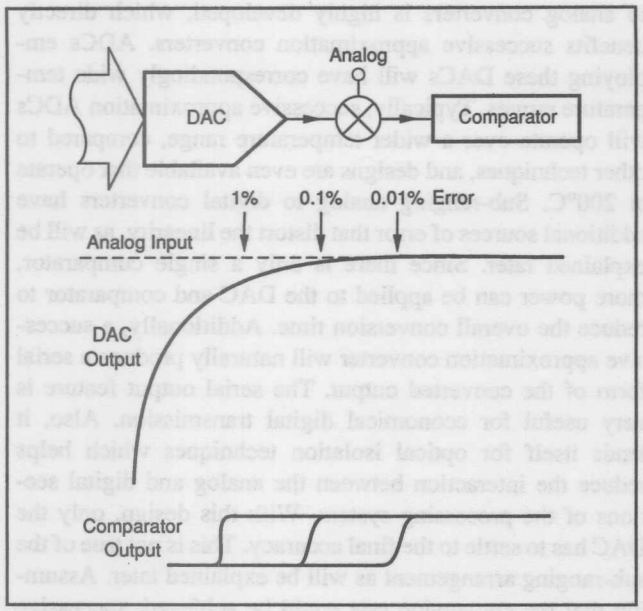


FIGURE 79. Speed vs Accuracy.

needed to switch the comparator more rapidly (see Figure 79). This tradeoff happens gradually, and very often a designer can increase the throughput rate of the system with only a moderate decrease in accuracy. This tradeoff is not possible with the other two architectures being compared, because once the stated conversion rate is exceeded, the accuracy degrades rapidly. Figure 80 shows this characteristic, which is common to successive approximation ADCs.

The aperture time of a successive approximation ADC is the conversion time. This occurs because it is necessary to hold the signal constant during the time when the conversion is taking place. If this does not occur, serious linearity errors will develop. This results from the fact that the conversion is not essentially instantaneous as it is with the other converter types that are being compared. It then becomes necessary to condition the signal that is to be digitized by a sample and hold and not by the ADC. This is true whether the input signal is making rapid changes or not. The sample and hold must hold the signal constant during the ADC conversion time. Therefore, the only effect that is experienced by the ADC is varying signal levels on the comparator input which generally has a rapid recovery time.

A potential source of error that needs to be considered is when the comparator has been converting at one extreme of the input range and the signal changes to the opposite extreme. If the comparator is not properly designed, the analog to digital converter will experience a thermally induced offset that will cause multiple conversions not to be the same until thermal equilibrium is established. The system designer must also allow for sample to hold settling to take place as this could become a source of error—the input signal will not be the same during the conversion cycle time. Before the section on successive approximation converters is completed, an application problem needs to be mentioned. As the converter is going through the conversion cycle it is possible to inject a transient waveform into the source which is generated by the DAC. As the DAC value is being programmed by the logic the "summing junction" at the input to the comparator is not balanced and a signal will be injected into the sources. It is therefore important to drive high speed successive approximation ADCs with sources that have adequate settling performance or the rated linearity performance will not be achieved. The use of a common mode comparator arrangement can help to alleviate this problem by isolating the DAC from the input by the comparator's common mode nature. See Figure 81.

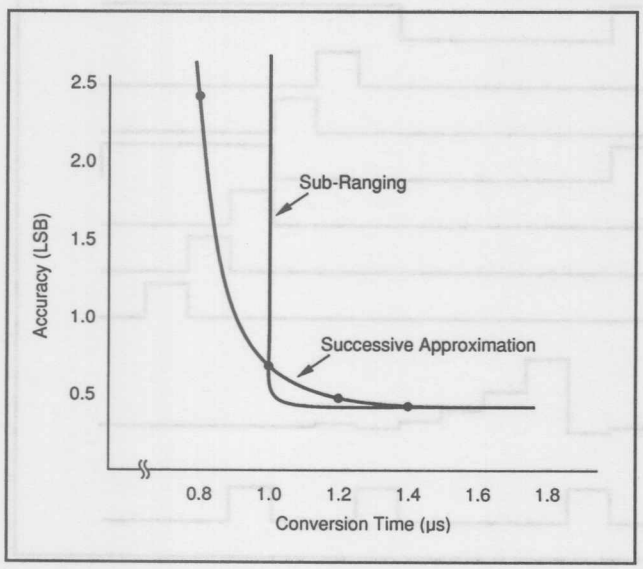


FIGURE 80. Speed vs Accuracy.

SUB-RANGING ADC

The final architecture to be studied uses the sub-ranging or two-step technique. Both names are descriptive of these types of analog to digital converters. Sub-ranging converters

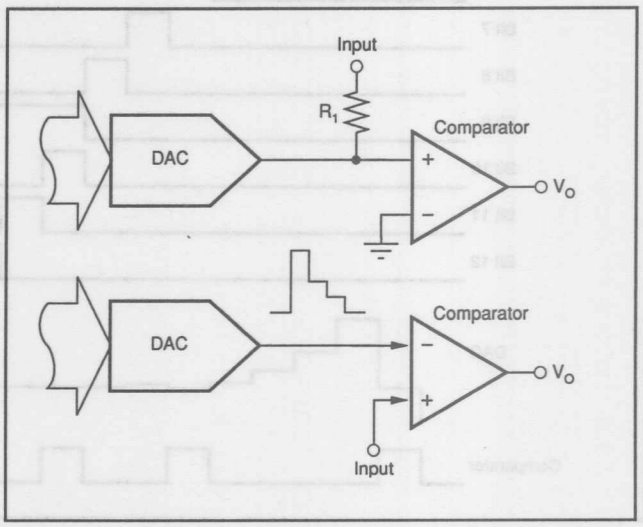


FIGURE 81. SAR ADC Input.

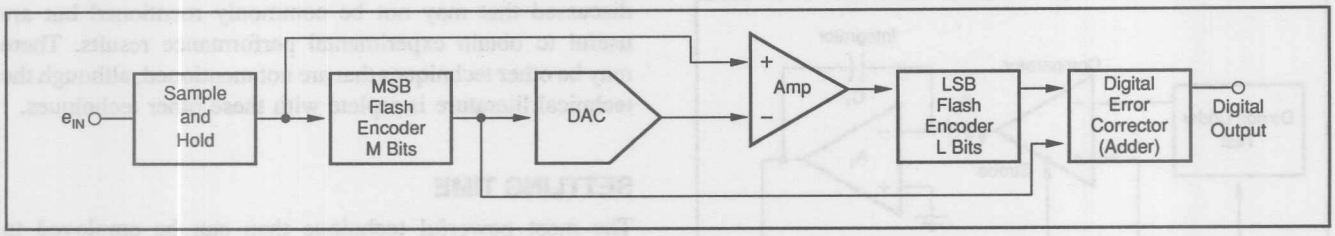


FIGURE 82. Block Diagram of Sub-Ranging ADC.

are considered by designers when high resolution is required for conversion rates that are faster than can be achieved with successive approximation. As an example, a two-step design becomes the approach of choice when the system engineer requires 12 bits of resolution at conversion rates lower than 1µs. This transition point between successive approximation and sub-ranging changes somewhat when lower resolution is required. Ten-bit performance can be achieved at conversion rates lower than 0.5µs using successive approximation.

Sub-ranging combines the elements of the two previously mentioned design techniques. All technologies are employed to produce sub-ranging designs varying from monolithic to modular. Flash converters only require one conversion cycle although 2^N comparators are necessary. Successive approximation uses only one comparator but N conversion cycles are needed. Sub-ranging is a mixture of the two, as an N-bit converter would use two cycles of an N/2-bit flash converter. As an example, a 10-bit flash encoder would use 1023 comparators while a successive approximation type would use one comparator and a sub-ranging design would use 62 comparators. It should be noted that the sub-ranging ADC to be discussed uses only two ranges or conversion cycles. In general, more steps can be used and often find their way into higher resolution converters. The principle of operation is similar and for purposes of simplicity only the two-step version will be explained.

Refer to Figure 82 which shows a block diagram of a sub-ranging converter. The analog signal is initially sent to a sample and hold to reduce aperture effects and to optimize AC performance. The output of the sample and hold then goes to an M-bit flash encoder and to a subtracter. After the sample and hold has acquired the signal and the sample to hold transient has decayed, the first encoder is strobed. The first encoder output determines the initial coarse approximation to the input signal. The digital output from the first encoder is sent to a digital to analog converter where it is converted back to analog form. This signal is then subtracted from the output of the sample and hold. The subtracted signal is then amplified before being applied to the second encoder which has L bits of resolution. The second encoder is also strobed with each encoder's output being sent to a digital adder where the final output word is created.

For a sub-ranging design to operate properly, it is necessary for (M + L) > N. These extra bits are used to encode internally developed errors which are capable of being corrected by a simple algorithm. Figure 83 helps to explain the operation of digital correction within a sub-ranging converter. The simplified analysis shown, in Figure 83, shows that the output of the ADC, with error correction, does not contain the error of the MSB encoder. This means that 12-bit accuracy can be achieved even though the MSB converter only has 8-bit accuracy. The output only contains the error of the LSB encoder which is reduced by the gain of the amplifier that precedes it. For simplicity the DAC error has been left off of the diagram shown in Figure 83 but has been shown in Figure 82. The DAC error has been omitted from the analysis because it has been assumed that the DAC is perfectly accurate. High speed DACs can achieve

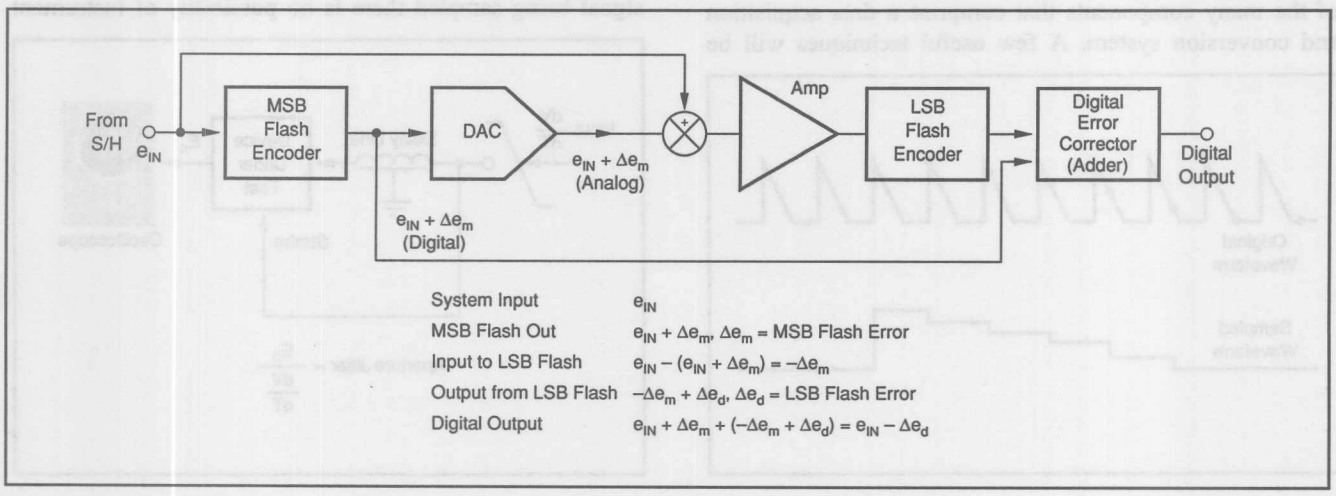


FIGURE 83. Error Correction.

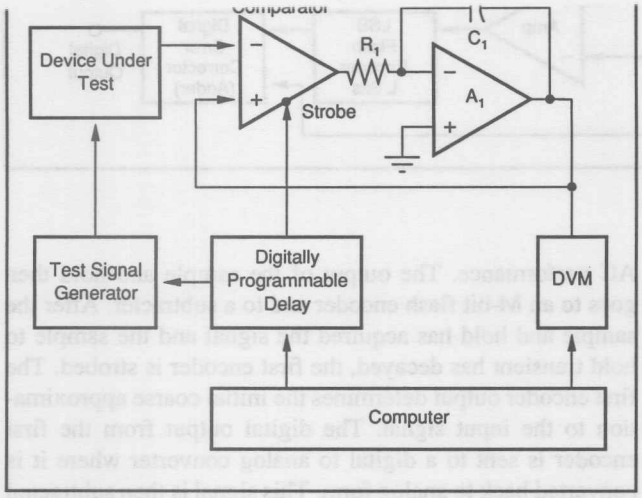


FIGURE 84. Waveform Digitizer.

14-bit accuracy, so this is a reasonable assumption. Another attractive feature of digital correction is that sample to hold settling errors can be corrected and will not lead to linearity errors as they do with successive approximation converters. The sample to hold settling error would be included as part of the MSB error. The M and L bit lines from each of the lower resolution encoders are then combined in the digital adder to form the final output word. To maintain high throughput rate the combining takes place during the next conversion cycle while the next data sample is being taken.

The adder, registers, and timing are grouped together and play the same role as does the successive approximation register of the single comparator design. Sub-ranging converters have achieved 12 bits of resolution with sampling rates to 20MHz.

TEST TECHNIQUES

There are numerous methods for evaluating the performance of the many components that comprise a data acquisition and conversion system. A few useful techniques will be may be other techniques that are not mentioned, although the technical literature is replete with these other techniques.

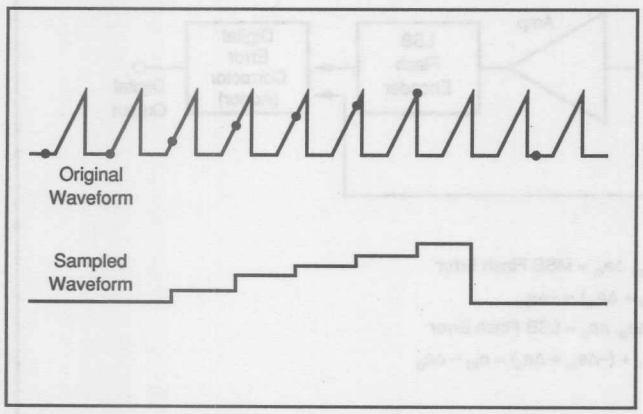


FIGURE 85. Waveform Sampling Process.

SETTLING TIME

The most powerful technique than can be employed to evaluate the settling time of a DAC or an amplifier is to digitize the waveform under test. Once the waveform is digitized, the waveform can be sent to a computer where software routines can be used to determine the performance of the device under test. Digitizing the waveform is superior to hardware-oriented instrumentation because of the versatility associated with a computer. Once the waveform has been digitized, any property of the waveform can be analyzed with the same hardware. Figure 84 is a block diagram of the digitizer. The waveform under test is fed to the inverting comparator input. The comparator's digital output is integrated by the op amp and fed back to the input. Figure 85 is an illustration of the sampling or digitization process. The sampled waveform shown in Figure 85 is a crude representation of the original signal and was done this way for purposes of the illustration. In actual practice, sampling is performed in fine increments to achieve high accuracy. Sampling of the waveform under test is accomplished by repeatedly strobing the comparator at a selected time point, until the integrator feedback forces the comparator reference input to equal the sampled value of the input signal. Once the loop settles, this value is read by the DVM and sent to the computer. The sample is then incremented by the computer through the programmable delay.

APERTURE JITTER

Determining the aperture jitter of an ADC or sample and hold can be accomplished by the block diagram shown in Figure 86. This system avoids introducing any additional error due to instrumentation induced jitter as the added delay is a passive delay line. When the sampling signal is the signal being sampled there is no possibility of instrument

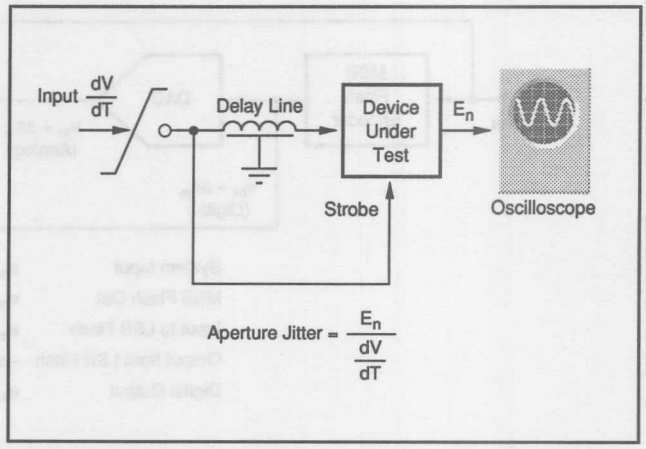


FIGURE 86. Aperture Jitter Measurement.

induced noise affecting the measurement. Once the delay is adjusted so the maximum rate of change section of the signal is being sampled, the aperture jitter T_A is determined by the relationship:

$$T_A = E_n/(dV/dt)$$

Where:
E_n = measured noise
(dV/dT) = input rate of change

BEAT FREQUENCY TESTING

Beat frequency tests are qualitative tests that provide a quick, simple visual demonstration of dynamic ADC performance. Figure 87 shows a block that is used to perform a beat frequency evaluation. An input frequency is selected that provides the worst case change. This usually occurs at the Nyquist rate. The name "beat frequency" describes the nature of the test. The sample frequency is chosen to be a multiple of the input frequency plus a small incremental frequency (see Figure 88). By choosing a low beat frequency, the dynamic performance of the DAC does not affect the accuracy of the measurement. With the block diagram shown, the output of the ADC is resampled at 1/2 the data rate to enable evaluation at the Nyquist rate. The beat frequency is set so that many samples are taken at each code. The beat frequency test should not be used as a substitute for more accurate methods for determining high frequency performance such as FFT measurements or histogram testing, but it provides a very effective method for optimizing the dynamic performance during the development stage of a project. The design engineer will get instant visual feedback, via the oscilloscope, to help pinpoint a circuit defect. This type of cause and effect relationship is not as easy to establish using more complex computer-oriented tests. Burr-Brown, of Tucson, Arizona, offers Application Note AN-133, which describes many other dynamic tests for evaluating ADC performance.

SERVO LOOP TEST

Figure 89 shows the block diagram of a system that can be used to evaluate the DC integral and differential linearity along with the gain and offset of an analog to digital converter. The desired code that is to be measured is loaded into the digital comparator from the computer. Based upon the results of the comparison between the output of the ADC and the desired code, the comparator will command the integrator to slew until a balance is reached. Loop balance

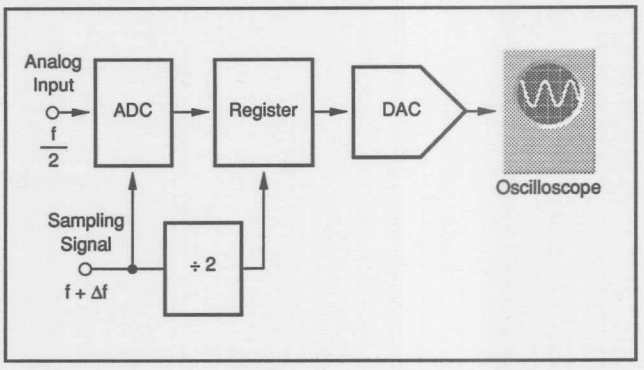


FIGURE 87. Block Diagram of Beat Frequency Testor.

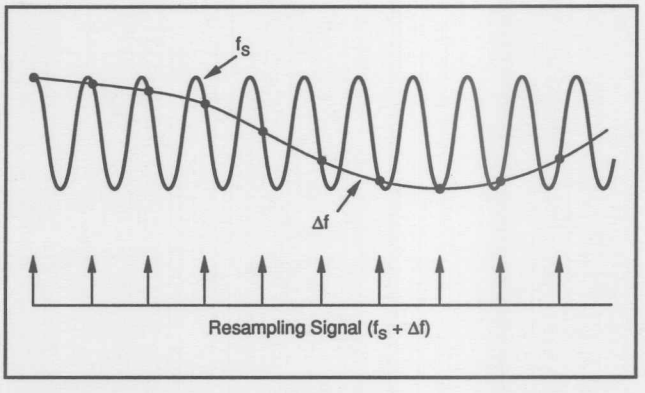


FIGURE 88. Beat Frequency Waveforms.

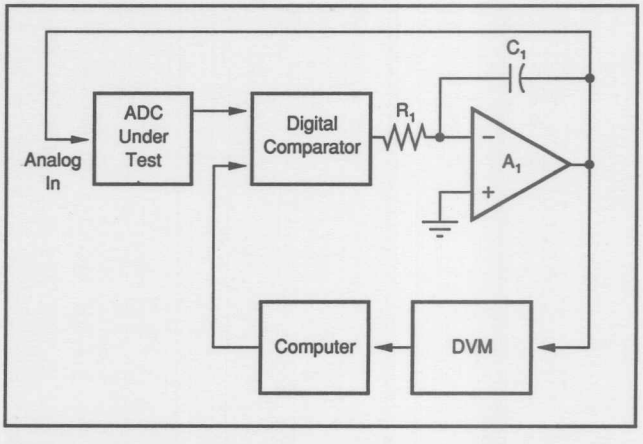


FIGURE 89. Block Diagram of Servo Loop Test.

Analog input
DAC
Pipeline
ADC
Sampling clock
Oscilloscope

Digital Comparator
ADC Under Test
Analog In
DVM
Computer

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HEAT SINKING — TO-3 THERMAL MODEL

Hubert Biagi (602) 746-7422

A critical issue with all semiconductor devices is junction temperature (T_J). T_J must be kept below its maximum rated value, typically 150°C. The lower the junction temperature the better.

The thermal circuit shown below allows temperature to be estimated with simple calculations. The temperature rise across each interface is equal to the total power dissipated in the device times the thermal resistance (PD • θ). An estimate of the junction temperature can be calculated using the following formula:

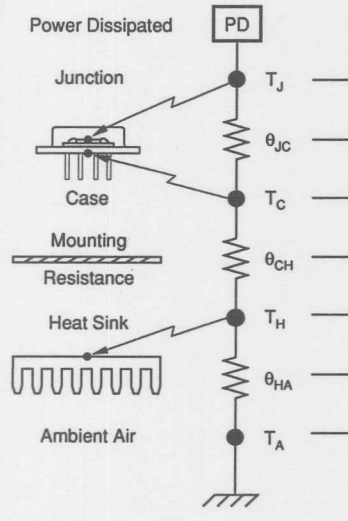
$$T_J = T_A + PD \bullet \theta_{JA}$$

Where,

$$\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA}$$

T_A (°C) = Temperature of Ambient Air
T_J (°C) = Temperature of the Semiconductor Junction
PD (Watts) = Power Dissipated in Semiconductor
θ_{JC} (°C/Watt) = Thermal Resistance (Junction to Case)
θ_{CH} (°C/Watt) = Thermal Resistance (Case to Heat Sink)
θ_{HA} (°C/Watt) = Thermal Resistance (Heat Sink to Air)
θ_{JA} (°C/Watt) = Thermal Resistance (Junction to Air)

The following example shows typical values for a TO-3 package mounted in two different ways — one for high power applications, the other for low power applications. The value for θ_{JC} of 0.8°C/W is for the OPA512 operating under AC signal conditions. For DC signal conditions, θ_{JC} is about 1.4°C/W.



UNITS	HIGH POWER APPLICATION		LOW POWER APPLICATION	
Watts	100W	10W	10W	1W
°C	145°C	37°C *	158°C *	39°C
°C/Watt	0.8	0.8	0.8	0.8
°C	65°C	29°C	150°C	38°C
°C/Watt	0.1	0.1	0.5	0.5
°C	55°C	28°C	145°C	37°C
°C/Watt	0.3	0.3	12	12
°C	25°C	25°C	25°C	25°C

* Note, the difference in junction temperature that thermal resistance can make even when operating at the same power level.

Calculations begin at the bottom of the chart and assume 25°C ambient temperature in these examples. Each component of thermal resistance produces a temperature rise equal to the product of power dissipated and thermal resistance. The temperature of the junction is equal to the product of power dissipated and the total thermal resistance (PD • θ_{JA}).

Thermal resistances can vary significantly with particular models and mounting. While θ values can be obtained from specifications, calculated temperatures should be confirmed by measurements made at the bottom of the case.

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HEAT SINKING — TO-3 THERMAL MODEL

A critical issue with all semiconductor devices is junction temperature (T_J). T_J must be kept below its maximum rated value, typically 150°C. The lower the junction temperature the better.

The thermal circuit shown below allows temperature to be estimated with simple calculations. The temperature rise across each interface is equal to the total power dissipated in the device times the thermal resistance (PD • θ). An estimate of the junction temperature can be calculated using the following formula:

$$T_J = T_A + PD \cdot \theta_{JA}$$

Where,

$$\theta_{JA} = \theta_{JC} + \theta_{CH} + \theta_{HA}$$

T_A (°C) = Temperature of Ambient Air
T_J (°C) = Temperature of the Semiconductor Junction
PD (Watts) = Power Dissipated in Semiconductor
θ_{JC} (°C/Watt) = Thermal Resistance (Junction to Case)
θ_{CH} (°C/Watt) = Thermal Resistance (Case to Heat Sink)
θ_{HA} (°C/Watt) = Thermal Resistance (Heat Sink to Air)
θ_{HA} (°C/Watt) = Thermal Resistance (Junction to Air)

The following example shows typical values for a TO-3 package mounted in two different ways — one for high power applications, the other for low power applications. The value for θ_{JC} of 0.8°C/W is for the OPA512 operating under AC signal conditions. For DC signal conditions, θ_{JC} is about 1.4°C/W.

	HIGH POWER APPLICATION		LOW POWER APPLICATION	
WHEN	120W	10W	10W	1W
T_C	145°C	87°C *	158°C *	30°C
θ_{JC} °C/Watt	0.8	0.8	0.8	0.8
T_S °C	85°C	25°C	150°C	28°C
θ_{CH} °C/Watt	0.1	0.1	0.5	0.5
T_H °C	65°C	25°C	140°C	27°C
θ_{HA} °C/Watt	0.5	0.5	12	12
T_A °C	25°C	25°C	28°C	28°C

* Note, the difference in junction temperature and thermal resistance can make even when operating at the same power level.

Calculations begin at the bottom of the chart and assume 25°C ambient temperature in these examples. Each component of thermal resistance produces a temperature rise equal to the product of power dissipated and thermal resistance. The temperature of the junction is equal to the product of power dissipated and the total thermal resistance (PD • θ_{JA}).

Thermal resistances can vary significantly with particular models and mounting. While θ values can be obtained from specifications, calculated temperatures should be confirmed by measurements made at the bottom of the case.

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MOUNTING CONSIDERATION FOR TO-3 PACKAGES

By Hubert Biagi (602) 746-7422

Proper mounting of TO-3 packages is required to assure rated performance and reliability. Although the procedures are simple, ignoring them can result in poor performance and catastrophic failure of the device.

PACKAGE HANDLING

The TO-3 package is a rugged hermetic package, but it can be damaged with improper handling. Excessive bending or twisting of the package pins can crack the glass seal around the pin and result in loss of hermeticity. If pin straightening is required, clamp the pin against the package base using needle-nose pliers. This will strain-relieve the pin during the straightening operation.

Another potential problem is cracking the internal circuit substrate from bending of the package base. This can be caused by mounting the package onto a non-flat surface, improper use of a compressible thermal pad, or over-tightening the mounting fasteners.

TO-3 SOCKET

The Burr-Brown 0804MC TO-3 socket is designed to meet the requirements of high current, high power products such as the OPA512, OPA541, and OPA2541. The socket has a rugged contact design which assures positive and reliable contact even when using thermal grease and pre-tinned pins. The closed-ended contacts will accept the full pin length of the TO-3 and guard against solder and flux contamination. The socket body has a center hole which allows for direct measurement of TO-3 case temperature.

FASTENERS

The fastener hardware used to mount the TO-3 package is very important. Table I describes the proper hardware combination. Sources for fastener hardware are listed at the end of this bulletin. The preferred fastener material is stainless steel. Plated steel is a good alternative. Brass or plastic fasteners are not recommended.

The mounting holes of the TO-3 package are designed to accept 6-32 machine screws; no other size should be used (see exploded views in Figure 1A and 1B). The pan-head is the best head style. It has a low profile and large bearing face to properly cover the mounting hole, but its not so large as to ride up onto the lip of the welded cover.

In order to maintain proper mounting pressure, the Belleville spring washer (also known as a conical compression washer), is recommended. Split ring and star lock washers are not recommended. They typically bottom out at less than 50 pounds, whereas 150-300 pounds of pressure is needed to

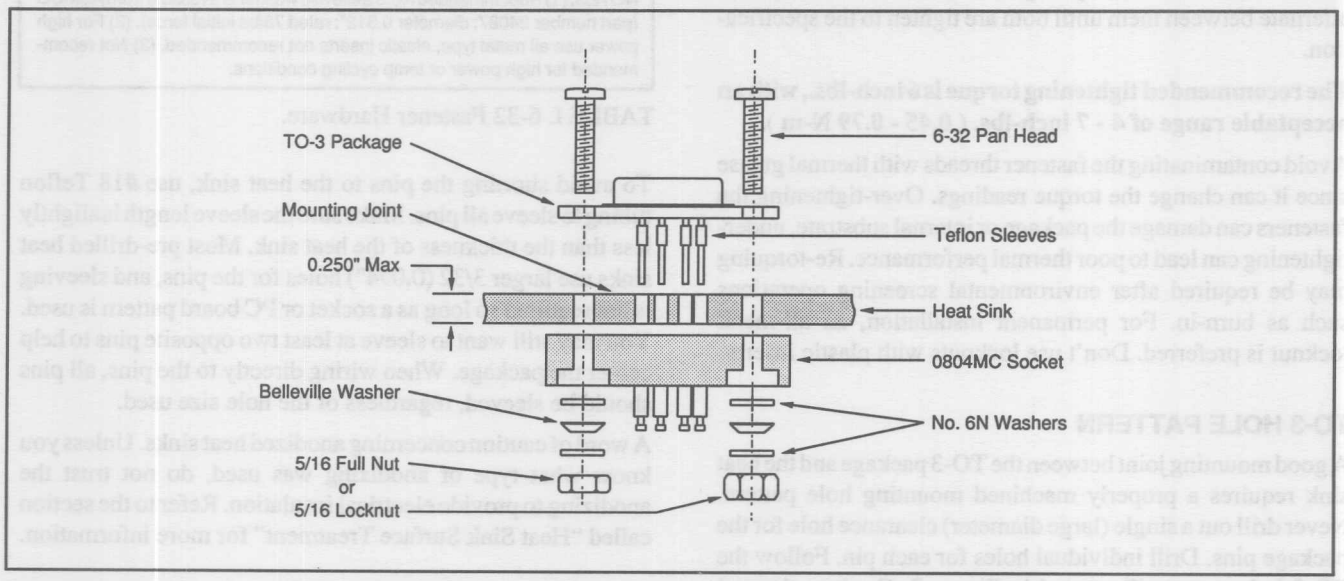

FIGURE 1A. High Power Application Using 0804MC Socket.

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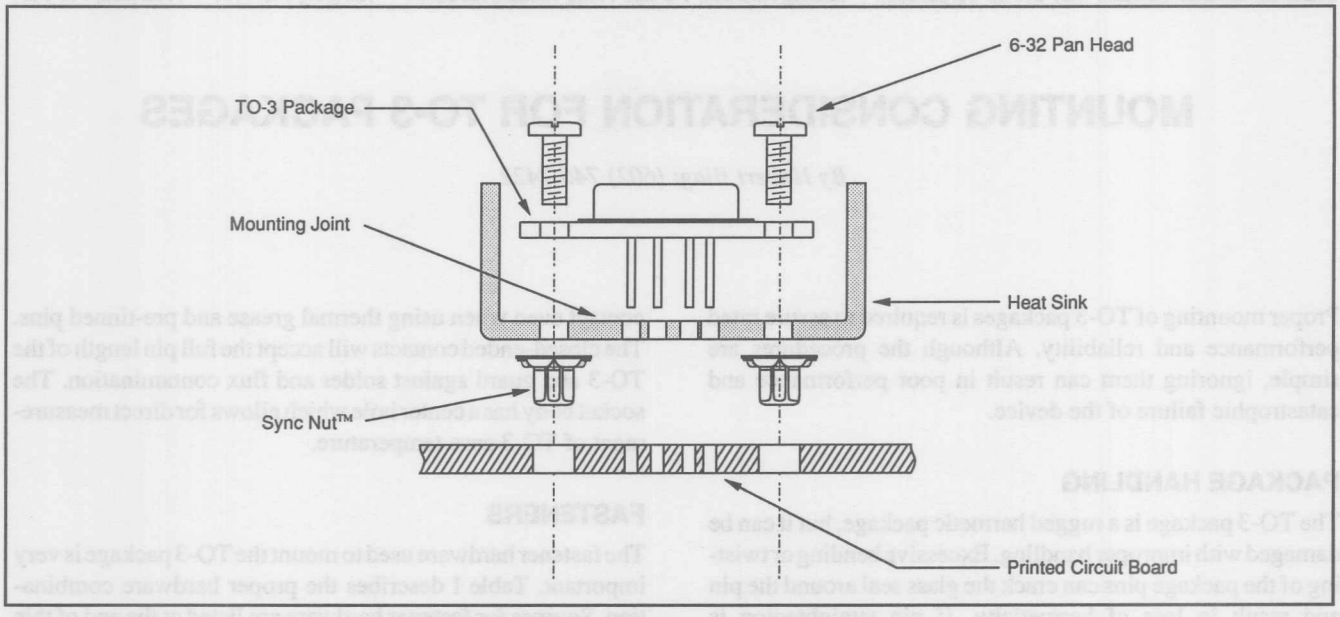


FIGURE 1B. Low Power Application Using Printed Circuit Board.

achieve low thermal resistance[1]. The Belleville washer does not bottom out and therefore can absorb the thermal expansion of the package[2] or any slight compression of the socket material that may occur over time. An excellent variation of the conical washer is called the Sync Nut™ and is available from EG&G Wakefield. It includes a spring washer as part of the nut.

The Belleville washer should be installed on the board or heat sink side of the fastener, *not* on top of the package flange. Install the large face of the Belleville washer toward the mounting surface. When tightening against a board or 0804MC socket, install an additional No.6N (narrow) flat washer against the relatively soft material to insure that the Belleville washer functions correctly. Tighten the fasteners slowly, and alternate between them until both are tighten to the specification.

The recommended tightening torque is 6 inch-lbs., with an acceptable range of 4 - 7 inch-lbs. (0.45 - 0.79 N-m).

Avoid contaminating the fastener threads with thermal grease since it can change the torque readings. Over-tightening the fasteners can damage the package or internal substrate, under-tightening can lead to poor thermal performance. Re-torquing may be required after environmental screening operations such as burn-in. For permanent installation, an all-metal locknut is preferred. Don't use locknuts with plastic inserts.

TO-3 HOLE PATTERN

A good mounting joint between the TO-3 package and the heat sink requires a properly machined mounting hole pattern. Never drill out a single (large diameter) clearance hole for the package pins. Drill individual holes for each pin. Follow the TO-3 hole pattern illustrated in Figure 2. For best thermal performance, use a minimum hole size of 0.073 inch (#49 drill). Smaller holes could interfere with the glass seal around each pin.

	BEST	ACCEPTABLE	NOT RECOMMENDED
Material	Stainless Steel	Plated Steel	Brass, Plastic
Fastener Head	Pan	Round, Hex	Binding, Flat, Oval, Truss, Fillister, Socket, Hex Washer
Washers	No.6 Belleville[1] + No.6N Flat	No.6N Flat	
Nut	5/16" Full, Sync Nut™	1/4" Hex Threaded, 1/4" Full	
Locking Device	5/16" Locknut[2]	Split Ring[3]	Star Washer

NOTES: (1) Recommended No.6 Belleville washer is available from ASMCO (part number 24087; diameter 0.312"; rated 78lbs initial force). (2) For high power use all metal type, elastic inserts not recommended. (3) Not recommended for high power or temp cycling conditions.

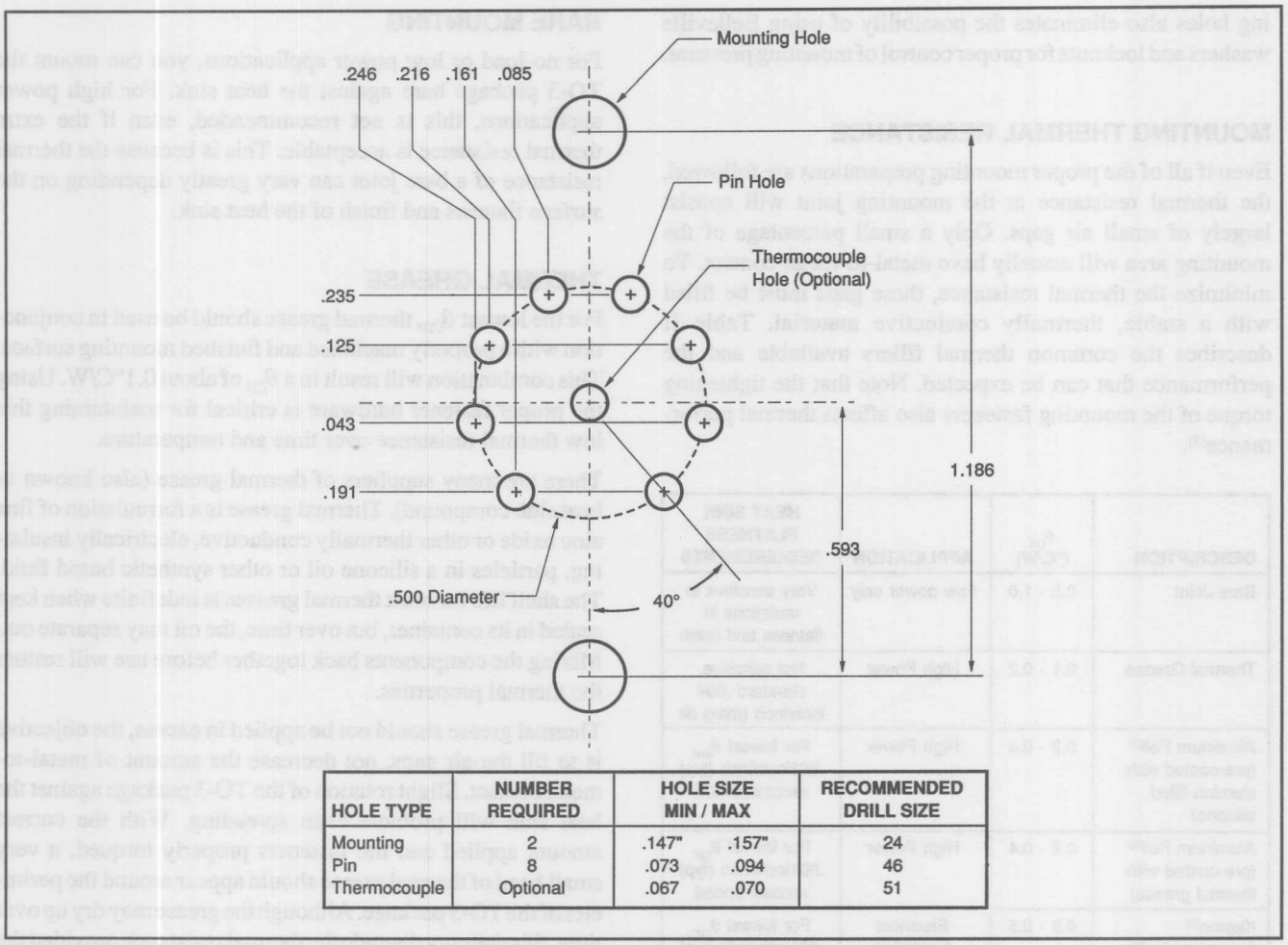
TABLE I. 6-32 Fastener Hardware.

To avoid shorting the pins to the heat sink, use #18 Teflon tubing to sleeve all pins. Make sure the sleeve length is slightly less than the thickness of the heat sink. Most pre-drilled heat sinks use larger 3/32 (0.094") holes for the pins, and sleeving is not required so long as a socket or PC board pattern is used. You may still want to sleeve at least two opposite pins to help center the package. When wiring directly to the pins, all pins should be sleeved, regardless of the hole size used.

A word of caution concerning anodized heat sinks. Unless you know what type of anodizing was used, do not trust the anodizing to provide electrical insulation. Refer to the section called "Heat Sink Surface Treatment" for more information.

MOUNTING SURFACE PREPARATIONS

In general, the heat sink mounting area should have a flatness and finish comparable to that of the TO-3 package. When



HOLE TYPE	NUMBER REQUIRED	HOLE SIZE MIN / MAX		RECOMMENDED DRILL SIZE
Mounting	2	.147"	.157"	24
Pin	8	.073	.094	46
Thermocouple	Optional	.067	.070	51

FIGURE 2. TO-3 Hole Pattern.

using thinner, low power heat sinks, it is sufficient that the mounting area appears flat against a straight edge. When mounting on thicker material, surface flatness is important not only for thermal performance, but to avoid distorting and stressing the package base when it is tightened down.

HEAT SINK SURFACE FLATNESS AND FINISH

JEDEC recommends a surface flatness of 0.004 inch/inch max. The standard flatness tolerance for most extruded heat sinks is 0.004 inch/inch, maximum, which results in typical values closer to 0.002 inch/inch. Surface finish is normally specified around 60 micro-inches (rms). Testing has shown that this is acceptable for most high power applications[3]. It is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse, immediately prior to assembly.

For best thermal performance, the mounting area of the heat sink can be spot faced. This removes oxidation or anodization and improves the surface flatness and finish. When using thermal pads instead of thermal grease, a surface flatness of 0.001 inch/inch is recommended. When mounting the TO-3 package to panels, brackets, or other structural members of the system, spot facing may be required to insure the proper flatness and finish.

HEAT SINK SURFACE TREATMENT

The typical surface treatment for aluminum heat sinks is black anodized[4] per MIL-A-8625, Type II. This surface treatment prevents corrosion and maximizes thermal performance. Do not trust this surface treatment to provide electrical insulation. For electrical insulation, always specify hard anodized, 0.001 inch thick, per MIL-A-8625, Type III. This *file hard* surface treatment resists scratches and punctures, and is typically rated for 200VDC electrical insulation for a 0.001 inch thick treatment.

HEAT SINK THRU-HOLES

Be wary of heat sinks with punched, rather than drilled, thru-holes. If not properly done, the area around each punched hole can be depressed into a crater with a raised lip or mound on the opposite side. This irregular surface can significantly degrade thermal performance.

For high power, extruded heat sinks, the general practice is to drill the hole pattern. All holes should be de-burred. The holes for the TO-3 pins should not be chamfered too deeply, as this will reduce the contact area of the mounting joint. Unless special precautions are taken, threading the TO-3 mounting holes is not recommended. The threading process can also leave a raised mound around each hole. Threading the mount-

MOUNTING THERMAL RESISTANCE

Even if all of the proper mounting preparations are followed, the thermal resistance at the mounting joint will consist largely of small air gaps. Only a small percentage of the mounting area will actually have metal-to-metal contact. To minimize the thermal resistance, these gaps must be filled with a stable, thermally conductive material. Table II describes the common thermal fillers available and the performance that can be expected. Note that the tightening torque of the mounting fasteners also affects thermal performance[5].

DESCRIPTION	θ_{CH} (°C/W)	APPLICATION	HEAT SINK FLATNESS REQUIREMENTS
Bare Joint	0.5 - 1.0	Low power only	Very sensitive to variations in flatness and finish
Thermal Grease	0.1 - 0.2	High Power	Not sensitive, standard .004 inch/inch (max) ok
Aluminum Foil[1] (pre-coated with alumina filled silicone)	0.2 - 0.4	High Power	For lowest θ_{CH}, .001 inch/inch (typ) recommended
Aluminum Foil[2] (pre-coated with thermal grease)	0.2 - 0.4	High Power	For lowest θ_{CH}, .001 inch/inch (typ) recommended
Kapton[3] (pre-coated with thermal grease)	0.3 - 0.5	Electrical Insulation	For lowest θ_{CH}, .001 inch/inch (typ) recommended
Silicon Rubber (compressible)	0.4 - 1.0	Electrical Insulation	See Text
Mica (bare)	1.0 - 1.5	Electrical Insulation	Not recommended Mica is brittle and prone to crack
Mica (with thermal grease)	0.3 - 0.4		

NOTE: (1) Available from BERGQUIST, part number QII-88 (with .094 inch holes). (2) Available from Power Devices, part number AL-155-10C. (3) Available from Crayotherm, part number TO-3-8 CR2-MT. See Appendix for manufacturers listings.

TABLE II. Thermal Interface Options For TO-3 Packages.

Understanding the thermal model of the system will enable you to make the best mounting compromises. Consider the simplified thermal model in Figure 3. The mounting thermal resistance is represented as θ_{CH} (case-to-heat sink). The overall thermal resistance is represented by θ_{JA} (junction-to-ambient). For low power applications, θ_{JA} can be as high 30°C/W. In this case, the mounting thermal resistance is not a significant portion of the overall thermal resistance. For high power applications, θ_{JA} can be as low as 1°C/W. Then it is critical to obtain a low θ_{CH}. For example, at a power dissipation of 50W, an additional 0.5°C/W mounting thermal resistance will increase the junction temperature by 25°C.

TO-3 package bare against the heat sink. For high power applications, this is not recommended, even if the extra thermal resistance is acceptable. This is because the thermal resistance of a bare joint can vary greatly depending on the surface flatness and finish of the heat sink.

THERMAL GREASE

For the lowest θ_{CH}, thermal grease should be used in conjunction with a properly machined and finished mounting surface. This combination will result in a θ_{CH} of about 0.1°C/W. Using the proper fastener hardware is critical for maintaining this low thermal resistance over time and temperature.

There are many suppliers of thermal grease (also known as heat sink compound). Thermal grease is a formulation of fine zinc oxide or other thermally conductive, electrically insulating, particles in a silicone oil or other synthetic based fluid. The shelf life for most thermal greases is indefinite when kept sealed in its container, but over time, the oil may separate out. Mixing the components back together before use will restore the thermal properties.

Thermal grease should not be applied in excess, the objective is to fill the air gaps, not decrease the amount of metal-to-metal contact. Slight rotation of the TO-3 package against the heat sink will promote even spreading. With the correct amount applied and the fasteners properly torqued, a very small bead of thermal grease should appear around the perimeter of the TO-3 package. Although the grease may dry up over time, this does not degrade the thermal resistance provided the mounting joint remains tight.

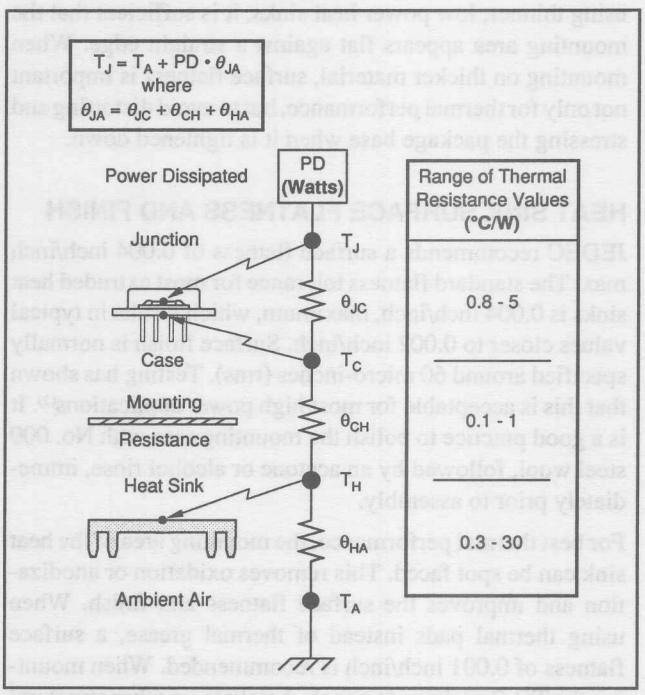


FIGURE 3. Simplified Thermal Model.

THERMAL PADS

Thermally conductive pads offer a cleaner, simpler method for improving the thermal interface. The lowest θ_{CH} attainable using a thermal pad is about 0.2°C/W, which is almost as good as thermal grease. However, one should approach with caution the multitude of different materials, designs, and applications for thermal pads.

Basically there are two types of thermal pads, electrically insulating and electrically conductive. Electrically insulating pads are designed to be used with discrete transistor TO-3s, which do not have an electrically isolated package. In general, they do not provide a low enough θ_{CH} for high power use because a dielectric layer must be sandwiched into the pad. Hybrid TO-3s with isolated headers do not require electrically isolated pads. They can use electrically conductive pads. Without the need for a dielectric layer, a very low θ_{CH} can be achieved, almost as good as thermal grease.

While they do a good job of filling small air gaps, all thermal pads suffer the same problem when used against heat sinks with standard flatness tolerances of 0.004 inch/inch. They do not flow to conform with the surfaces as does thermal grease. Therefore, it is recommended that whenever thermal pads are to be used, the mounting area should be spot faced to a typical surface flatness of 0.001 inch/inch. Silicon rubber pads are also sensitive to surface flatness[6]. Approach these with caution. Most do not improve thermal performance over a bare joint. The compressibility of these rubber pads can cause the package header to flex and possibly crack the internal substrate. They can also settle over time and temperature, resulting in loose fasteners and low mounting pressure.

SUGGESTED MOUNTING SCHEMES

The mounting schemes presented here address the more common operating conditions for TO-3 power products (see Figure 4). These conditions include high power operation, low power operation, and functional testing under unloaded, quiescent conditions. The options are for the 0804MC socket, individual cage jacks, and direct PC board soldering. Table III describes the recommended cage jacks.

MANUFACTURER	PART NUMBER	DRILL SIZE INCHES	(NUM)	COMMENTS
Cambion	450-3716-01-03	.076	48	Knock-out bottom permits wave soldering.
Concord	09-9047-1-03	.104	37	Heavy duty, open ended.
SPC Technology	MC76	.089	43	PC board press fit.
Mil-Max	0325-0-15-01-34-27-10-0	.089	43	Closed end, accepts full pin length.
(See Appendix for manufacturers listings)				

TABLE III. Recommended Cage Jacks.

FUNCTIONAL TESTING AND NO-LOAD CHARACTERIZATION

For functional testing and no-load characterization at room temperature, heat sinking may not be required. These mounting schemes are the least critical and easiest to fabricate. When using the 0804MC socket, the socket can be mounted directly to the test box or PC board by drilling a single clearance hole for all eight socket contacts. The hole should be (0.63 - 0.75) inches in diameter. Be careful not to short the copper cladding or metal box to any of the contacts. The socket body should be mounted using flat head machine screws. For electrical insulation, nylon flat head machine screws may be used instead. When using cage jacks, follow the TO-3 hole pattern illustrated in Figure 2. Use close ended cage jacks whenever possible to avoid solder contamination.

LOW POWER OPERATION

The mounting schemes for low power applications are an extension of those used for functional testing and no-load characterization. The difference is that a small heat sink is must be attached to the TO-3 package. The overall thermal resistance (θ_{JA}) for low power applications can be relatively high, from 5 - 30°C/W. Therefore, θ_{CH} is not as critical as for high power operation. In most instances, the TO-3 package can be mounted bare.

Low power heat sinks are usually stamped rather than extruded, and some even press fit around the TO-3 cover. They are called "low power" or "standard" heat sinks (versus "high power" or "extruded" heat sinks used for high power operation). The thermal resistance of these types of heat sink range from 3 - 20°C/W, depending on their size, weight, and design.

Low power mounting schemes are commonly used on PC board applications. For these applications, heat sink manufacturers have developed many custom accessories such as wave solderable fasteners and thermally conductive pads. These must be approached with caution. It is important to follow the specific recommendations of this bulletin. Thermal pads are discussed in the section called "Thermal Mounting Resistance".

The recommended fastener for PC board applications is the Sync Nut™. This fastener allows the TO-3/heat sink combination to be wave soldered directly to the board. Re-torquing should be performed after any wave solder. For low power applications that do not involve temperature cycling, split ring lock washers may be safely used.

HIGH POWER OPERATION

Mounting schemes for high power operation involve the use of larger, heavier heat sinks, that are machined rather than stamped. Their size and weight usually requires that they be integrated into the system layout, rather than simply attached to the TO-3 package. In general, they are cut to length from extruded sections, thus are often called "extruded" heat sinks.

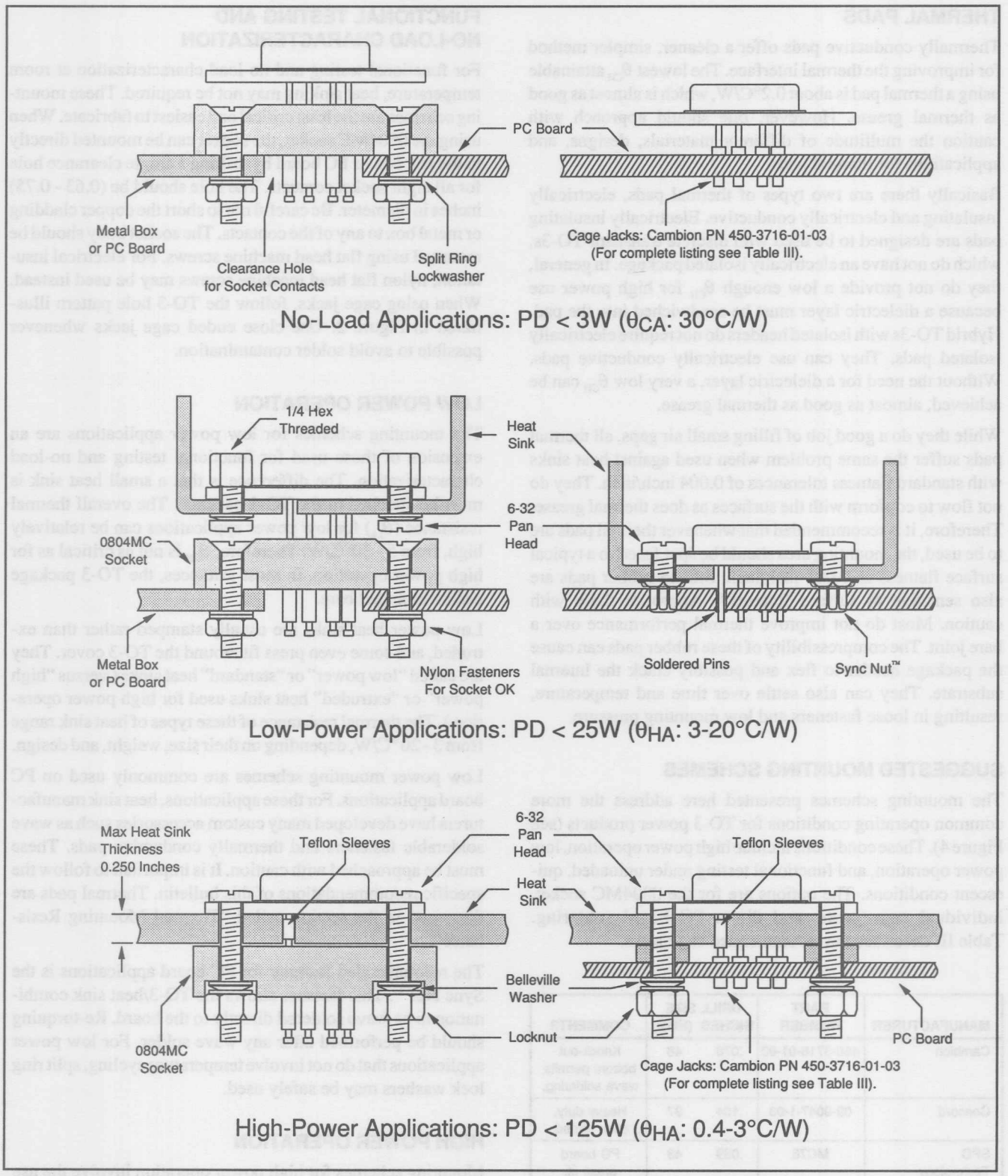


FIGURE 4. TO-3 Mounting Examples.

The thermal resistance of these types of heat sink range from 0.4 - 3°C/W for operation in still air. With forced air, θ_{HA} can be reduced by one-half to two-thirds.

For high power applications, the overall thermal resistance (θ_{JA}) can be as low as 1°C/W. Under these conditions, obtaining a low θ_{CH} is critical. To insure a good mounting joint, use the recommended fastener hardware and surface preparations as described in the previous sections of this application bulletin.

THERMAL MEASUREMENT AND EVALUATION

It is always a good idea to check the TO-3 mounting scheme by measuring the package case temperature (T_C) under actual operating conditions. The semiconductor junction temperature (T_J) can then be calculated from the case temperature, as indicated in Figure 3 :

$$T_J = T_C + PD \bullet \theta_{JC}$$

where PD is the total power dissipation (including quiescent power) and θ_{JC} is the junction-to-case thermal resistance (given in the product data sheet). The calculated junction temperature should be less than the maximum allowable temperature indicated by the product data sheet (typically 150°C).

The true case temperature is located directly below the substrate and centered within the package pins (see Figure 5). This location, called the case backside, will also give the most repeatable measurements. To directly access the case backside, drill the heat sink with the optional thermocouple hole(7) as illustrated in Figure 2. The recommended thermocouple is an Omega fast-response probe (part no. SDX-SET-RT-K-SMP). Allow enough time for the system to reached thermal equilibrium. A touch of thermal grease on the probe tip will ensure good thermal contact.

The package case temperature can also be estimated by fitting a spade-lug type thermocouple under the head of the mounting fastener. This will give the temperature at the mounting flange of the package rather than the case backside. The case backside will actually be hotter than the mounting flange. The difference can be as large as 10°C, depending on the power dissipation, mounting thermal resistance, etc. For high power applications, it is recommended that the case backside temperature be measured directly, at least for the prototype setup.

References:

(1) Thermalloy catalog #90-HS-11 (page 13), Figures 6 and 8.

(2) EG&G Wakefield catalog, printed 4/90 (page 103), "115, 116, 117, & 118 Series SyncNut".

(3) Thermalloy catalog #90-HS-11 (page 12), "Test Results".

(4) Thermalloy catalog #90-HS-11 (page 9), "Available Finishes".

(5) Thermalloy catalog #90-HS-11 (page 13), Figures 6 and 8.

(6) Thermalloy catalog #90-HS-11 (page 106), "Test Method Comparison — TO-3 Silicon Rubber Insulators".

(7) The optional thermocouple hole will not increase the mounting thermal resistance significantly. The difference cannot be measured experimentally. Computer simulations indicate an increase of less than 0.02°C/W.

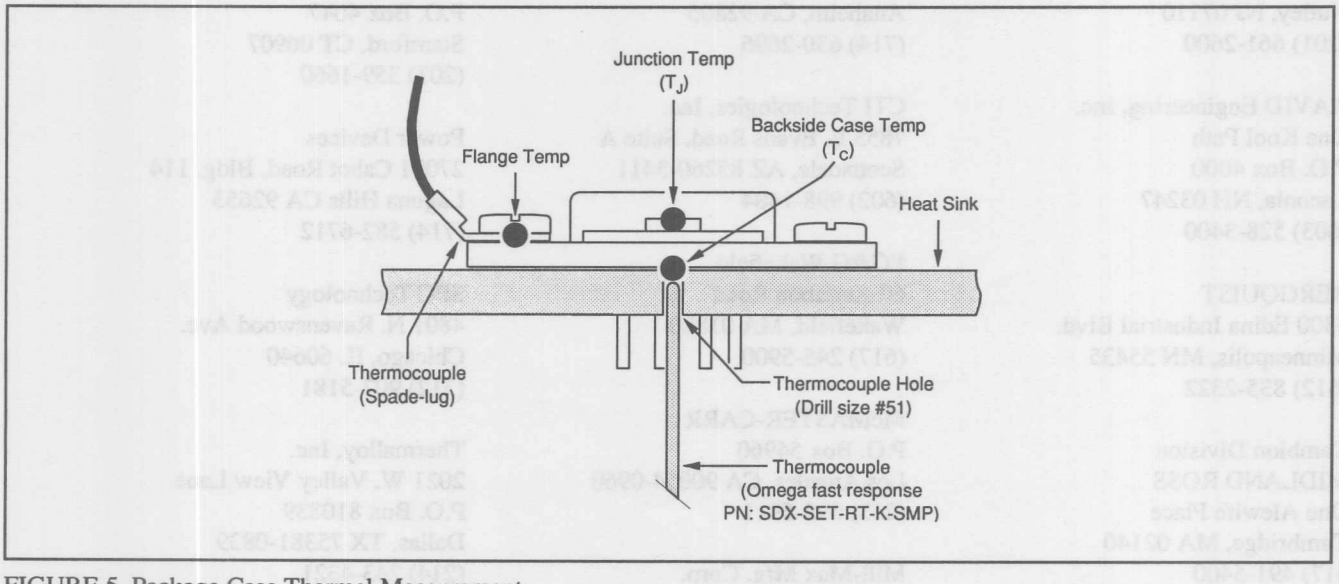


FIGURE 5. Package Case Thermal Measurement.

MANUFACTURER	TO-3 SOCKET	GAGE JACKS	THERMAL GREASE	THERMAL PADS	HEAT SINKS	TEFLON TUBING	FASTENER HARDWARE	TEMP MEAS	ASM TOOLS
BURR-BROWN	0804MC								
CTI	X								
CONCORD		X							
Cambion		X							
Mill-Max		X							
NEWARK		X			X		X		
Thermalloy			X		X				
AAVID Engineering			X		X				
EG&G Wakefield			X		X		X		
BERGQUIST				X					
Power Devices				X					
Crayotherm				X					
Alpha Wire						X			
SPC Technology						X			
McMASTER-CARR							X		X
ASMCO							X		
OMEGA								X	

TABLE IV. Sources of TO-3 Mounting Hardware.

Alpha Wire Corp.
711 Lidgerwood Ave.
Elizabeth, NJ 07207-0711
(908) 925-8000

ASMCO
19 Baltimore St.
Nutley, NJ 07110
(201) 661-2600

AAVID Engineering, Inc.
One Kool Path
P.O. Box 4000
Laconia, NH 03247
(603) 528-3400

BERGQUIST
5300 Edina Industrial Blvd.
Minneapolis, MN 55435
(612) 835-2322

Cambion Division
MIDLAND ROSS
One Alewife Place
Cambridge, MA 02140
617) 491-5400

CONCORD
30 Great Jones St.
New York, NY 10012
(212) 777-6571

Crayotherm Corp.
1185 N. Van Home Way
Anaheim, CA 92806
(714) 630-2696

CTI Technologies, Inc.
7855 E. Evans Road, Suite A
Scottsdale, AZ 85260-3411
(602) 998-1484

EG&G Wakefield
60 Audubon Road
Wakefield, MA 01880
(617) 245-5900

McMASTER-CARR
P.O. Box 54960
Los Angeles, CA 90054-0960
(213) 692-5911

Mill-Max Mfg. Corp.
P.O. Box 300
190 Pine Hollow Road
Oyster Bay, NY 11771-0300
(516) 922-6000

NEWARK Electronics
4801 N. Ravenswood Ave.
Chicago, IL 60640-4496
(312) 784-5100

OMEGA
One Omega Drive
P.O. Box 4047
Stamford, CT 06907
(203) 359-1660

Power Devices
27071 Cabot Road, Bldg. 114
Laguna Hills CA 92653
(714) 582-6712

SPC Technology
4801 N. Ravenswood Ave.
Chicago, IL 60640
(312) 907-5181

Thermalloy, Inc.
2021 W. Valley View Lane
P.O. Box 810839
Dallas, TX 75381-0839
(214) 243-4321

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OPERATIONAL AMPLIFIER AND INSTRUMENTATION AMPLIFIER MACROMODELS

By Hubert Biagi and R. Mark Stitt
Edited by Bonnie Baker

INTRODUCTION

This application bulletin and the accompanying disk is a collection of Spice models for Burr-Brown op amps, difference amps, and IAs. There are three types of models; a standard macromodel, an enhanced macromodel and a simplified circuit model. The standard op amp macromodels were derived using the MicroSim Corporation PSpice® Parts™ Simulation software. An enhanced version of this standard macromodel is also included for all op amps and instrumentation amplifiers. In some instances, a third model, "X", is available. This model is not a macromodel, but rather a simplified circuit model at the transistor level. The simplified circuit models produce more accurate simulations, but because of their complexity, require more simulation time. The instrumentation amplifier macromodels use op amp macromodels and additional components. Table I summarizes how the files on this disk are labeled.

FILE NAME	DESCRIPTION
OPA111.MOD	OPA111 Standard Op Amp Macromodel
OPA111E.MOD	OPA111 Enhanced Op Amp Macromodel
OPA603X.MOD	OPA603 Simplified Circuit Model
INA105.MOD	INA105 Standard Difference Amp Macromodel
INA105E.MOD	INA105 Enhanced Difference Amp Macromodel

TABLE Ia. Examples of Files on Macromodel Disk.

STANDARD OP AMP MACROMODELS

The op amp macromodels were created by running the PSpice® Parts™ Simulation software on an IBM-compatible PC. This software uses the standard Boyle op amp model[1]. The PSpice manual available from MicroSim[2] contains a detailed discussion of each of the elements used in the macromodels.

Op amp macromodels use the node assignments shown in Figures 1 to 3. Table II below summarizes the circuits. Figure 4 shows the external op amp node assignments. Tables III, IV, and V list component prefix designations, macromodel component descriptions, and Spice INPUT designations.

FIGURE	INPUT TRANSISTORS	TYPE OF MACROMODEL
1A	N-Channel JFET	Standard PSpice® Parts™
1B	N-Channel JFET	Enhanced PSpice® Parts™
1C	P-Channel JFET	Standard PSpice® Parts™
1D	P-Channel JFET	Enhanced PSpice® Parts™
2A	NPN Bipolar	Standard PSpice® Parts™
2B	NPN Bipolar	Enhanced PSpice® Parts™
2C	PNP Bipolar	Standard PSpice® Parts™
2D	PNP Bipolar	Enhanced PSpice® Parts™
3A	NPN Bipolar	OPA620/621 Simplified Circuit Model
3B	Bipolar CFB	OPA603 Simplified Circuit Model

TABLE II. Op Amp Macromodel Circuits.

CONTENTS OF MACROMODEL DISK						
OPA27	OPA512	OPA27E	OPA512E	INA101	INA101E	OPA603X
OPA27HT	OPA541	OPA27HE	OPA541E	INA102	INA102E	OPA620X
OPA37	OPA602	OPA37E	OPA602E	INA103	INA103E	OPA621X
OPA77	OPA606	OPA77E	OPA606E	INA105	INA105E	
OPA101	OPA620	OPA101E	OPA620E	INA106	INA106E	
OPA102	OPA621	OPA102E	OPA621E	INA110	INA110E	
OPA111	OPA627	OPA111E	OPA627E	INA117	INA117E	
OPA121	OPA637	OPA121E	OPA637E	INA120	INA120E	
OPA128	OPA1013	OPA128E	OPA1013E			
OPA177	OPA2107	OPA177E	OPA2107E			
OPA404	OPA2111	OPA404E	OPA2111E	UAF42	UAF42E	
OPA445	OPA2541	OPA445E	OPA2541E			
OPA501	OPA2604	OPA501E	OPA2604E			
OPA511		OPA511E				

TABLE Ib. Contents of Macromodel Disk.

1) For more information, see: G.R. Boyle, B.M. Cohn, D.O. Pederson, and J.E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers," *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

2) MicroSim Corporation, 20 Fairbanks, Irvine, CA 92718 USA, (714) 770-3022, (800) 245-3022.

PSpice® Parts™, MicroSim Corp.

Printed in U.S.A. October, 1991

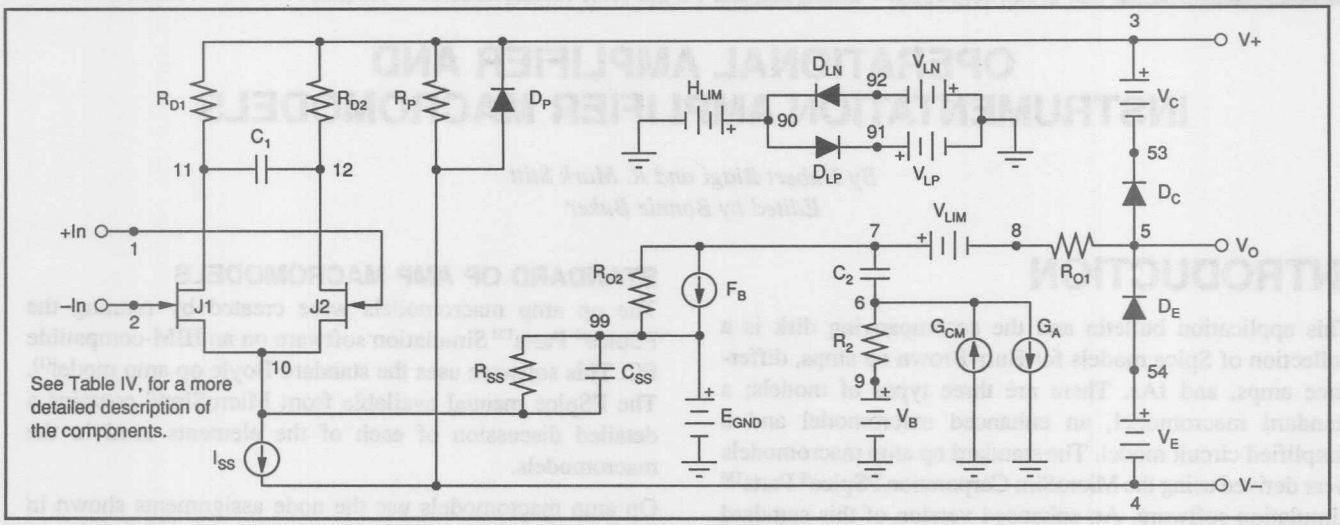


FIGURE 1a. N-Channel JFET-Input Op Amp Standard PSpice® Parts™ Macromodel.

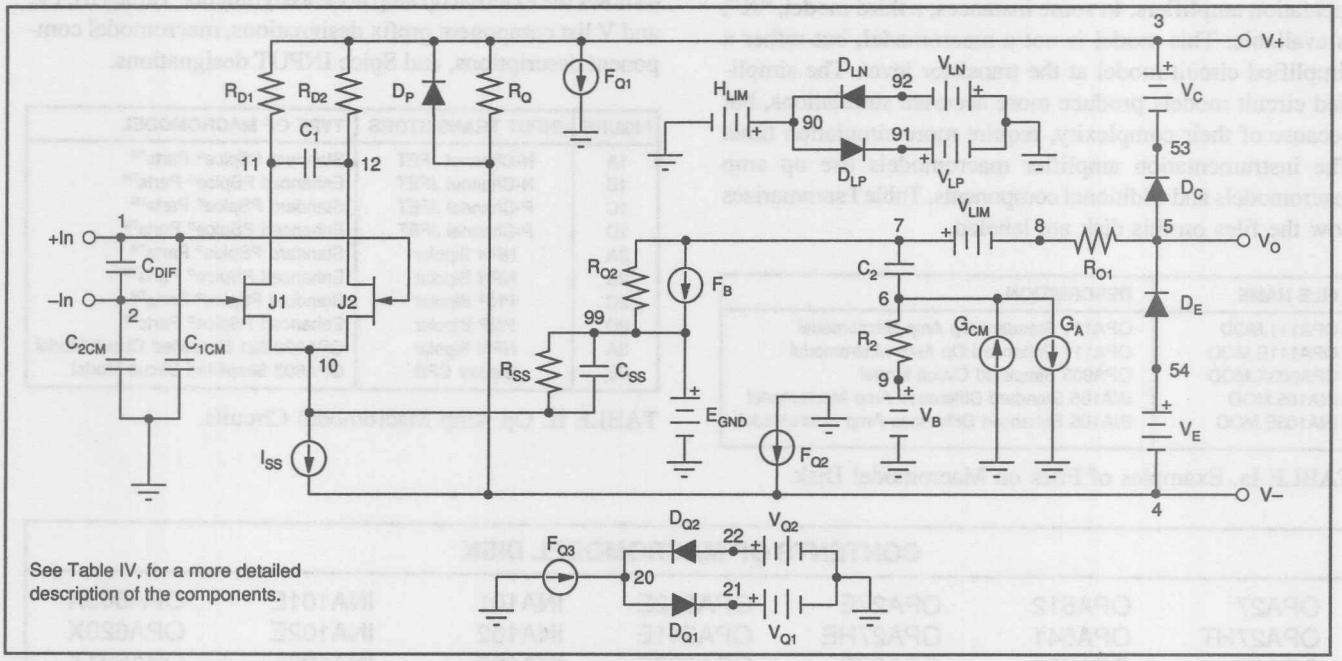


FIGURE 1b. N-channel JFET-Input Op Amp Enhanced PSpice® Parts™ Macromodel.

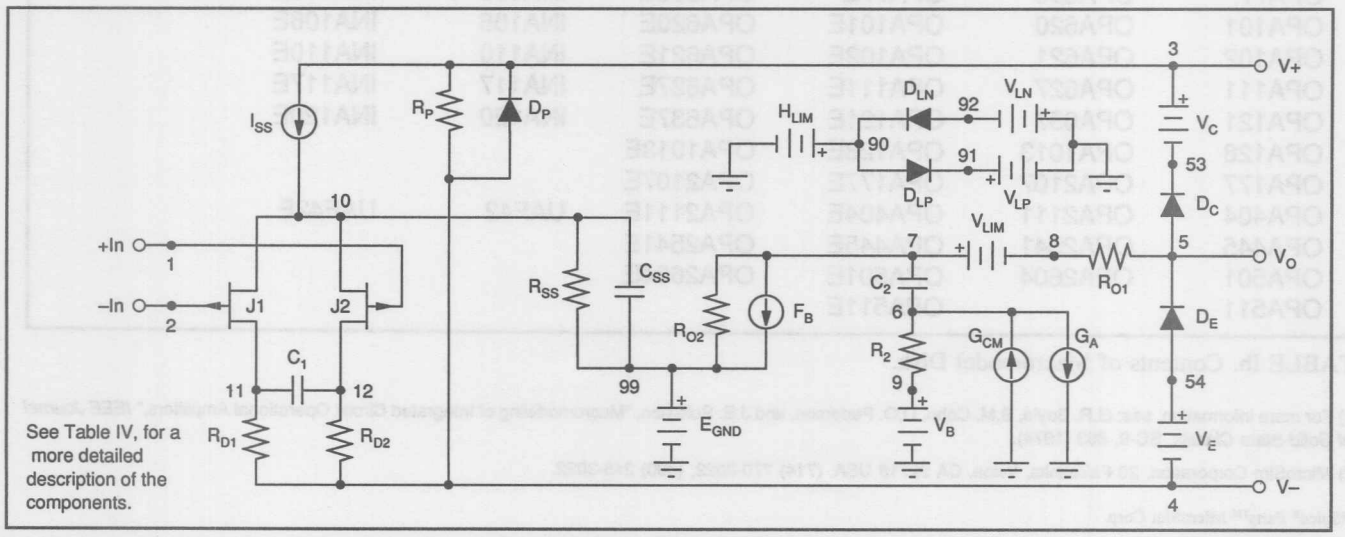


FIGURE 1c. P-channel JFET-Input Op Amp Standard PSpice® Parts™ Macromodel.

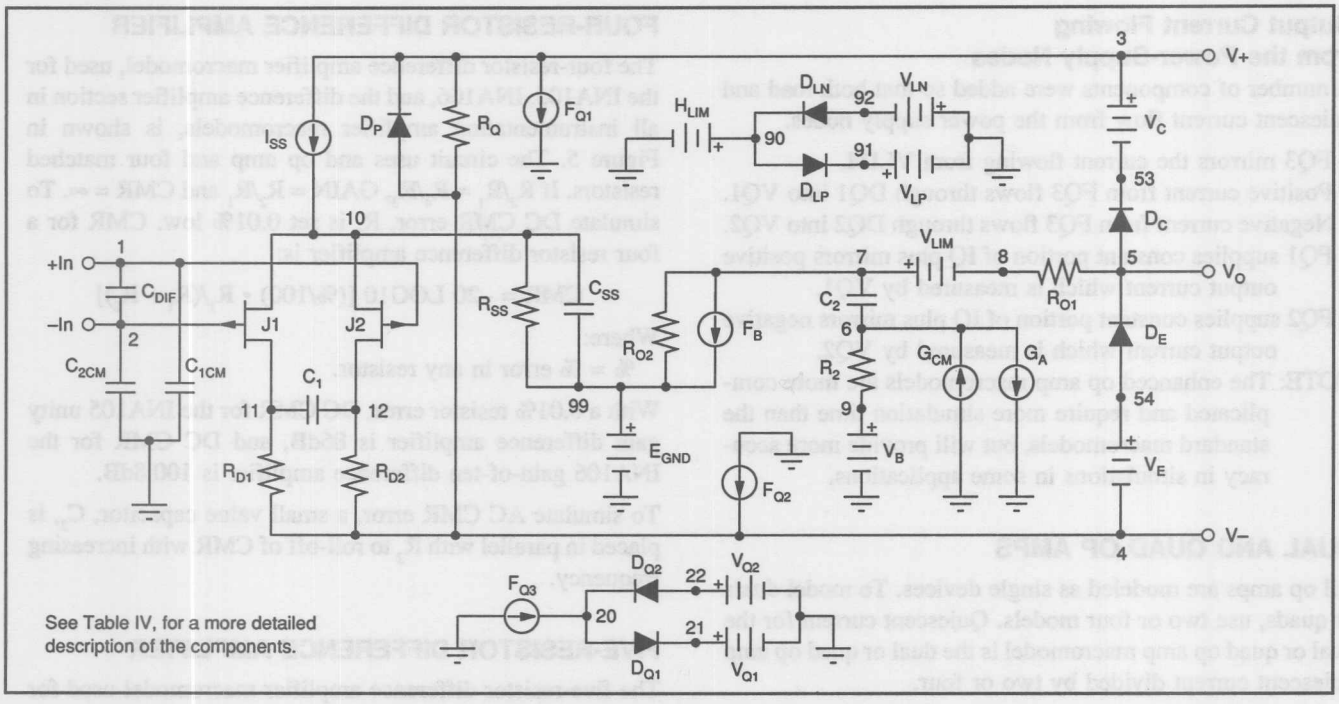


FIGURE 1d. P-channel JFET-Input Op Amp Enhanced PSpice® Parts™ Macromodel.

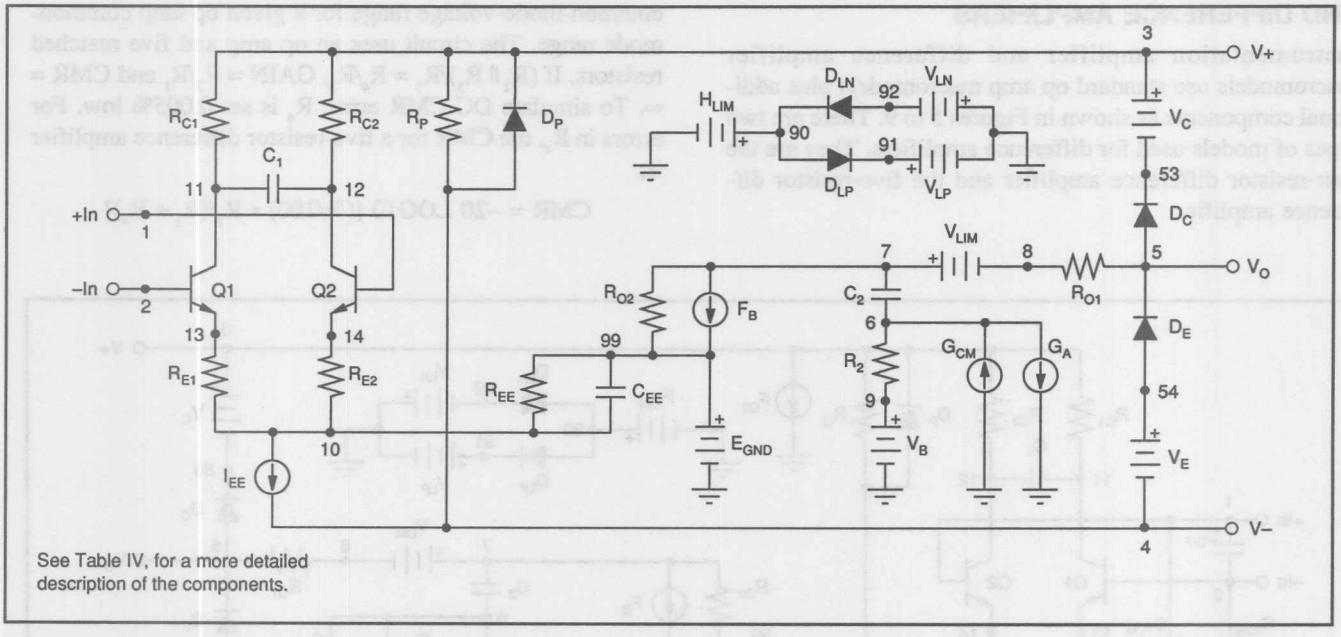


FIGURE 2a. NPN-Input Op Amp Standard PSpice® Parts™ Macromodel.

ENHANCED PSpice® Parts™ MACROMODEL

The enhanced version of the standard PSpice® Parts™ model contains the following additions and changes:

Input capacitance

Differential and common-mode input capacitors, C_{DIF}, C_{1CM}, and C_{2CM} have been added to the standard macromodel. Input capacitance could also be modeled by including capacitor coefficients in the transistor models. Instead, discrete capacitors were used so the comparison to the standard model would be more obvious.

Input protection diodes

If an op amp contains input protection diodes, its enhanced op amp macromodel also contains diodes connected between the input pins as shown in Figures 4C and 4D, for example.

Quiescent power

R_P was replaced by R_Q. The value of R_Q is higher. It models only the resistive portion of quiescent current. The current sources described below model the constant portion of the quiescent current. This technique provides a more accurate model of quiescent current vs power-supply voltage.

from the Power-Supply Nodes

A number of components were added so that both load and quiescent current flow from the power supply nodes.

FQ3 mirrors the current flowing from VLIM.
Positive current from FQ3 flows through DQ1 into VQ1.
Negative current from FQ3 flows through DQ2 into VQ2.
FQ1 supplies constant portion of IQ plus mirrors positive output current which is measured by VQ1.
FQ2 supplies constant portion of IQ plus mirrors negative output current which is measured by VQ2.

NOTE: The enhanced op amp macromodels are more complicated and require more simulation time than the standard macromodels, but will provide more accuracy in simulations in some applications.

DUAL AND QUAD OP AMPS

All op amps are modeled as single devices. To model duals or quads, use two or four models. Quiescent current for the dual or quad op amp macromodel is the dual or quad op amp quiescent current divided by two or four.

INSTRUMENTATION AMPLIFIERS AND DIFFERENCE AMPLIFIERS

Instrumentation amplifier and difference amplifier macromodels use standard op amp macromodels plus additional components as shown in Figures 5 to 9. There are two types of models used for difference amplifiers. They are the four-resistor difference amplifier and the five-resistor difference amplifier.

The four-resistor difference amplifier macromodel, used for the INA105, INA106, and the difference amplifier section in all instrumentation amplifier macromodels, is shown in Figure 5. The circuit uses and op amp and four matched resistors. If $R_2/R_1 = R_4/R_3$, GAIN = R_2/R_1 and CMR = ∞. To simulate DC CMR error, R_2 is set 0.01% low. CMR for a four resistor difference amplifier is:

$$CMR = -20\ LOG10\ [(\%/100) \bullet R_1/(R_1 + R_2)]$$

Where:

% = % error in any resistor.

With a 0.01% resistor error, DC CMR for the INA105 unity gain difference amplifier is 86dB, and DC CMR for the INA106 gain-of-ten difference amplifier is 100.8dB.

To simulate AC CMR error, a small value capacitor, C_2, is placed in parallel with R_2 to roll-off of CMR with increasing frequency.

FIVE-RESISTOR DIFFERENCE AMPLIFIER

The five-resistor difference amplifier macromodel used for the INA117 is shown in Figure 9. The advantage of the five-resistor difference amplifier configuration is a boost in input common-mode-voltage range for a given op amp common-mode range. The circuit uses an op amp and five matched resistors. If $(R_2 \parallel R_5)/R_1 = R_4/R_3$, GAIN = R_2/R_1 and CMR = ∞. To simulate DC CMR error, R_4 is set 0.005% low. For errors in R_4, the CMR for a five-resistor difference amplifier is;

$$CMR = -20\ LOG10\ [(\%/100) \bullet R_1/(R_1 + R_4)]$$

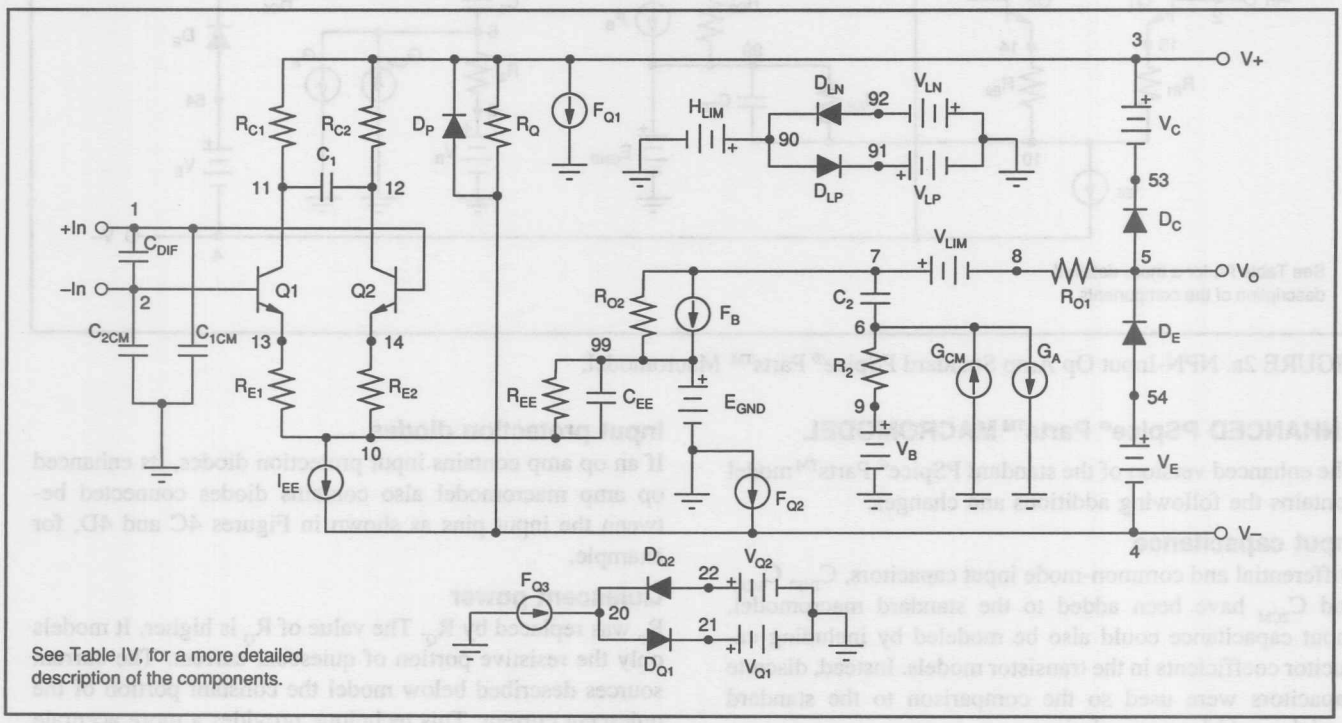


FIGURE 2b. NPN-Input Op Amp Enhanced PSpice® Parts™ Macromodel.

Where:

% = % error in R_4

*$R_2 \| R_5 = R_2 \cdot R_5/(R_2 + R_5)$

With a 0.005% resistor error, DC CMR for the INA117 high common-mode-voltage unity-gain difference amplifier is 86.5dB. Note that unlike the four resistor difference amplifier, the sensitivity of DC CMR to errors in resistor value is different for different resistors.

To simulate AC CMR error, a small value capacitor, C_2, is placed in parallel with R_2 to roll-off of CMR with increasing frequency.

LIMITATIONS

These macromodels are intended to help designers simulate typical amplifier performance. The macromodels were compiled by entering data sheet typical specifications into MicroSim Parts™. Where data sheet specifications were not available, typical measured values or design values were used. Macromodels were verified with several standard simulations such as gain-phase and large and small-signal transient response. In some cases adjustments were made to the Parts™ macromodel inputs or component parameters so simulations with the macromodel more closely agreed with actual measured typical performance.

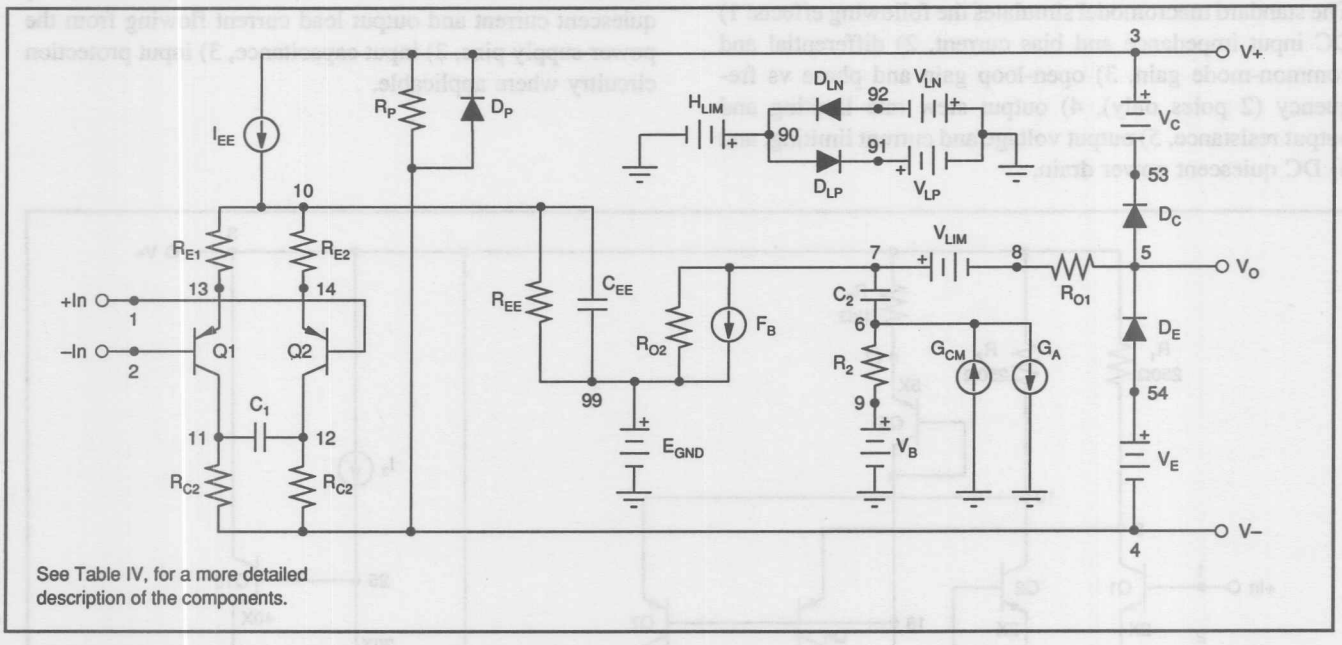


FIGURE 2c. PNP-Input Op Amp Standard PSpice® Parts™ Macromodel.

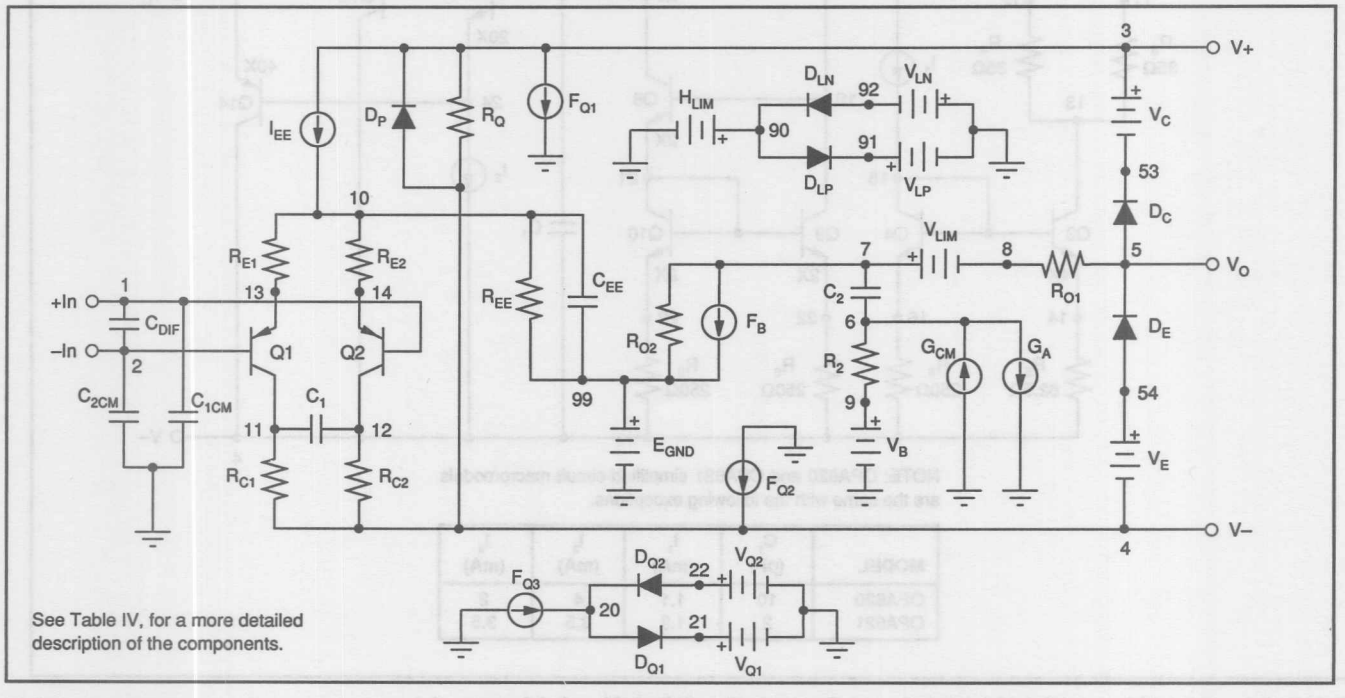


FIGURE 2d. PNP-Input Op Amp Enhanced PSpice® Parts™ Macromodel.

Since these macromodels only simulate the typical performance of certain selected specifications, they will not predict actual device performance under all conditions. Good design practice dictates that, in addition to simulation with macromodels, circuit verification must include; 1) Worst case analysis with data sheet minimum and maximum room temperature specifications, 2) Worst case analysis with variation of specifications over the operating temperature range, 3) thorough breadboard evaluation, and 4) complete prototype characterization.

EFFECTS THE STANDARD MACROMODEL SIMULATES

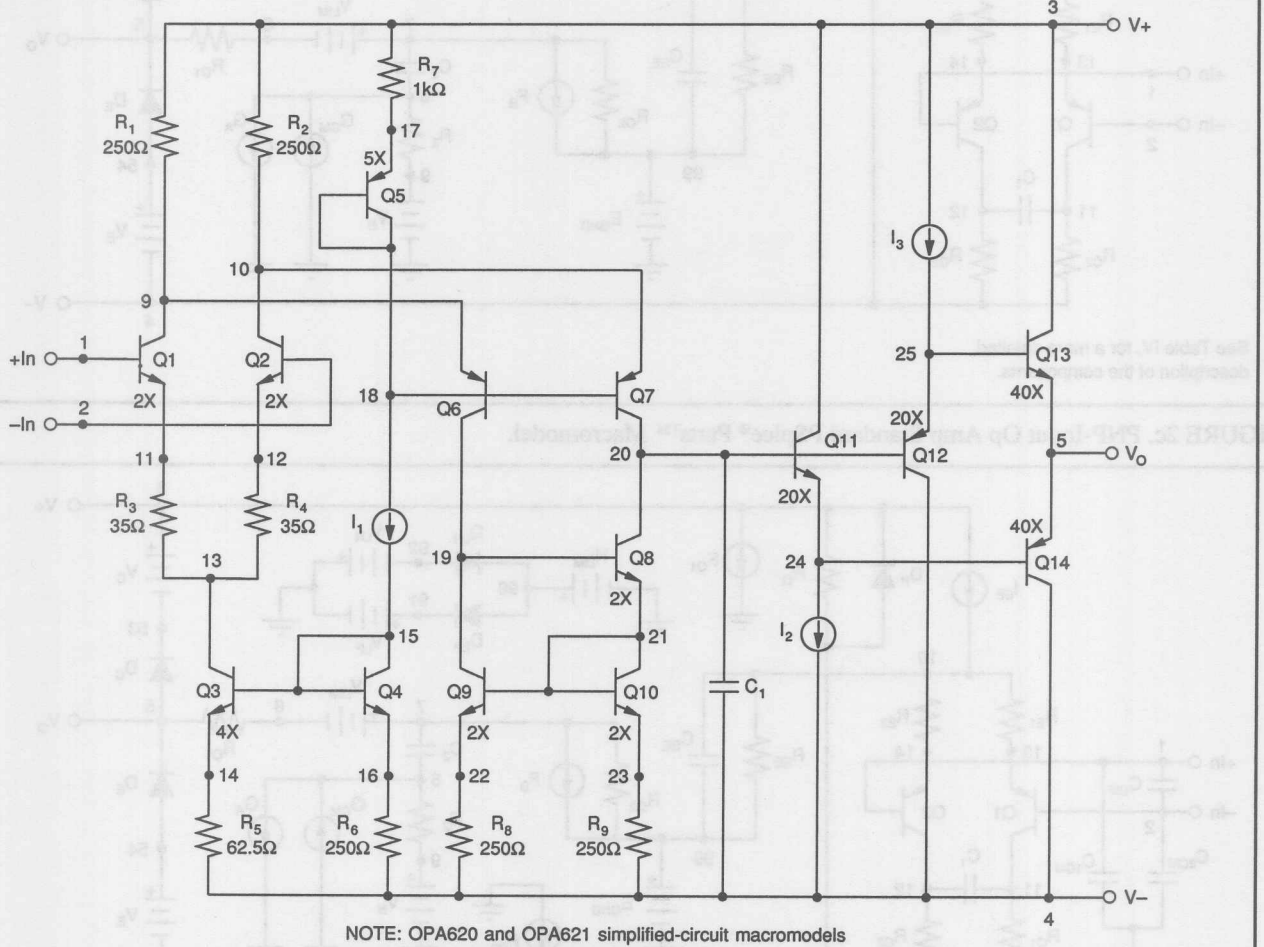
The standard macromodel simulates the following effects: 1) DC input impedance and bias current, 2) differential and common-mode gain, 3) open-loop gain and phase vs frequency (2 poles only), 4) output slew rate limiting and output resistance, 5) output voltage and current limiting, and 6) DC quiescent power drain.

EFFECTS THE STANDARD MACROMODEL DOES NOT SIMULATE

Some of the characteristics the standard macromodel does *not* simulate are: 1) distortion, 2) output current flowing from the power supplies, 3) noise 4) variations in performance vs temperature. 5) "Worst case" specifications (e.g. V_{OS}, I_{OS}, etc.), 6) Zeros in the gain-phase response, 7) more than 2 poles in gain-phase response.

EFFECTS THE ENHANCED MACROMODEL SIMULATES

The enhanced version of the standard PSpice® Parts™ model simulates the standard effects and, in addition, simulates: 1) quiescent current and output load current flowing from the power-supply pins, 2) input capacitance, 3) input protection circuitry where applicable.



NOTE: OPA620 and OPA621 simplified-circuit macromodels are the same with the following exceptions.

MODEL	C_1 (pF)	I_1 (mA)	I_2 (mA)	I_3 (mA)
OPA620	10	1.1	4	2
OPA621	2	1.3	3.5	3.5

FIGURE 3a. OPA620 and OPA621 High Speed Op Amp Simplified-Circuit Macromodel.

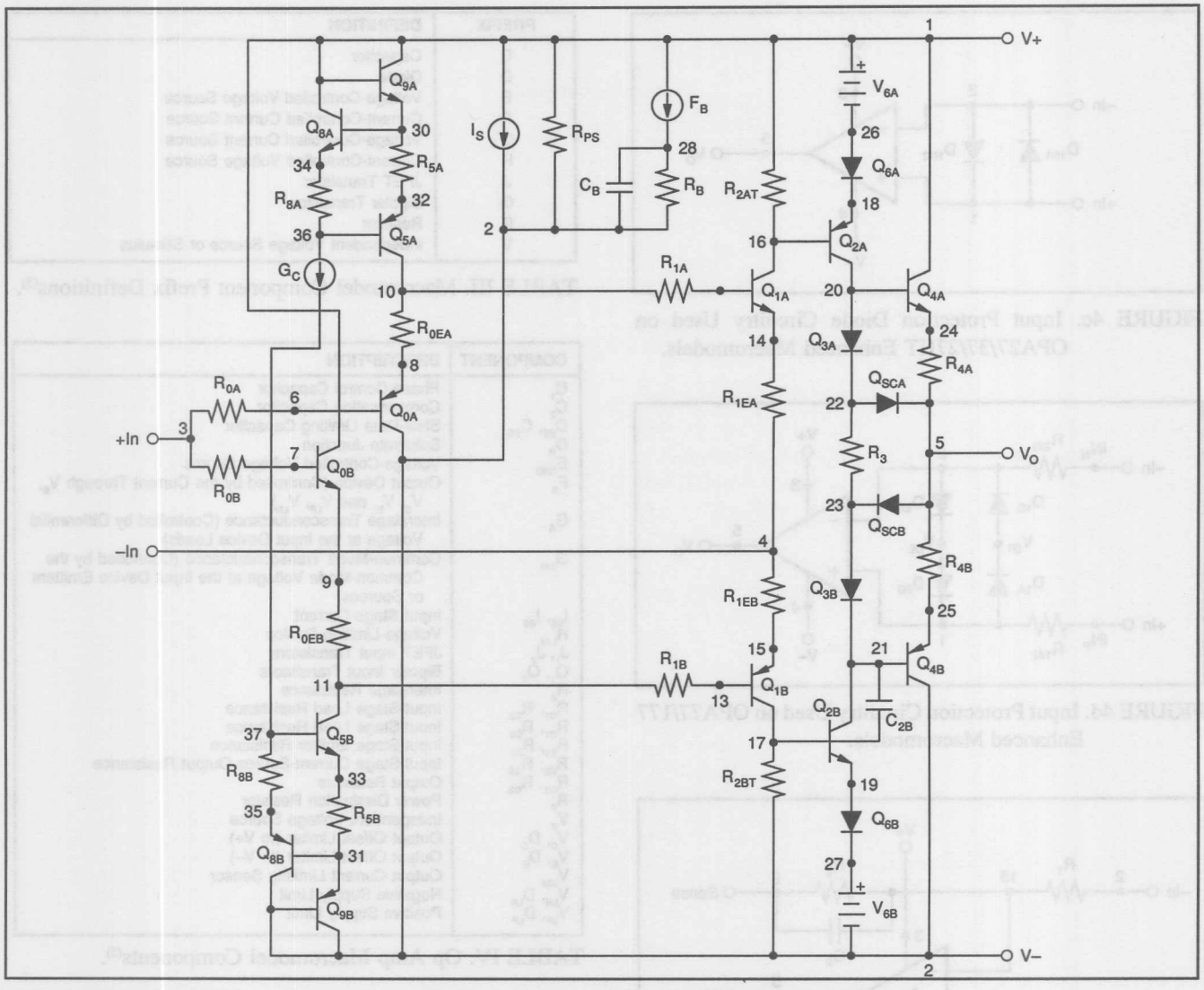


FIGURE 3b. OPA603 High Speed Current-Feedback Op Amp Simplified-Circuit Macromodel.

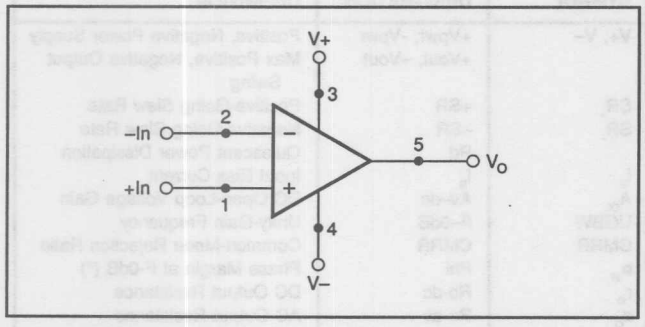
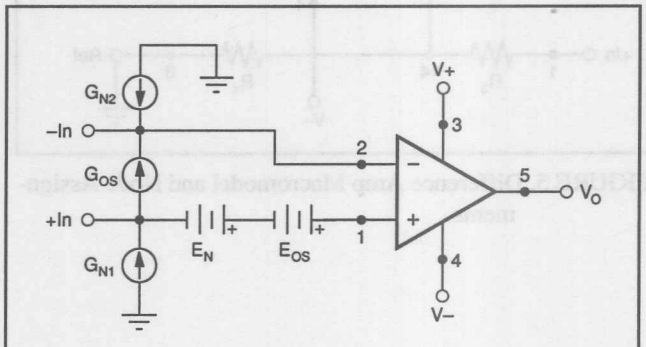


FIGURE 4a. Op Amp Macromodel Node Assignments.

SIMULATING OP AMP INPUT NOISE AND OFFSET

To simulate op amp input voltage noise, current noise, voltage offset, and current offset, error sources can be inserted as shown in Figure 4B.



ERROR-SOURCE DESIGNATIONS

DESIGNATION	DESCRIPTION
G_{OS}	Input Bias-Current Offset
E_N	Input Voltage Noise
E_{OS}	Input Offset Voltage
G_{N1}	+Input Bias-Current Noise
G_{N2}	–Input Bias-Current Noise

FIGURE 4b. Recommended Connection of Macromodel Noise and Offset Error Sources.

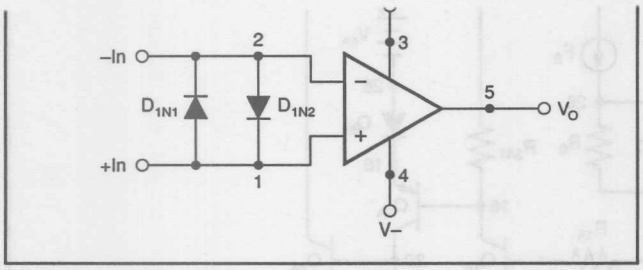


FIGURE 4c. Input Protection Diode Circuitry Used on OPA27/37/27HT Enhanced Macromodels.

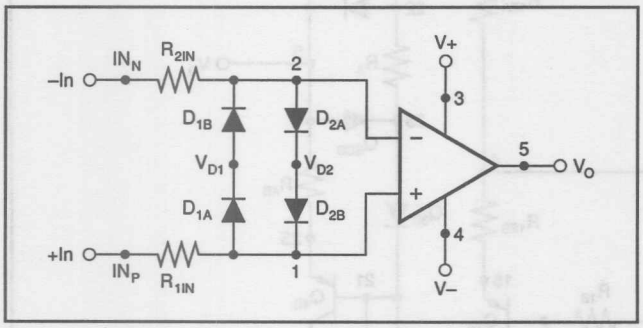


FIGURE 4d. Input Protection Circuitry Used on OPA77/177 Enhanced Macromodels.

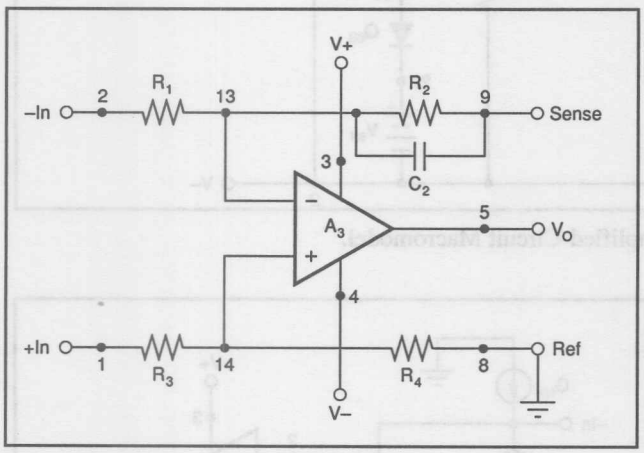


FIGURE 5. Difference Amp Macromodel and Node Assignments.

D	Diode
E	Voltage-Controlled Voltage Source
F	Current-Controlled Current Source
G	Voltage-Controlled Current Source
H	Current-Controlled Voltage Source
J	JFET Transistor
Q	Bipolar Transistor
R	Resistor
V	Independent Voltage Source or Stimulus

TABLE III. Macromodel Component Prefix Definitions[3].

COMPONENT	DESCRIPTION
C_1	Phase-Control Capacitor
C_2	Compensation Capacitor
C_{EE}, C_{SS}	Slew-Rate Limiting Capacitor
D_P	Substrate Junction
E_{GND}	Voltage-Controlled Voltage Source
F_B	Output Device (Controlled by the Current Through V_B, V_C, V_E, and V_{LP}, V_{LN})
G_A	Interstage Transconductance (Controlled by Differential Voltage at the Input Device Loads)
G_{CM}	Common-Mode Transconductance (Controlled by the Common-Mode Voltage at the Input Device Emitters or Sources)
I_{EE}, I_{SS}	Input Stage Current
H_{LIM}	Voltage-Limiting Device
J_1, J_2	JFET Input Transistors
Q_1, Q_2	Bipolar Input Transistors
R_2	Interstage Resistance
R_{C1}, R_{C2}	Input-Stage Load Resistance
R_{D1}, R_{D2}	Input-Stage Load Resistance
R_{E1}, R_{E2}	Input-Stage Emitter Resistance
R_{EE}, R_{SS}	Input-Stage Current-Source Output Resistance
R_{O1}, R_{O2}	Output Resistors
R_P	Power Dissipation Resistor
V_B	Independent Voltage Source
V_C, D_C	Output Offset Limiter (to V+)
V_E, D_E	Output Offset Limiter (to V–)
V_{LIM}	Output Current Limiting Sensor
V_{LN}, D_{LN}	Negative Supply Limit
V_{LP}, D_{LP}	Positive Supply Limit

TABLE IV. Op Amp Macromodel Components[3].

BURR-BROWN SYMBOL	MACROMODEL DESIGNATION	DEFINITION
V+, V–	+Vpwr, -Vpwr	Positive, Negative Power Supply
	+Vout, –Vout	Max Positive, Negative Output Swing
SR_+	+SR	Positive-Going Slew Rate
SR_-	–SR	Negative-Going Slew Rate
	Pd	Quiescent Power Dissipation
I_B	I_B	Input Bias Current
A_{OL}	Av–dc	DC Open-Loop Voltage Gain
UGBW	F–0dB	Unity-Gain Frequency
CMRR	CMRR	Common-Mode Rejection Ratio
$ø_M$	Phi	Phase Margin at F-0dB (°)
r_O	Ro-dc	DC Output Resistance
z_O	Ro-ac	AC Output Resistance
I_{SC}	Ios	Short-Circuit Output Current
C_C	Cc	Compensation Cacitance

TABLE V. PSpice® Parts™ Inputs[3].

3) Per MicroSim Corp. PSpice®.

PRODUCT HIGHLIGHTS AND NOTES

INA101
INSTRUMENTATION AMPLIFIER

KEY FEATURES

Input offset voltage: 25µV max
Input offset voltage drift: 0.25µV/°C max
CMR: 106dB (60Hz) min
Available packages: Hermetic Ceramic DIP, Hermetic Metal TO-100, Plastic DIP, and Plastic SOIC.
See Figure 6 for macromodel circuit diagram.

Notes about the INA101:
The INA101 contains internal gain-setting feedback resistors;

$$R_{FB} = 20k\Omega$$

When using the metal package (TO-100) these resistors must be used. When using the ceramic or plastic packages, the internal gain-setting feedback resistors may be used, or external feedback resistors may be used.

If the internal resistors are used:

$$GAIN = 1 + (40K/R_G)$$

If external feedback resistors are used:

$$GAIN = 1 + (2 \bullet R_{FB}/R_G)$$

Where:
R_G = external gain-setting resistor (Ω)
R_{FB} = optional external feedback resistor (Ω)
See product data sheet (PDS-454) for gain accuracy specifications.

INA102
INSTRUMENTATION AMPLIFIER

Low quiescent current: 750µA max
Internal gains: 1, 10, 100, 1000 (V/V)
Low gain drift: 5, 10, 15, 20ppm/°C max, Gain = 1, 10, 100, 1000
Input offset voltage: 100µV max
Input offset voltage drift: 2µV/°C max
CMR: 90dB (60Hz)
Available packages: Hermetic Ceramic DIP, Plastic DIP, and Plastic SOIC.

See Figure 6 for macromodel circuit diagram.

Notes about the INA102:
The INA102 contains internal gain-setting and feedback resistors;

$$R_{FB} = 20k\Omega$$

INA102 INTERNAL GAIN-SETTING RESISTORS

R_G (Ω)	GAIN (V/V)
4.444k	10
404	100
40.4	1000

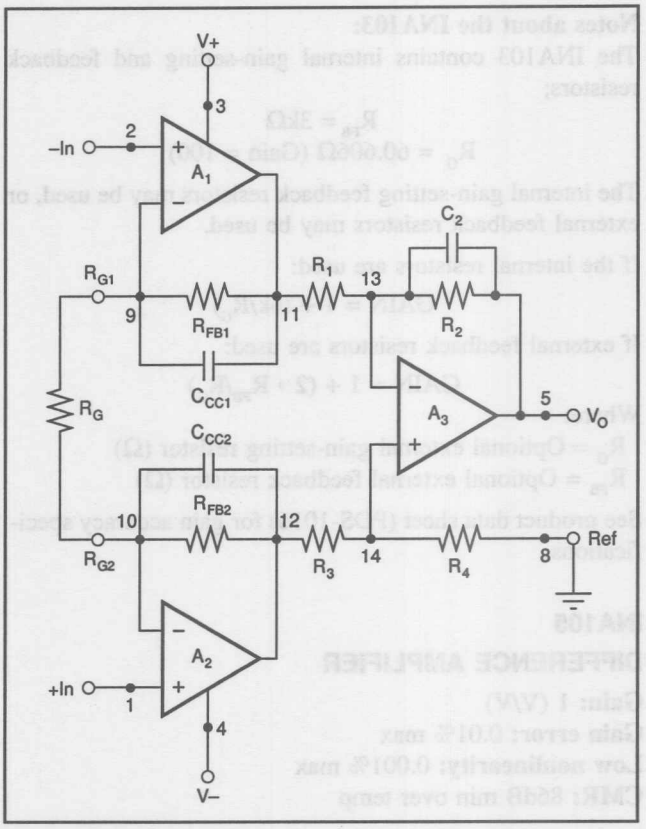


FIGURE 6. Standard Instrumentation Amplifier Macromodel and Node Assignments.

The internal resistors are ratio trimmed to high accuracy and have excellent tracking with temperature for low gain drift.
If the internal resistors are used:

$$GAIN = 1 + (40k/R_G)$$

External gain-setting resistors can be used in series with one of the internal gain-setting resistors. If external gain-setting resistors are used:

$$GAIN = 1 + (40k/[R_{GI} + R_{GE}])$$

R_{GI} = One of the three internal gain-setting resistors shown in the table (Ω)
R_{GE} = external gain-setting resistor (Ω)

See product data sheet (PDS-523) for gain accuracy specifications.

INA103
INSTRUMENTATION AMPLIFIER

Low noise: $1nV/\sqrt{Hz}$
Low THD: 0.002% (20Hz to 20kHz, Gain = 1 to 100)
Wide supply range: ±9V to ±24V
High gain-bandwidth: 100MHz, Gain=1000
Internal gains: 1, 100 (V/V)
Input offset voltage: 100µV max
Input offset voltage drift: 2µV/°C max
CMR: 110dB min
Available packages: Hermetic Ceramic DIP and Plastic DIP

See Figure 7 for macromodel circuit diagram.

Notes about the INA103:
The INA103 contains internal gain-setting and feedback resistors;

$$R_{FB} = 3k\Omega$$
$$R_G = 60.606\Omega \text{ (Gain = 100)}$$

The internal gain-setting feedback resistors may be used, or external feedback resistors may be used.

If the internal resistors are used:

$$GAIN = 1 + (6k/R_G)$$

If external feedback resistors are used:

$$GAIN = 1 + (2 \bullet R_{FB}/R_G)$$

Where:
R_G = Optional external gain-setting resistor (Ω)
R_{FB} = Optional external feedback resistor (Ω)

See product data sheet (PDS-1016) for gain accuracy specifications.

INA105
DIFFERENCE AMPLIFIER

Gain: 1 (V/V)
Gain error: 0.01% max
Low nonlinearity: 0.001% max
CMR: 86dB min over temp
Available packages: Hermetic Metal TO-99, Plastic DIP, and Plastic SOIC.

See Figure 5 for macromodel circuit diagram.

INA106
DIFFERENCE AMPLIFIER

Gain: 10 (V/V)
Gain error: 0.01% max
Low nonlinearity: 0.001% max
CMR: 100dB min over temp
Available packages: Hermetic Metal TO-99 and Plastic DIP.

See Figure 5 for macromodel circuit diagram.

INA110
INSTRUMENTATION AMPLIFIER

FET input
Bias current: 50pA max
Internal gains: 1, 10, 100, 200, 500 (V/V)
Low gain drift: 10 to 50 ppm/°C
Input offset voltage drift: 2μV/°C max
CMR: 106dB min
Available packages: Hermetic Ceramic DIP, Plastic DIP, and Plastic SOIC.

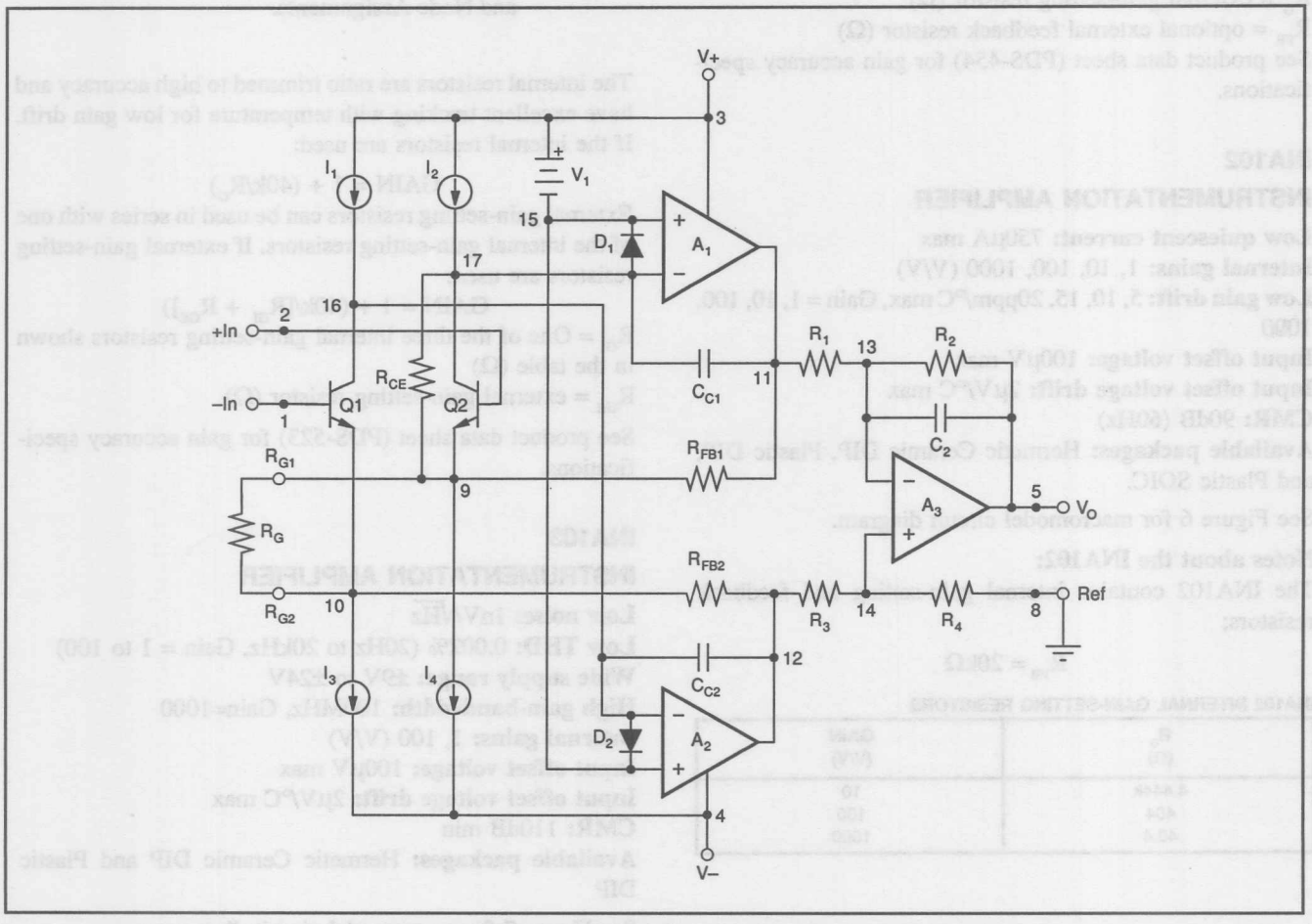


FIGURE 7. INA103 Current-Feedback Instrumentation Amplifier Macromodel and Node Assignments.

See Figure 8 for macromodel circuit diagram.

Notes about the macromodel:
The INA110 contains internal gain-setting and feedback resistors;

$$R_{FB} = 20k\Omega$$

INA110 INTERNAL GAIN-SETTING RESISTORS

R_G (Ω)	GAIN (V/V)
4.4444k	10
404.04	100
201.0	200
80.16	500

The internal resistors are ratio trimmed to high accuracy and have excellent tracking with temperature for low gain drift. If the internal resistors are used:

$$GAIN = 1 + (40k/R_G)$$

External gain-setting resistors can be used in series with one of the internal gain-setting resistors. If external gain-setting resistors are used:

$$GAIN = 1 + (40k/[R_{GI} + R_{GE}])$$

R_{GI} = one of the four above internal gain-setting resistors (Ω)
R_{GE} = external gain-setting resistor (Ω)

See product data sheet (PDS-645) for gain accuracy specifications.

INA117

HIGH COMMON-MODE VOLTAGE DIFFERENCE AMPLIFIER

Gain: 1 (V/V)
Gain error: 0.02% max
Low nonlinearity: 0.001% max
Common-mode input range: ±200V
Input protection: ±500V common-mode or differential
CMR: 106dB (60Hz)
Available packages: Hermetic Metal TO-99, Plastic 8-pin DIP, and Plastic 8-pin SOIC.
See Figure 9 for macromodel circuit diagram.

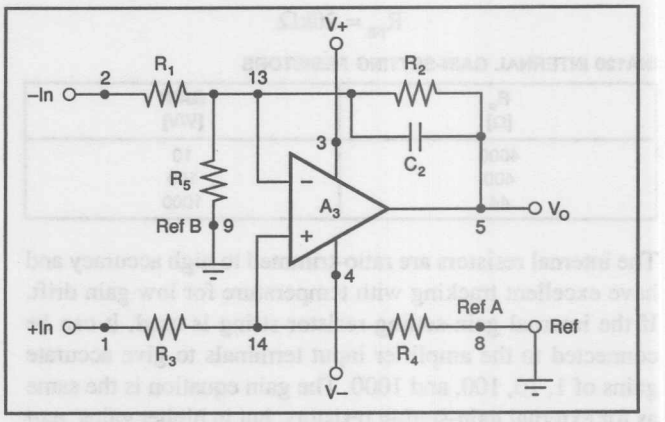


FIGURE 9. INA117 High Voltage Difference Amplifier Macromodel and Node Assignments.

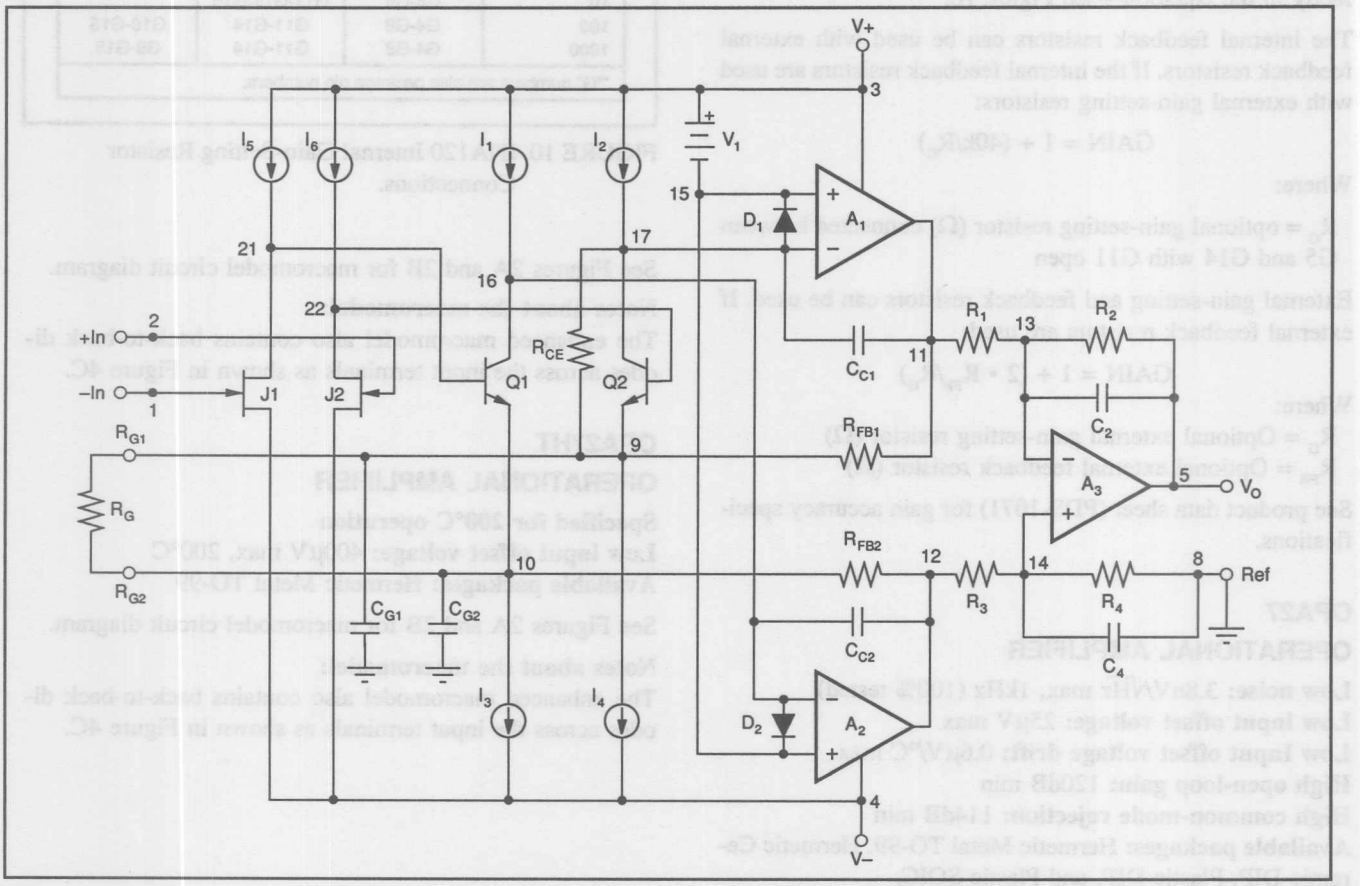


FIGURE 8. INA110 Current-Feedback FET-Input Instrumentation Amplifier Macromodel and Node Assignments.

INSTRUMENTATION AMPLIFIER

Input offset voltage: 25µV max
Input offset voltage drift: 0.25µV/°C max
Internal gains: 1, 10, 100, 1000 (V/V)
CMR: 106dB (60Hz, Gain = 100)
Available packages: Hermetic Ceramic DIP and Plastic DIP.

See Figure 6 for macromodel circuit diagram.

Notes about the INA120:
The INA120 contains an internal gain-setting and feedback resistor string;

$$R_{FB} = 20k\Omega$$

INA120 INTERNAL GAIN-SETTING RESISTORS

R_G [Ω]	GAIN [V/V]
4000	10
400	100
44	1000

The internal resistors are ratio-trimmed to high accuracy and have excellent tracking with temperature for low gain drift. If the internal gain-setting resistor string is used, it can be connected to the amplifier input terminals to give accurate gains of 1, 10, 100, and 1000. The gain equation is the same as for external gain-setting resistors, but in higher gains, part of the lower gain-setting resistor is added to the feedback resistor so the values shown for R_G can not be inserted directly in the equation—see Figure 10.

The internal feedback resistors can be used with external feedback resistors. If the internal feedback resistors are used with external gain-setting resistors:

$$GAIN = 1 + (40k/R_G)$$

Where:

R_G = optional gain-setting resistor (Ω) connected between G5 and G14 with G11 open

External gain-setting and feedback resistors can be used. If external feedback resistors are used:

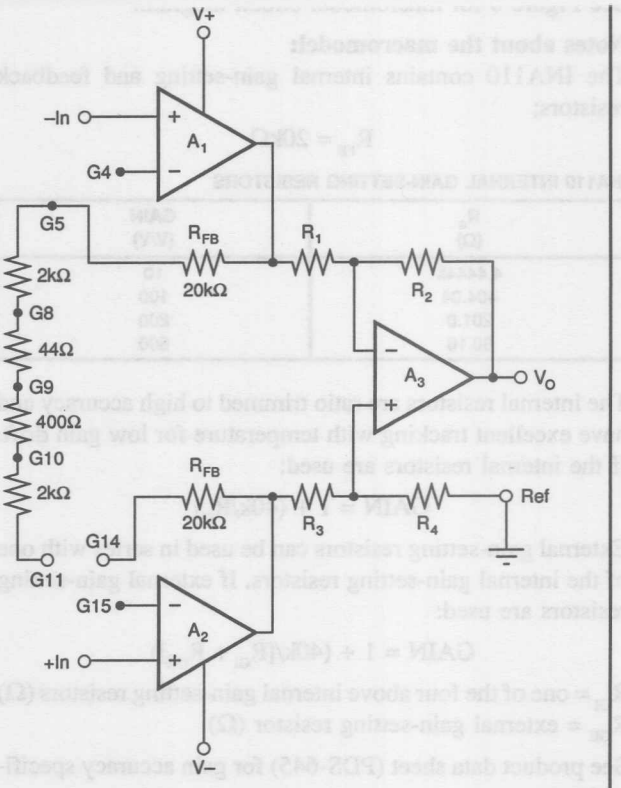
$$GAIN = 1 + (2 \bullet R_{FB}/R_G)$$

Where:
R_G = Optional external gain-setting resistor (Ω)
R_{FB} = Optional external feedback resistor (Ω)

See product data sheet (PDS-1071) for gain accuracy specifications.

OPA27
OPERATIONAL AMPLIFIER

Low noise: 3.8nV/√Hz max, 1kHz (100% tested)
Low input offset voltage: 25µV max
Low Input offset voltage drift: 0.6µV/°C max
High open-loop gain: 120dB min
High common-mode rejection: 114dB min
Available packages: Hermetic Metal TO-99, Hermetic Ceramic DIP, Plastic DIP, and Plastic SOIC.



INA120 INTERNAL GAIN CONNECTIONS*

GAIN	CONNECT		
1	G4-G5	G14-G15	
10	G4-G5	G11-G14-G15	
100	G4-G8	G11-G14	G10-G15
1000	G4-G8	G11-G14	G9-G15

*"G" numbers are also package pin numbers.

FIGURE 10. INA120 Internal Gain-Setting Resistor Connections.

See Figures 2A and 2B for macromodel circuit diagram.

Notes about the macromodel:
The enhanced macromodel also contains back-to-back diodes across the input terminals as shown in Figure 4C.

OPA27HT
OPERATIONAL AMPLIFIER

Specified for 200°C operation
Low input offset voltage: 400µV max, 200°C
Available packages: Hermetic Metal TO-99

See Figures 2A and 2B for macromodel circuit diagram.

Notes about the macromodel:
The enhanced macromodel also contains back-to-back diodes across the input terminals as shown in Figure 4C.

OPA37

OPERATIONAL AMPLIFIER

Stable in gain of 5V/V or higher
Small signal gain-bandwidth: 63MHz typ
Slew rate: 11.9V/µs typ
Low noise: 3.8nV/√Hz max, 1kHz (100% tested)
Low input offset voltage: 25µV max
Low Input offset voltage drift: 0.6µV/°C max
High open-loop gain: 120dB min
High common-mode rejection: 114dB min
Available packages: Hermetic Metal TO-99, Hermetic Ceramic DIP, Plastic DIP, and Plastic SOIC

See Figures 2A and 2B for macromodel circuit diagram.

Notes about the macromodel:
The enhanced macromodel also contains back-to-back diodes across the input terminals as shown in Figure 4C.

OPA77

OPERATIONAL AMPLIFIER

Low input offset voltage: 25µV max
Low Input offset voltage drift: 0.3µV/°C max
High open-loop gain: 130dB min
High common-mode rejection: 120dB min
Quiescent current: 1.5mA
Available packages: Hermetic Ceramic DIP, Plastic DIP, and Plastic SOIC.

See Figures 2A and 2B for macromodel circuit diagram.

Notes about the macromodel:
The enhanced macromodel also contains input protection diodes and resistors as shown in Figure 4D.

OPA101

OPERATIONAL AMPLIFIER

FET input
Low bias current: 10pA max
Low noise: 8nV/√Hz max, 10kHz (100% tested)
Low input offset voltage: 250µV max
Low Input offset voltage drift: 5µV/°C max
Available packages: Hermetic Metal TO-99

See Figures 1A and 1B for macromodel circuit diagram.

OPA102

OPERATIONAL AMPLIFIER

FET input
Stable in gain of 3V/V or higher
Small-signal gain-bandwidth: 40MHz typ
Slew rate: 10V/µs
Low bias current: 10pA max
Low noise: 8nV/√Hz max, 10kHz (100% tested)
Low input offset voltage: 250µV max
Low Input offset voltage drift: 5µV/°C max
Available packages: Hermetic Metal TO-99

See Figures 1A and 1B for macromodel circuit diagram.

OPA111

OPERATIONAL AMPLIFIER

FET input
Low bias current: 1pA max
Low noise: 8nV/√Hz max, 10kHz (100% tested)
Low input offset voltage: 250µV max
Low Input offset voltage drift: 1µV/°C max
Available packages: Hermetic Metal TO-99

See Figures 1C and 1D for macromodel circuit diagram.

Notes about the macromodel:
The OPA111 slew rate is asymmetric with the positive-going slope faster than the negative-going slope (4V/µs vs 2V/µs). Since the PSpice macromodel only allows asymmetric slew rate in the opposite direction, a conservative symmetrical slew rate of 2V/µs was usedin the macromodel.

OPA121

OPERATIONAL AMPLIFIER

FET input
Low bias current: 5pA max
Low noise: 6nV/√Hz typ, 10kHz
Input offset voltage: 2mV max
Input offset voltage drift: 3µV/°C typ
Available packages: Hermetic Metal TO-99 and 8-pin Plastic DIP

See Figures 1C and 1D for macromodel circuit diagram.

Notes about the macromodel:
The OPA121 slew rate is asymmetric with the positive-going slope faster than the negative-going slope (4V/µs vs 2V/µs). Since the PSpice macromodel only allows asymmetric slew rate in the opposite direction, a conservative symmetrical slew rate of 2V/µs was used in the macromodel.

OPA128

OPERATIONAL AMPLIFIER

FET input
Ultra low bias current: 75fA max
Low input offset voltage: 500µV max
Low Input offset voltage drift: 5µV/°C max
Available packages: Hermetic Metal TO-99
See Figures 1C and 1D for macromodel circuit diagram.

OPA177

OPERATIONAL AMPLIFIER

Low input offset voltage: 10µV max
Low Input offset voltage drift: 0.1µV/°C max
High open-loop gain: 130dB min
High common-mode rejection: 130dB min
Quiescent current: 1.5mA
Available packages: Hermetic Ceramic DIP, Plastic DIP, and Plastic SOIC.

See Figures 2A and 2B for macromodel circuit diagram.

Notes about the macromodel:
The enhanced macromodel also contains input protection diodes and resistors as shown in Figure 4D.

OPA404
QUAD OPERATIONAL AMPLIFIER

FET input
Low bias current: 4pA max
Small-signal gain-bandwidth: 6.4MHz
Slew rate: 35V/µs
Available packages: Hermetic Ceramic DIP and Plastic DIP

See Figures 1C and 1D for macromodel circuit diagram.

OPA445
HIGH VOLTAGE OPERATIONAL AMPLIFIER

FET input
Wide power supply range: ±10V to ±45V
Low bias current: 50pA max
Available packages: Hermetic Metal TO-99 and 8-pin Plastic DIP

See Figures 1C and 1D for macromodel circuit diagram.

OPA501
POWER OPERATIONAL AMPLIFIER

Wide power supply range: ±10V to ±40V
High output current: ±10A peak
Available package: Hermetic Metal TO-3

See Figures 2A and 2B for macromodel circuit diagram.

OPA511
POWER OPERATIONAL AMPLIFIER

Wide power supply range: ±10V to ±30V
High output current: ±5A peak
Low distortion class A/B output stage
Available package: Hermetic Metal TO-3

See Figures 1C and 1D for macromodel circuit diagram.

OPA512
POWER OPERATIONAL AMPLIFIER

Wide power supply range: ±10V to ±50V
High output current: ±15A peak
Low distortion class A/B output stage
Available package: Hermetic Metal TO-3

See Figures 1C and 1D for macromodel circuit diagram.

OPA541
POWER OPERATIONAL AMPLIFIER

FET input
Low bias current: 50pA max
Wide power supply range: ±10V to ±40V
High output current: ±10A peak
Available package: Hermetic Metal TO-3

See Figures 1C and 1D for macromodel circuit diagram.

OPA602
OPERATIONAL AMPLIFIER

FET input
Low bias current: 1pA max
Fast settling: 1µs, 0.01%
Small-signal gain-bandwidth: 6.5MHz
Slew rate: 35V/µs
Low input offset voltage: 250µV max
Low input offset voltage drift: 2µV/°C max
Available packages: Hermetic Metal TO-99, Plastic 8-pin DIP, and Plastic 8-pin SOIC.

See Figures 1C and 1D for macromodel circuit diagram.

OPA603
(HAS SIMPLIFIED CIRCUIT MODEL ONLY)
CURRENT-FEEDBACK OPERATIONAL AMPLIFIER

Wide power supply range: ±4.5V to ±18V
High output current: ±150mA peak
Low distortion
  Differential gain: 0.03%, 4.43MHz
  Differential phase: 0.025%, 4.43MHz
Fast settling: 50ns, 0.1%
Small-signal gain-bandwidth: 45MHz, Gain = 1 to 100
High slew rate: 1000V/µs
Available packages: Plastic 8-pin DIP

See Figure 3B for macromodel circuit diagram.

OPA606
OPERATIONAL AMPLIFIER

FET input
Low bias current: 10pA max
Small-signal gain-bandwidth: 13MHz
Slew rate: 35V/µs
Low input offset voltage: 500µV max
Input offset voltage drift: 5µV/°C max
Available packages: Hermetic Metal TO-99 and Plastic 8-pin DIP

See Figures 1C and 1D for macromodel circuit diagram.

OPA620
(HAS PSpice® AND SIMPLIFIED CIRCUIT MODEL)
OPERATIONAL AMPLIFIER

Low distortion
Differential gain: 0.05%, 3.58MHz
Differential phase: 0.05%, 3.58MHz
Fast settling: 25ns, 0.01%
Small-signal gain-bandwidth: 200MHz
Slew rate: 250V/µs
Low input offset voltage: 100µV max
Available packages: Plastic 8-pin DIP and Plastic 8-pin SOIC.

See Figures 2A and 2B for macromodel circuit diagram.

OPA621
(HAS PSpice® AND SIMPLIFIED CIRCUIT MODEL)
OPERATIONAL AMPLIFIER

Stable in gain of 2V/V or higher
Low distortion
Differential gain: 0.05%, 3.58MHz
Differential phase: 0.05%, 3.58MHz
Fast settling: 25ns, 0.01%
Small-signal gain-bandwidth: 500MHz
Slew rate: 500V/µs
Low input offset voltage: 100µV max
Available packages: Plastic 8-pin DIP and Plastic 8-pin SOIC.

See Figures 2A and 2B for macromodel circuit diagram.

OPA627
OPERATIONAL AMPLIFIER

FET input
Low bias current: 20pA max
Low noise: 4.5nV/$\sqrt{\text{Hz}}$ max, 10kHz
Low distortion: 0.00003%, 1kHz, Gain = +1V/V
Fast settling: 550ns, 0.01%
Small-signal gain-bandwidth: 16MHz
Slew rate: 55V/µs
Low input offset voltage: 100µV max
Low input offset voltage drift: 0.8µV/°C max
Available packages: Hermetic Metal TO-99, Plastic 8-pin DIP, and Plastic 8-pin SOIC.

See Figures 1C and 1D for macromodel circuit diagram.

OPA637
OPERATIONAL AMPLIFIER

Stable in gain of 5V/V or higher
FET input
Low bias current: 20pA max
Low noise: 4.5nV/$\sqrt{\text{Hz}}$ max, 10kHz
Low distortion: 0.00003%, 1kHz, Gain = +1V/V
Fast settling: 450ns, 0.01%
Small-signal gain-bandwidth: 80MHz
Slew rate: 135V/µs
Low input offset voltage: 100µV max
Low Input offset voltage drift: 0.8µV/°C max
Available packages: Hermetic Metal TO-99, Plastic 8-pin DIP, and Plastic 8-pin SOIC.

See Figures 1C and 1D for macromodel circuit diagram.

OPA1013
DUAL SINGLE-SUPPLY
OPERATIONAL AMPLIFIER

Single power supply operation
Input common-mode range to negative supply or ground
Output swings near negative supply or ground
Low quiescent current: 500µA max
Low input offset voltage: 150µV max
Input offset voltage drift: 2µV/°C max
Input bias-current offset: 0.8nA max

See figures 3A and 3B for macromodel circuit diagram.

OPA2107
DUAL OPERATIONAL AMPLIFIER

FET input
Low bias current: 5pA max
Low noise: 8nV/$\sqrt{\text{Hz}}$ max, 10kHz
Fast settling: 2µs, 0.01%
Slew rate: 18V/µs
Low input offset voltage: 500µV max
Input offset voltage drift: 5µV/°C max
Available packages: Hermetic Metal TO-99, Plastic 8-pin DIP, and Plastic 8-pin SOIC.

See Figures 1C and 1D for macromodel circuit diagram.

OPA2111
OPERATIONAL AMPLIFIER

Dual op amp
FET input
Low bias current: 1pA max
Low noise: 8nV/$\sqrt{\text{Hz}}$ max, 10kHz (100% tested)
Low input offset voltage: 250µV max
Low Input offset voltage drift: 1µV/°C max
Available packages: Hermetic Metal TO-99

See Figures 1C and 1D for macromodel circuit diagram.

Notes about the macromodel:
The OPA2111 slew rate is asymmetric with the positive-going slope faster than the negative-going slope (4V/µs vs 2V/µs). Since the PSpice macromodel only allows asymmetric slew rate in the opposite direction, a conservative symmetrical slew rate of 2V/µs was used in the macromodel.

Dual op amp
FET input
Low bias current: 50pA max
Wide power supply range: ±10V to ±40V
High output current: ±10A peak
Available package: Hermetic Metal TO-3

See Figures 1C and 1D for macromodel circuit diagram.

OPA2604

DUAL OPERATIONAL AMPLIFIER

FET input
Wide power supply range: ±4.5V to ±24V
Bias current: 100pA max
Low noise: 10nV/√Hz max, 10kHz
Low distortion: 0.0003%, 1kHz, Gain = +1V/V
Fast settling: 2µs, 0.01%
Slew rate: 25V/µs
Small signal gain-bandwidth: 10MHz
Input offset voltage: 2mV max
Input offset voltage drift: 5µV/°C typ
Available packages: Plastic 8-pin DIP and Plastic 8-pin SOIC.

See Figures 1C and 1D for macromodel circuit diagram.

SAMPLE MACROMODEL LISTINGS

STANDARD OPA27 OP AMP MACROMODEL

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* OPA27 OPERATIONAL AMPLIFIER "MACROMODEL"
SUBCIRCUIT
* CREATED USING PARTS RELEASE 4.03 ON 09/
20/90 AT 16:00
```



```
*                  | | POSITIVE POWER SUPPLY
*                  | | | NEGATIVE POWER SUPPLY
*                  | | | | OUTPUT
*                  | | | | |
*SUBCKT OPA27  1 2 3 4 5
*
C1     11   12   20.79E-12
C2      6    7   114.3E-12
CEE    10   99   5.713E-12
DC      5   53   DX
DE     54    5   DX
DLP    90   91   DX
DLN    92   90   DX
DP      4    3   DX
EGND   99    0   POLY(2) (3,0) (4,0) 0 .5 .5
FB      7   99   POLY(5) VB VC VE VLP VLN 0
                 10.95E6 -10E6 10E6 10E6
                 -10E6
GA      6    0   11 12 4.638E-3
GCM     0    6   10 99 2.608E-9
IEE    10    4   DC 240.0E-6
HLIM   90    0   VLIM 1K
Q1     11    2   13 QX
Q2     12    1   14 QX
R2      6    9   100.0E3
RC1     3   11   215.6
RC2     3   12   215.6
RE1    13   10   5.395E-3
RE2    14   10   5.395E-3
REE    10   99   833.5E3
RO1     8    5   35
RO2     7   99   35
RP      3    4   10.87E3
VB      9    0   DC 0
VC      3   53   DC 1.200
VE     54    4   DC 1.200
VLIM    7    8   DC 0
VLP    91    0   DC 25
VLN     0   92   DC 25
.MODEL DX D(IS=800.0E-18)
.MODEL QX NPN(IS=800.0E-18 BF=7.998E3)
.ENDS
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ENHANCED OPA27 OP AMP MACROMODEL

```
* OPA27E OPERATIONAL AMPLIFIER "MACROMODEL"
SUBCIRCUIT
* "E" IS ENHANCED MODEL
* CREATED USING PARTS RELEASE 4.03 ON 09/
05/90 AT 10:27
```



```
*CONNECTIONS: NON-INVERTING INPUT
*              | INVERTING INPUT
*              | | POSITIVE POWER SUPPLY
*              | | | NEGATIVE POWER SUPPLY
*              | | | | OUTPUT
*              | | | | |
*SUBCKT OPA27E 1 2 3 4 5
*
C1     11   12   20.79E-12
C2      6    7   114.3E-12
CEE    10   99   5.713E-12
DC      5   53   DX
DE     54    5   DX
DLP    90   91   DX
DLN    92   90   DX
DP      4    3   DX
EGND   99    0   POLY(2) (3,0) (4,0) 0 .5 .5
FB      7   99   POLY(5) VB VC VE VLP VLN 0
                 10.95E6 -10E6 10E6 10E6
                 -10E6
GA      6    0   11 12 4.638E-3
GCM     0    6   10 99 2.608E-9
IEE    10    4   DC 240.0E-6
HLIM   90    0   VLIM 1K
Q1     11    2   13 QX
Q2     12    1   14 QX
R2      6    9   100.0E3
RC1     3   11   215.6
RC2     3   12   215.6
RE1    13   10   5.395E-3
RE2    14   10   5.395E-3
REE    10   99   833.5E3
RO1     8    5   35
RO2     7   99   35
RP      3    4   10.87E3
VB      9    0   DC 0
VC      3   53   DC 1.200
VE     54    4   DC 1.200
VLIM    7    8   DC 0
VLP    91    0   DC 25
VLN     0   92   DC 25
* OPA27 "E" - ENHANCEMENTS
* OUTPUT SUPPLY MIRROR
FQ3     0   20   POLY(1) VLIM 0  1
DQ1    20   21   DX
DQ2    22   20   DX
VQ1    21    0   0
VQ2    22    0   0
FQ1     3    0   POLY(1) VQ1  1.56E-3  1
FQ2     0    4   POLY(1) VQ2  1.56E-3 -1
* QUIESCIENT CURRENT
RQ      3    4   2.5E4
* DIFF INPUT CAPACITANCE
CDIF    1    2   5.0E-12
* COMMON MODE INPUT CAPACITANCE
C1CM    1   99   2.5E-12
C2CM    2   99   2.5E-12
* INPUT PROTECTION
DIN1    1    2   DX
DIN2    2    1   DX
.MODEL DX D(IS=800.0E-18)
.MODEL QX NPN(IS=800.0E-18 BF=7.998E3)
.ENDS
```

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MODEL INDEX